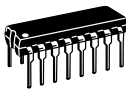
Quad Latch

MC10168

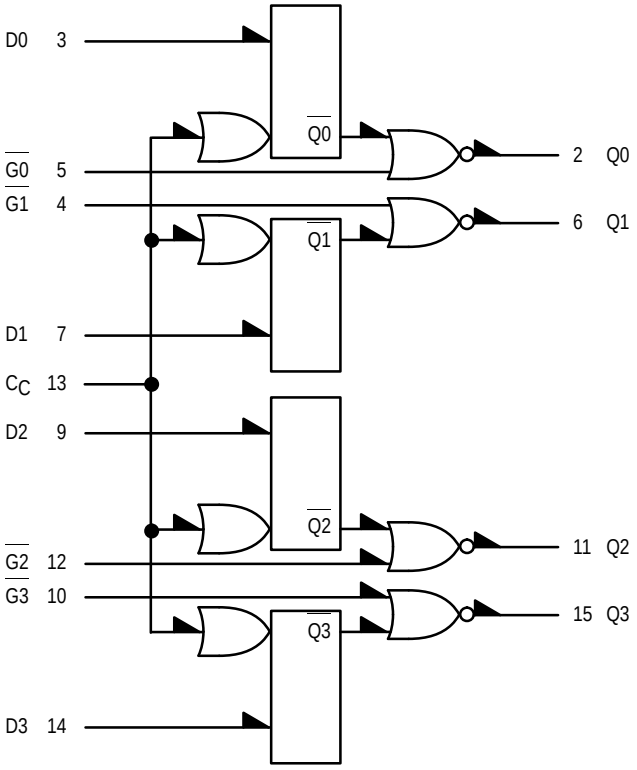
The MC10168 is a Quad Latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative–going transition of the clock.

P_D = 310 mW typ/pkg (No Load)
t_{pd} = G to Q = 2 ns typ
D to Q = 3 ns typ
C to Q = 4 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)



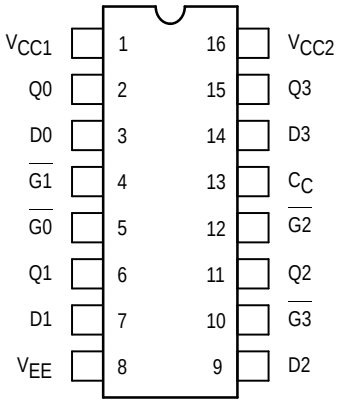
P SUFFIX
PLASTIC PACKAGE
CASE 648–08

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

PIN ASSIGNMENT



TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	X	X	L
L	L	X	Q_n
L	H	L	L
L	H	H	H

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		82		60	75		82	mAdc
Input Current	I_{inH}	3,7,9,14 4,5,10,12 13		390 425 460			245 265 290		245 265 290	µAdc
	I_{inL}	*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 6	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 6	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 6	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 6		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Data	t_{3+2+}	2	1.0	5.6	1.0	3.0	5.4	1.1	5.9	
Gate	t_{5-2+}	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4	
Clock	t_{13+2+}	2	1.0	5.8	1.0	4.0	5.6	1.2	6.2	
Setup Time	t_{3+13+}	2	2.5		2.5			2.5		
Hold Time	t_{13+3+}	2	1.0		1.0			1.0		
Rise Time (20 to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	
Fall Time (20 to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	

* Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS (continued)

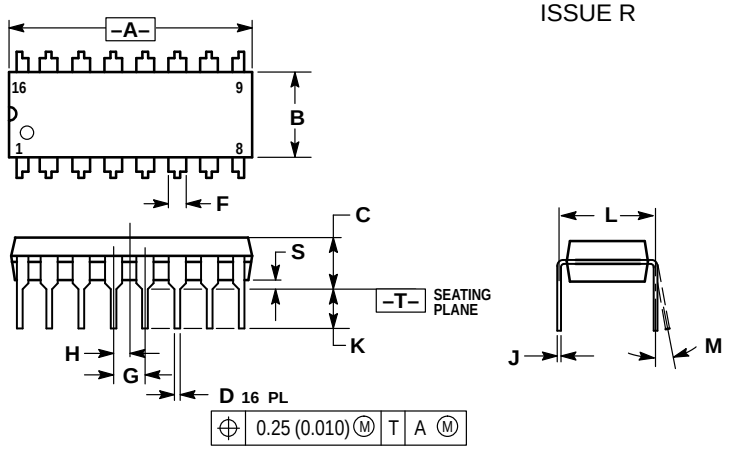
@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**				**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	3,7,9,14 4,5,10,12 13	* * 13				8 8 8	1, 16 1, 16 1, 16
		I_{inL}	*		*			8	1, 16
Output Voltage	Logic 1	V_{OH}	2 6	3, 13 7, 13				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2 6	3, 5 4, 7				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 6	13 13		3 7		8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2 6	13 13			3 7	8 8	1, 16 1, 16
Switching Times	(50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Data	t_{3+2+}	2			3	2	8	1, 16
	Gate	t_{5-2+}	2			5	2	8	1, 16
	Clock	t_{13+2+}	2			13	2	8	1, 16
Setup Time		t_{3+13+}	2					8	1, 16
Hold Time		t_{13+3+}	2					8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2			3	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			3	2	8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298