MC10129

Quad Bus Receiver

The MC10129 data inputs are compatible with, and accept TTL logic levels as well as levels compatible with IBM–type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, and the reset input is disabled, the outputs will follow the D inputs. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V_{CC} or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to V_{EE}. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V_{EE}. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The outer input pins are unaffected by the mode of operation used.

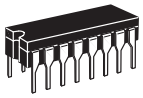
The MC10129 is especially useful in interface applications for central processors, mini–computers, and peripheral equipment.

- P_D = 750 mW typ/pkg (No Load)
- t_{pd} = 10 ns typ
- V_{CC} Max = 7.0 Vdc

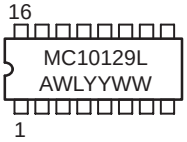
ON Semiconductor

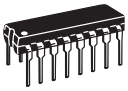
http://onsemi.com

MARKING DIAGRAMS

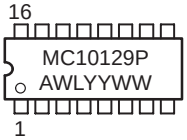


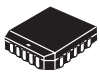
CDIP–16
L SUFFIX
CASE 620



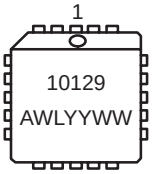


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

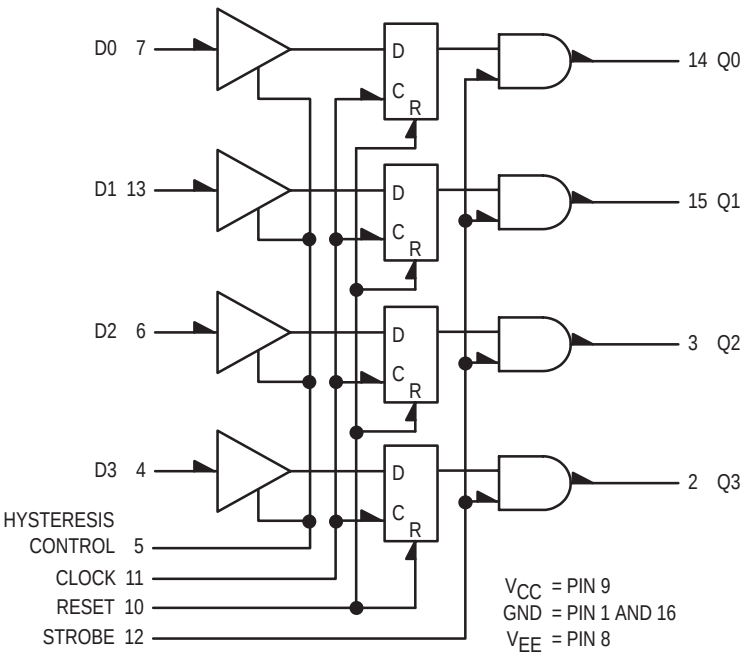


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

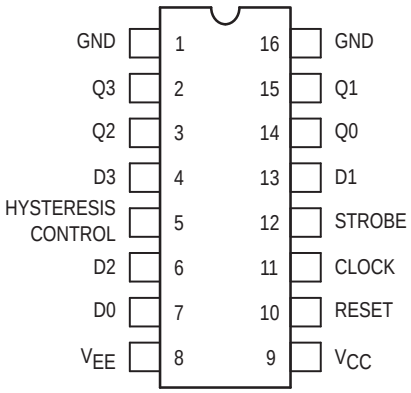
ORDERING INFORMATION

Device	Package	Shipping
MC10129L	CDIP–16	25 Units / Rail
MC10129P	PDIP–16	25 Units / Rail
MC10129FN	PLCC–20	46 Units / Rail

LOGIC DIAGRAM



PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

TRUTH TABLE

D	C	STROBE	RESET	Q_{n+1}
X	X	L	X	L
X	H	X	H	L
L	L	H	X	L
X	H	H	L	Q_n
H	L	H	X	H

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Negative Power Supply Drain Current	I_E	8 8		167 189			152 172		167 189	mAdc
Positive Power Supply Drain Current	I_{CC}	9		8.0			8.0		8.0	mAdc
Input Current	I_{inH}	4 6 7 10 11 12 13		150 150 150 720 390 390 150			95 95 95 450 245 245 95		95 95 95 450 245 245 95	µAdc
	I_{CBO} (1.)	4 6 7 13		1.5 1.5 1.5	 –1.0		–1.0 –1.0 –1.0		1.0 1.0 1.0	µAdc
	I_{inL}	10 11 12	0.5 0.5 0.5		0.5 0.5 0.5			0.3 0.3 0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3 2 3	–1.060 –1.060 –1.060 –1.060	–0.890 –0.890 –0.890 –0.890	–0.960 –0.960 –0.960 –0.960		–0.810 –0.810 –0.810 –0.810	–0.890 –0.890 –0.890 –0.890	–0.700 –0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 2 3	–1.890 –1.890 –1.890 –1.890	–1.675 –1.675 –1.675 –1.675	–1.850 –1.850 –1.850 –1.850		–1.650 –1.650 –1.650 –1.650	–1.825 –1.825 –1.825 –1.825	–1.615 –1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 (2.) 2 2 2 2 (3.) 2 (4.)	–1.080 –1.080 –1.080 –1.080 –1.080 –1.080		–0.980 –0.980 –0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 (2.) 2 2 (2.) 2 2 (3.) 2 (4.)		–1.655 –1.655 –1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595 –1.595 –1.595	Vdc
Switching Times Propagation Delay										ns
Data Input	t_{7+14+} t_{7-14-}	14 14	3.7 3.7	15 15	3.7 3.7	10 10	15 15	3.7 3.7	30 40	
Clock Input	t_{11-14+} t_{11-14-}	14 14	2.7 2.7	11 11	2.7 2.7	5.0 5.0	9.0 9.0	2.7 2.7	11 11	
Strobe Input	t_{12+14+} t_{12-14-}	14 14	1.6 1.6	8.0 8.0	1.6 1.6	4.0 4.0	7.0 7.0	1.6 1.6	8.0 8.0	
Reset Input	t_{10+14-}	14	2.0	8.0	2.0	5.0	6.5	2.0	8.0	
Hysteresis Mode	t_{7+14+} t_{7-14-}	14 14	6.6 3.7	30 17	6.7 3.7	18 10	25 15	6.6 3.7	30 40	
Setup Time	t_{setup}	14	30		2.7	15		30		
Hold Time	t_{hold}	14	0		–2.0	15		–2.0		
Rise Time	t+	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0	
Fall Time	t–	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0	

1. Pin 5 to V_{EE}, V_{IL} to Data input one at a time.
2. Output latched to logic high state prior to test. V_{IHA}', V_{ILA}' are standard logic 1 and logic 0 MTTL threshold voltages. V_{IHA}'', V_{ILA}'', V_{IHA}''' and V_{ILA}''' are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 3.
3. Input level on data input taken from +0.4V up to voltage level given.
4. Input level on data input taken from +4.0V down to voltage level given.
5. Operation and limits shown also apply for V_{CC} = +6.0V.

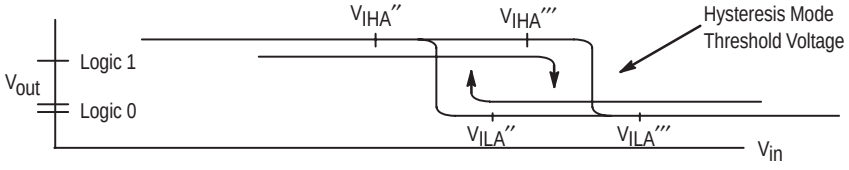


Figure 1. Hysteresis Mode Threshold Voltage

ELECTRICAL CHARACTERISTICS

			TEST VOLTAGE VALUES (Volts)								
			MECL 10,000 INPUT LEVELS				TTL INPUT LEVELS (6.)				
@ Test Temperature			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	
–30°C			–0.890	–1.890	–1.155	–1.500	3.000	0.400	2.000	0.800	
+25°C			–0.810	–1.850	–1.105	–1.475	3.000	0.400	2.000	0.800	
+85°C			–0.700	–1.825	–1.035	–1.440	3.000	0.400	2.000	0.800	
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW								
Characteristic	Symbol	Pin Under Test	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	Gnd
Negative Power Supply Drain Current	I_E	8 8	11 11	12 12							1,5,16 1,16
Positive Power Supply Drain Current	I_{CC}	9						4,6,7,13			1,16
Input Current	I_{inH}	4 6 7 10 11 12 13	 10,11 11 12 				4 6 7 13				1,16 1,16 1,16 1,16 1,16 1,16 1,16
	I_{CBO} (1.)	4 6 7 13						4 6 7 13			1,16 1,16 1,16 1,16
	I_{inL}	10 11 12		10 11 12							1,16 1,16 1,16
Output Voltage Logic 1	V_{OH}	2 3 2 3	12 12 12 12	10,11 10,11 10,11 10,11			4 6 4 6				1,16 1,16 1,5,16 1,5,16
Output Voltage Logic 0	V_{OL}	2 3 2 3	12 12 12 12	10,11 10,11 10,11 10,11				4 6 4 6			1,16 1,16 1,5,16 1,5,16
Threshold Voltage Logic 1	V_{OHA}	2 (2.) 2 2 2 2 (3.) 2 (4.)	11,12 10,12 12 12 12	 10,11 10,11 10,11 10,11	 12 	10 11 	4 4 4 	 	 4 	 	1,16 1,16 1,16 1,16 1,5,16 1,5,16
Threshold Voltage Logic 0	V_{OLA}	2 (2.) 2 2 (2.) 2 2 (3.) 2 (4.)	11,12 10,12 12 12 12	 10,11 10,11 10,11 10,11	10 11 	 12 	4 4 4 	 	 	 4 	1,16 1,16 1,16 1,16 1,5,16 1,5,16
Switching Times Propagation Delay			+1.11V	+0.31V	Pulse In	Pulse Out	+5.0V	+2.40V	Figure		+2.0V
Data Input	t_{7+14+} t_{7-14-}	14 14	12 12	10,11 10,11	7 7	14 14			Figure 3 Figure 3		1,16 1,16
Clock Input	t_{11-14+} t_{11-14-}	14 14	12 12	10 10	7,11 7,11	14 14			Figure 6 Figure 6		1,16 1,16
Strobe Input	t_{12+14+} t_{12-14-}	14 14		10,11 10,11	12 12	14 14	7 7		Figure 4 Figure 4		1,16 1,16
Reset Input	t_{10+14-}	14	12		10,11	14	7	7	Figure 5		1,16
Hysteresis Mode	t_{7+14+} t_{7-14-}	14 14	12 12	10,11 10,11	7 7	14 14			Figure 3 Figure 3		1,5,16 1,5,16
Setup Time	t_{setup}	14	12	10	7,11	14			Figure 7		1,16
Hold Time	t_{hold}	14	12	10	7,11	14			Figure 7		1,16
Rise Time	t+	14	12	10,11	7	14			Figure 3		1,16
Fall Time	t–	14	12	10,11	7	14			Figure 3		1,16

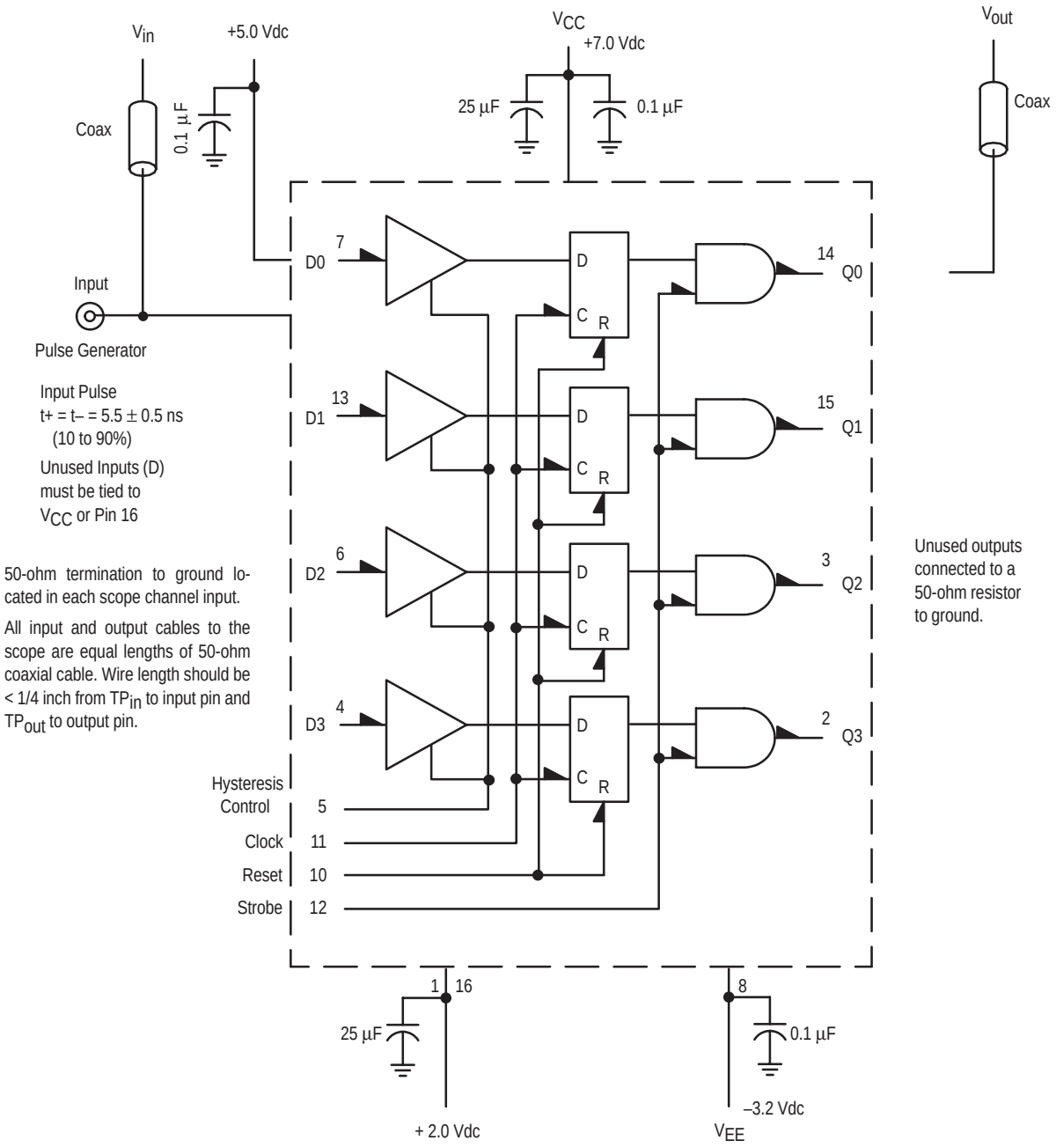
1. Pin 5 to V_{EE}, V_{IL} to Data input one at a time.
2. Output latched to logic high state prior to test. $V_{IHA'}$, $V_{ILA'}$ are standard logic 1 and logic 0 MTTL threshold voltages. $V_{IHA''}$, $V_{ILA''}$, $V_{IHA'''}$ and $V_{ILA'''}$ are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 3.
3. Input level on data input taken from +0.4V up to voltage level given.
4. Input level on data input taken from +4.0V down to voltage level given.
5. Operation and limits shown also apply for V_{CC} = +6.0V.
6. When testing, choose either TTL or IBM input levels.

ELECTRICAL CHARACTERISTICS

@ Test Temperature			TEST VOLTAGE VALUES (Volts)										
			IBM INPUT LEVELS (6.)				HYSTERESIS MODE						
			V_{IH}	V_{IL}	V_{IHA}'	V_{ILA}'	V_{IHA}''	V_{ILA}''	V_{IHA}'''	V_{ILA}'''	V_{CC} (5.)	V_{EE}	
–30°C			3.11	0.150			2.90	2.00	2.20	1.30	+5.0	–5.2	
+25°C			3.11	0.150	1.700	0.70	2.60	1.70	1.90	1.00	+5.0	–5.2	
+85°C			3.11	0.150			2.30	1.40	1.60	0.70	+5.0	–5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW										Gnd
			V_{IH}	V_{IL}	V_{IHA}'	V_{ILA}'	V_{IHA}''	V_{ILA}''	V_{IHA}'''	V_{ILA}'''	V_{CC} (5.)	V_{EE}	
Negative Power Supply Drain Current	I_E	8 8									9 9	8 5,8	1,5,16 1,16
Positive Power Supply Drain Current	I_{CC}	9		4,6, 7,13							9 9	5,8 5,8	1,16 1,16
Input Current	I_{inH}	4 6 7 10 11 12 13	4 6 7 13								9 9 9 9 9 9 9	8 8 8 8 8 8 8	1,16 1,16 1,16 1,16 1,16 1,16 1,16
	I_{CBO} (1.)	4 6 7 13		4 6 7 13							9 9 9 9	8 8 8 8	1,16 1,16 1,16 1,16
	I_{inL}	10 11 12									9 9 9	8 8 8	1,16 1,16 1,16
Output Voltage Logic 1	V_{OH}	2 3 2 3	4 6 4 6								9 9 9 9	5,8 5,8 8 8	1,16 1,16 1,5,16 1,5,16
Output Voltage Logic 0	V_{OL}	2 3 2 3		4 6 4 6							9 9 9 9	5,8 5,8 8 8	1,16 1,16 1,5,16 1,5,16
Threshold Voltage Logic 1	V_{OHA}	2 (2.) 2 2 2 2 (3.) 2 (4.)	4 4 4		4		4		4		9 9 9 9 9 9	5,8 5,8 5,8 5,8 8 8	1,16 1,16 1,16 1,16 1,5,16 1,5,16
Threshold Voltage Logic 0	V_{OLA}	2 (2.) 2 2 (2.) 2 2 (3.) 2 (4.)	4 4 4			4		4		4	9 9 9 9 9 9	5,8 5,8 5,8 5,8 8 8	1,16 1,16 1,16 1,16 1,5,16 1,5,16
Switching Times Propagation Delay			+5.0V	+2.40V	Figure						+7.0V	–3.2V	+2.0V
Data Input	t_{7+14+} t_{7-14-}	14 14			Figure 3 Figure 3						9 9	5,8 5,8	1,16 1,16
Clock Input	t_{11-14+} t_{11-14-}	14 14			Figure 6 Figure 6						9 9	5,8 5,8	1,16 1,16
Strobe Input	t_{12+14+} t_{12-14-}	14 14	7 7		Figure 4 Figure 4						9 9	5,8 5,8	1,16 1,16
Reset Input	t_{10+14-}	14	7		Figure 5						9	5,8	1,16
Hysteresis Mode	t_{7+14+} t_{7-14-}	14 14			Figure 3 Figure 3						9 9	8 8	1,5,16 1,5,16
Setup Time	t_{setup}	14			Figure 7						9	5,8	1,16
Hold Time	t_{hold}	14			Figure 7						9	5,8	1,16
Rise Time	t+	14			Figure 3						9	5,8	1,16
Fall Time	t–	14			Figure 3						9	5,8	1,16

1. Pin 5 to V_{EE}, V_{IL} to Data input one at a time.
2. Output latched to logic high state prior to test. V_{IHA}', V_{ILA}' are standard logic 1 and logic 0 MTTL threshold voltages. V_{IHA}'', V_{ILA}'', V_{IHA}''' and V_{ILA}''' are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 3.
3. Input level on data input taken from +0.4V up to voltage level given.
4. Input level on data input taken from +4.0V down to voltage level given.
5. Operation and limits shown also apply for V_{CC} = +6.0V.
6. When testing, choose either TTL or IBM input levels.

Figure 2. SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE: All power supplies and logic levels are shifted 2 volts positive.

Figure 3 – DATA to OUTPUT
(Clock and Reset are low, Strobe is high)

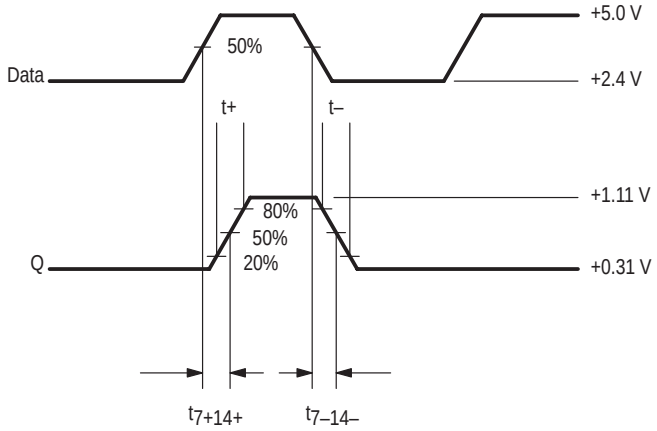


Figure 4 – STROBE to OUTPUT
(Data is high, Clock and Reset are low)

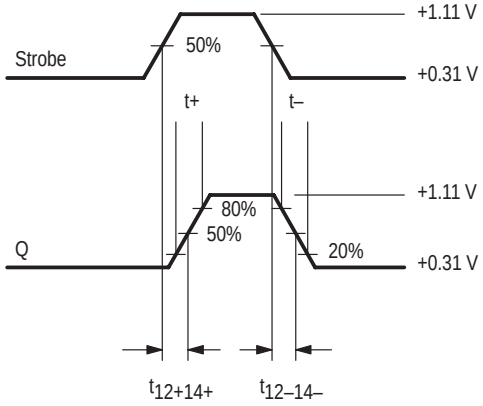


Figure 5 – RESET to OUTPUT
(Data and Strobe are high)

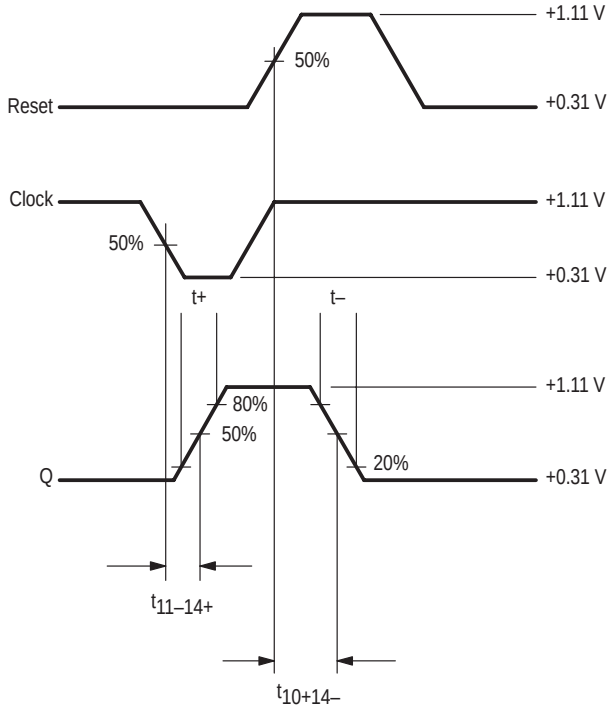


Figure 6 – CLOCK to OUTPUT
(Reset is low, Strobe is high)

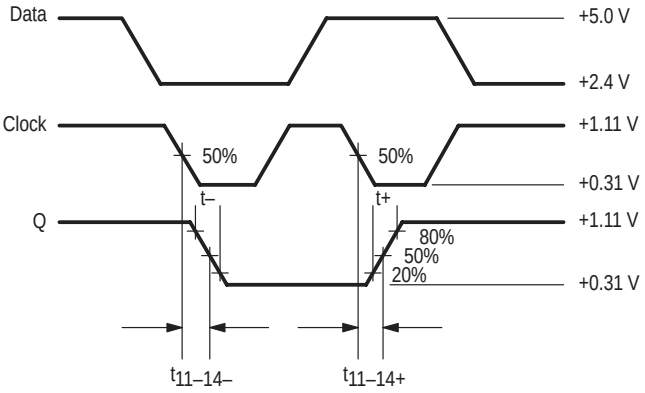
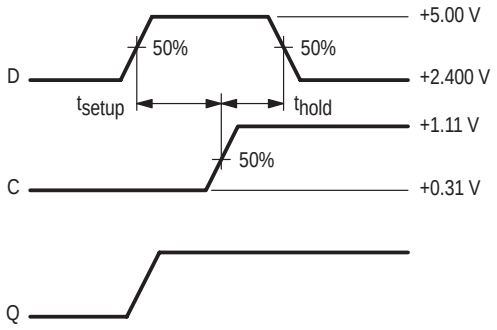
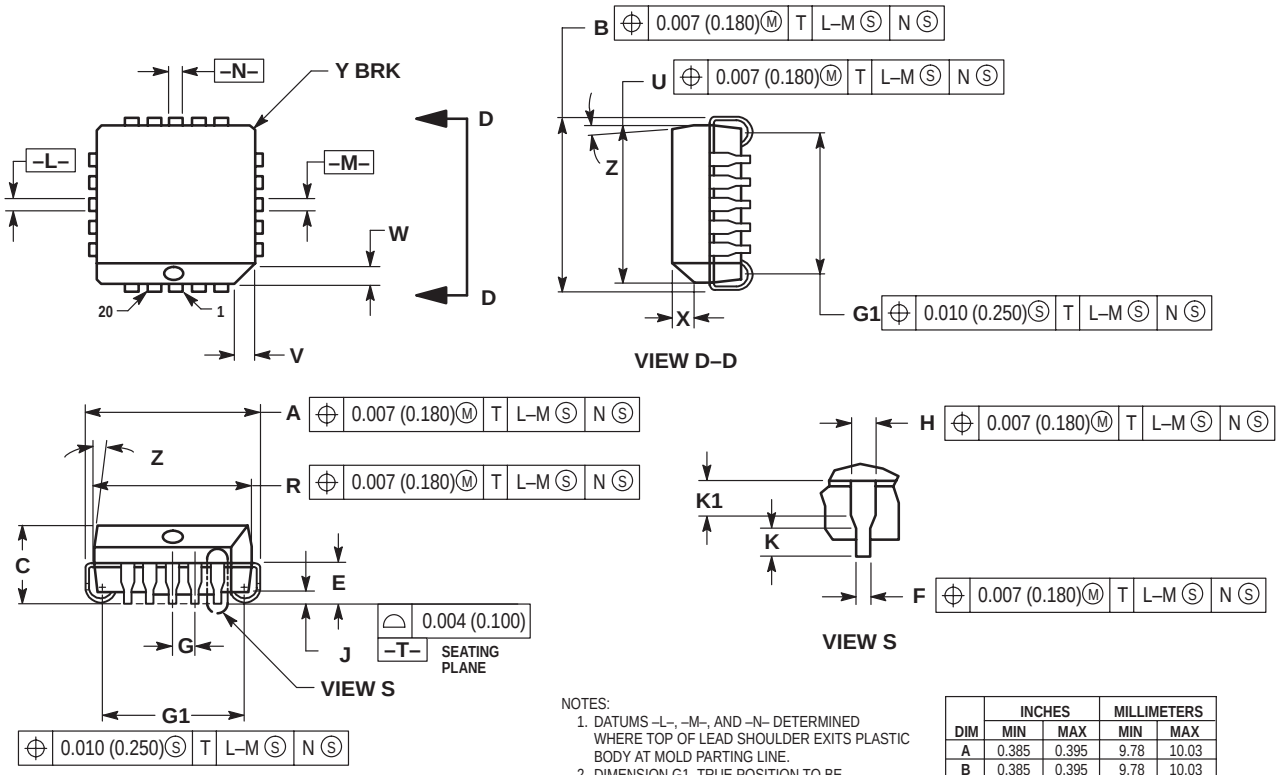


Figure 7 – $T_{SET\ UP}$ AND T_{HOLD} WAVEFORMS



PACKAGE DIMENSIONS

PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C

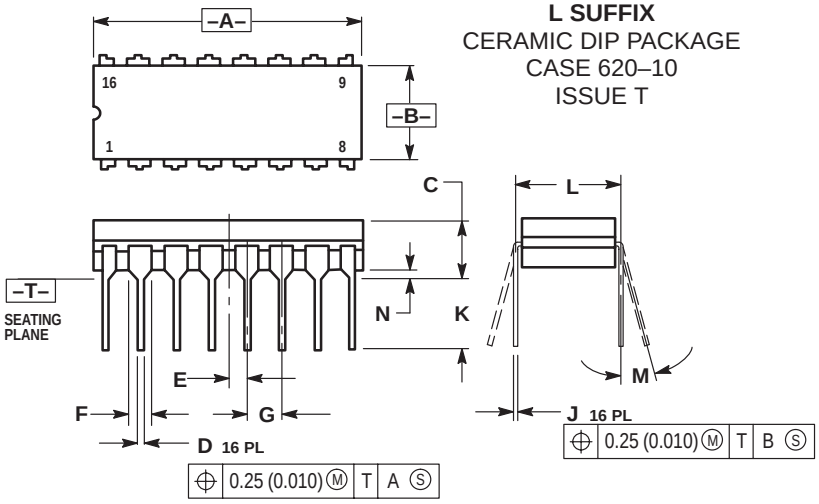


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

PACKAGE DIMENSIONS

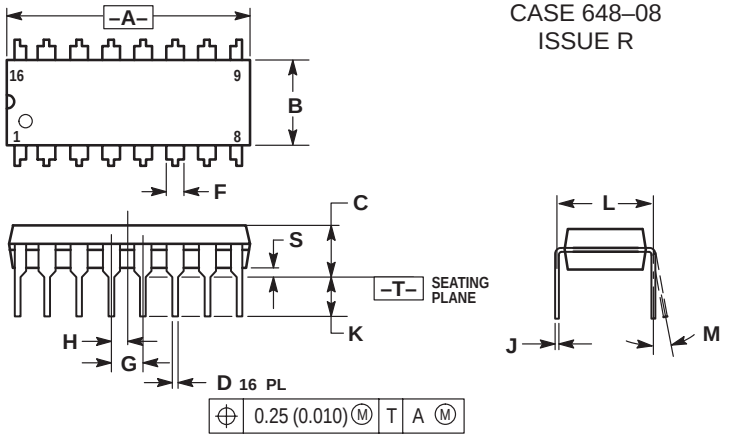
CDIP–16
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

Notes

Notes

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