

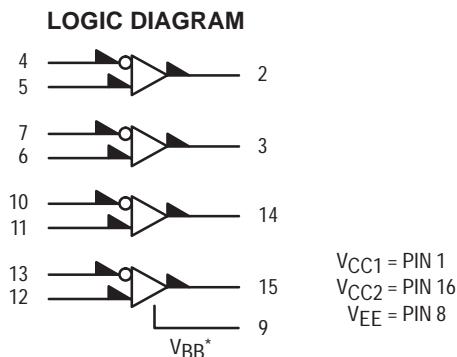
# MC10115

## Quad Line Receiver

The MC10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply ( $V_{BB}$ ) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

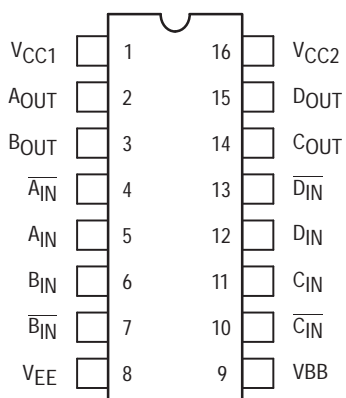
Active current sources provide the MC10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to  $V_{BB}$  (pin 9) to prevent upsetting the current source bias network.

- $P_D = 110 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 2.0 \text{ ns typ}$
- $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$



\* $V_{BB}$  to be used to supply bias to the MC10115 only and bypassed (when used) with  $0.01 \mu\text{F}$  to  $0.1 \mu\text{F}$  capacitor to ground (0 V).  $V_{BB}$  can source  $< 1.0 \text{ mA}$ .  
 When the input pin with the bubble goes positive, the output goes negative.

### DIP PIN ASSIGNMENT



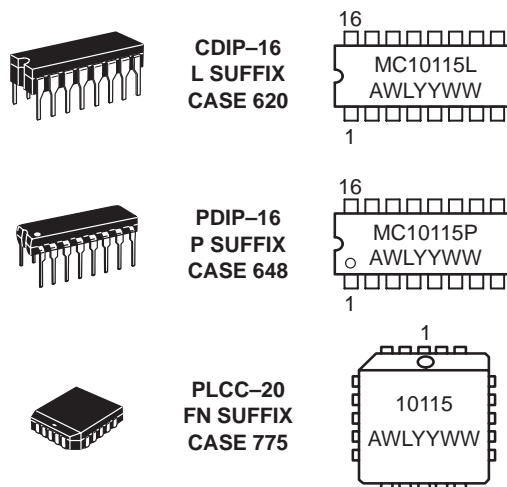
Pin assignment is for Dual-in-Line Package.  
 For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



**ON Semiconductor**

<http://onsemi.com>

### MARKING DIAGRAMS



A = Assembly Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC10115L	CDIP-16	25 Units / Rail
MC10115P	PDIP-16	25 Units / Rail
MC10115FN	PLCC-20	46 Units / Rail

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I <sub>E</sub>	8		29			26		29	mAdc
Input Current	I <sub>inH</sub>	4		150			95		95	μAdc
	I <sub>CBO</sub>	4		1.5			1.0		1.0	μAdc
Output Voltage      Logic 1	V <sub>OH</sub>	2	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
Output Voltage      Logic 0	V <sub>OL</sub>	2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc
Threshold Voltage    Logic 1	V <sub>OHA</sub>	2	−1.080		−0.980			−0.910		Vdc
Threshold Voltage    Logic 0	V <sub>OLA</sub>	2		−1.655			−1.630		−1.595	Vdc
Reference Voltage	V <sub>BB</sub>	9	1.420	1.280	−1.350		−1.230	1.295	−1.150	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t <sub>4−2+</sub>	2	1.0	3.1	1.0		2.9	1.0	3.3	
	t <sub>4+2−</sub>	2	1.0	3.1	1.0		2.9	1.0	3.3	
Rise Time            (20 to 80%)	t <sub>2+</sub>	2	1.1	3.6	1.1		3.3	1.1	3.7	
Fall Time            (20 to 80%)	t <sub>2−</sub>	2	1.1	3.6	1.1		3.3	1.1	3.7	

## ELECTRICAL CHARACTERISTICS (continued)

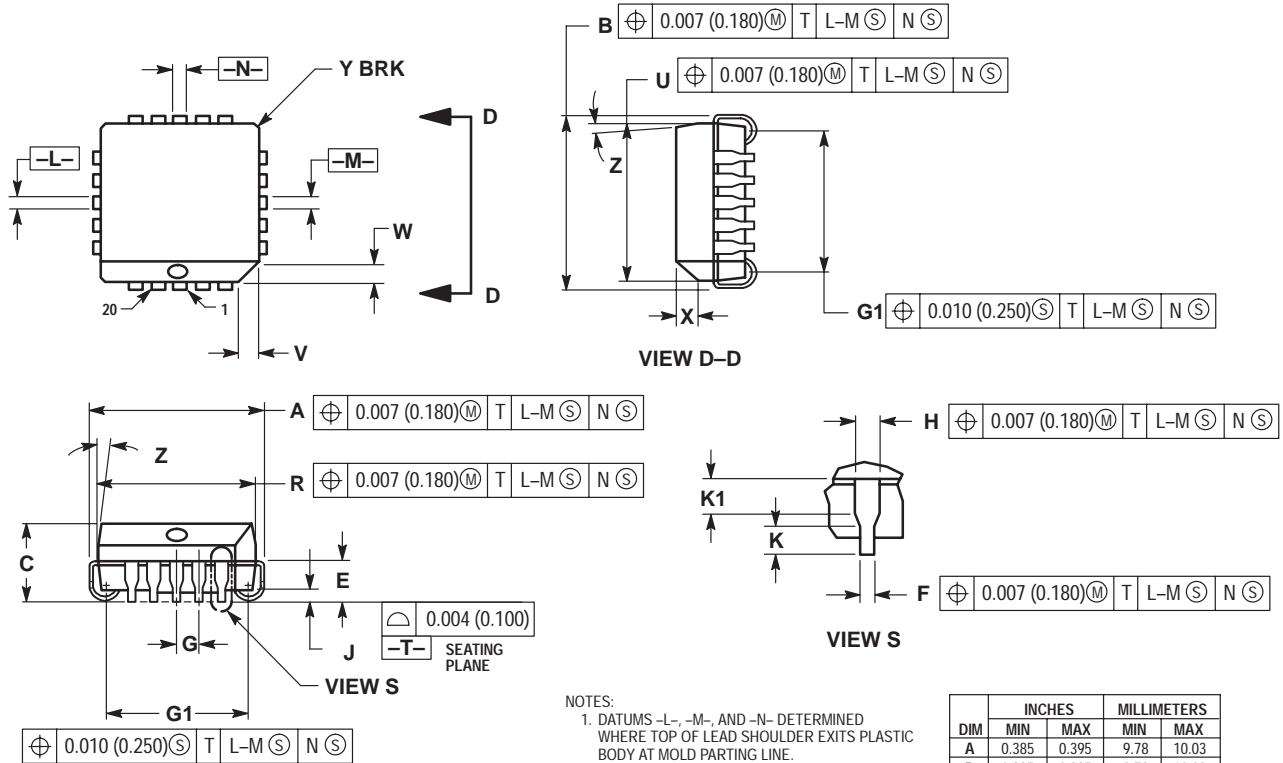
@ Test Temperature			TEST VOLTAGE VALUES (Volts)						(V <sub>CC</sub> ) Gnd	
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAm</sub> ax	V <sub>BB</sub>	V <sub>EE</sub>		
			-30°C	-0.890	-1.890	-1.205	-1.500	From Pin 9		-5.2
			+25°C	-0.810	-1.850	-1.105	-1.475			-5.2
			+85°C	-0.700	-1.825	-1.035	-1.440			-5.2
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						(V <sub>CC</sub> ) Gnd	
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAm</sub> ax	V <sub>BB</sub>	V <sub>EE</sub>		
Power Supply Drain Current	I <sub>E</sub>	8		4,7,10,13			5,6,11,12	8	1, 16	
Input Current	I <sub>inH</sub>	4	4	7,10,13			5,6,11,12	8	1, 16	
	I <sub>CBO</sub>	4		7,10,13			5,6,11,12	8,4	1, 16	
Output Voltage      Logic 1	V <sub>OH</sub>	2	7,10,13	4			5,6,11,12	8	1, 16	
Output Voltage      Logic 0	V <sub>OL</sub>	2	4	7,10,13			5,6,11,12	8	1, 16	
Threshold Voltage    Logic 1	V <sub>OHA</sub>	2		7,10,13		4	5,6,11,12	8	1, 16	
Threshold Voltage    Logic 0	V <sub>OLA</sub>	2		7,10,13	4		5,6,11,12	8	1, 16	
Reference Voltage	V <sub>BB</sub>	9					5,6,11,12	8	1, 16	
Switching Times      (50Ω Load)			Pulse In		Pulse Out			-3.2 V	+2.0 V	
Propagation Delay	t <sub>4-2+</sub>	2	4		2		5,6,11,12	8	1, 16	
	t <sub>4+2-</sub>	2	4		2		5,6,11,12	8	1, 16	
Rise Time              (20 to 80%)	t <sub>2+</sub>	2	4		2		5,6,11,12	8	1, 16	
Fall Time               (20 to 80%)	t <sub>2-</sub>	2	4		2		5,6,11,12	8	1, 16	

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

# MC10115

## PACKAGE DIMENSIONS

PLCC-20  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



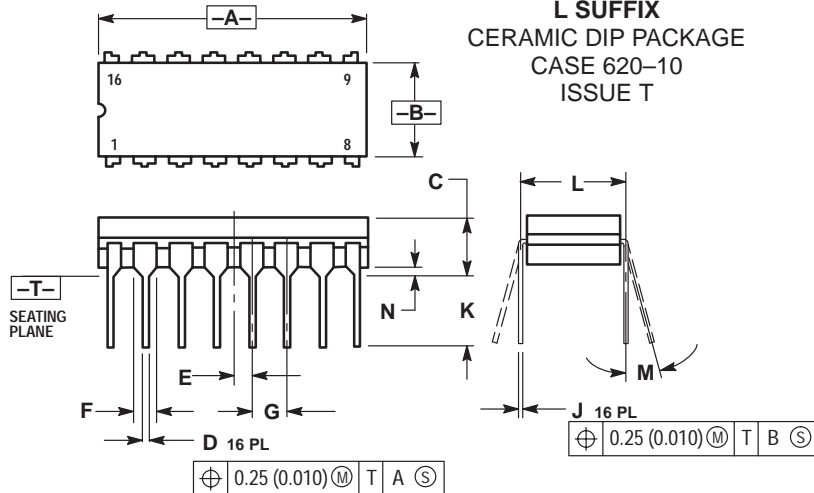
### NOTES:

1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

# MC10115

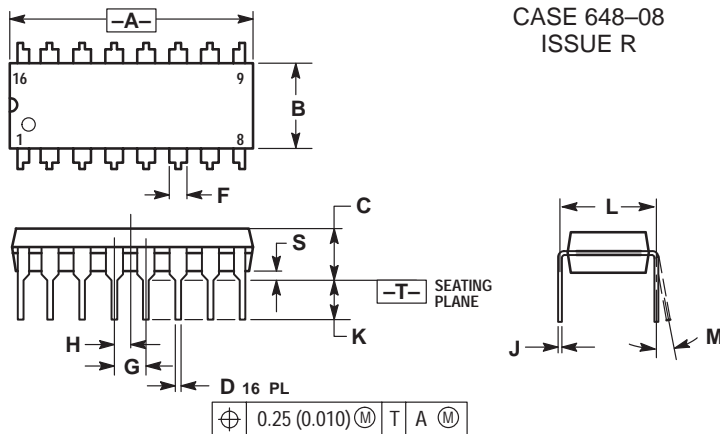
## CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

## PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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