

# MC10114

## Triple Line Receiver

The MC10114 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

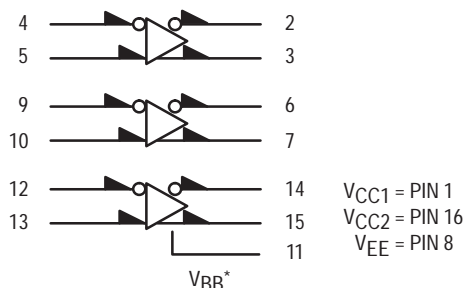
Another feature of the MC10114 is that the OR outputs go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumentation systems. The MC10114 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A  $V_{BB}$  reference is provided which is useful in making the MC10114 a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary. See MECL Design Handbook (HB205) pages 226 and 228.

- $P_D = 145 \text{ mW typ/pkg}$
- $t_{pd} = 2.4 \text{ ns typ (Single Ended Input)}$
- $t_{pd} = 2.0 \text{ ns typ (Differential Input)}$
- $t_r, t_f = 2.1 \text{ ns typ (20\%–80\%)}$

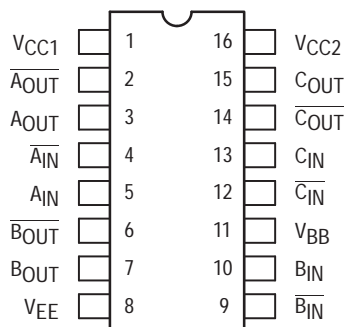
### LOGIC DIAGRAM



\* $V_{BB}$  to be used to supply bias to the MC10114 only and bypassed (when used) with  $0.01 \mu\text{F}$  to  $0.1 \mu\text{F}$  capacitor to ground (0 V).  $V_{BB}$  can source  $< 1.0 \text{ mA}$ .

When the input pin with the bubble goes positive, its respective output pin with bubble goes positive.

### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.

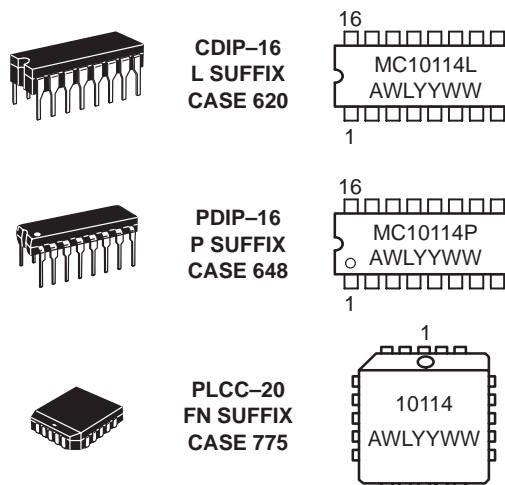
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



ON Semiconductor

<http://onsemi.com>

### MARKING DIAGRAMS



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC10114L	CDIP-16	25 Units / Rail
MC10114P	PDIP-16	25 Units / Rail
MC10114FN	PLCC-20	46 Units / Rail

# MC10114

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I <sub>E</sub>	8		39		28	35		39	mAdc
Input Current	I <sub>inH</sub>	4		70			45		45	μAdc
	I <sub>CBO</sub>	4		1.5			1.0		1.0	μAdc
Output Voltage      Logic 1	V <sub>OH</sub>	2 3	−1.060 −1.060	−0.890 −0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
Output Voltage      Logic 0	V <sub>OL</sub>	2 3	−1.890 −1.890	−1.675 −1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Threshold Voltage    Logic 1	V <sub>OHA</sub>	2 3	−1.080 −1.080		−0.980 −0.980			−0.910 −0.910		Vdc
Threshold Voltage    Logic 0	V <sub>OLA</sub>	2 3		−1.655 −1.655			−1.630 −1.630		−1.595 −1.595	Vdc
Reference Voltage	V <sub>BB</sub>	11	−1.420	−1.280	−1.350		−1.230	−1.295	−1.150	Vdc
Common Mode Rejection Test	V <sub>OH</sub>	2 3	−1.060 −1.060	−0.890 −0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
	V <sub>OL</sub>	2 3	−1.890 −1.890	−1.675 −1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Switching Times (50Ω Load)			Min	Max	Min	Typ	Max	Min	Max	ns
Propagation Delay	t <sub>4+2+</sub>	2	1.0	4.4	1.0	2.4	4.0	0.9	4.3	
	t <sub>4−2−</sub>	2	1.0	4.4	1.0	2.4	4.0	0.9	4.3	
	t <sub>4+3−</sub>	3	1.0	4.4	1.0	2.4	4.0	0.9	4.3	
	t <sub>4−3+</sub>	3	1.0	4.4	1.0	2.4	4.0	0.9	4.3	
Rise Time            (20 to 80%)	t <sub>2+</sub>	2	1.5	3.8	1.5	2.1	3.5	1.5	3.7	
	t <sub>3+</sub>	3	1.5	3.8	1.5	2.1	3.5	1.5	3.7	
Fall Time            (20 to 80%)	t <sub>2−</sub>	2	1.5	3.8	1.5	2.1	3.5	1.5	3.7	
	t <sub>3−</sub>	3	1.5	3.8	1.5	2.1	3.5	1.5	3.7	

# MC10114

## ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					Unit
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>BB</sub>	
			−30°C	−0.890	−1.890	−1.205	−1.500	
			+25°C	−0.810	−1.850	−1.105	−1.475	
			+85°C	−0.700	−1.825	−1.035	−1.440	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					Unit
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>BB</sub>	
Power Supply Drain Current	I <sub>E</sub>	8		4, 9, 12			5, 10, 13	mAdc
Input Current	I <sub>inH</sub>	4	4	9, 12			5, 10, 13	μAdc
	I <sub>inL</sub>	4		9, 12			5, 10, 13	μAdc
Output Voltage Logic 1	V <sub>OH</sub>	2	4	9, 12			5, 10, 13	Vdc
		3	9, 12	4			5, 10, 13	
Output Voltage Logic 0	V <sub>OL</sub>	2	9, 12	4			5, 10, 13	Vdc
		3	4	9, 12			5, 10, 13	
Threshold Voltage Logic 1	V <sub>OHA</sub>	2		9, 12	4		5, 10, 13	Vdc
		3	9, 12			4	5, 10, 13	
Threshold Voltage Logic 0	V <sub>OLA</sub>	2		9, 12		4	5, 10, 13	Vdc
		3		9, 12	4		5, 10, 13	
Reference Voltage	V <sub>BB</sub>	11					5, 10, 13	Vdc
Common Mode Rejection Test	V <sub>OH</sub>	2						Vdc
		3						
	V <sub>OL</sub>	2						Vdc
		3						
Switching Times (50Ω Load)					Pulse In	Pulse Out		ns
Propagation Delay	t <sub>4+2+</sub>	2			4	2	5, 10, 13	
	t <sub>4−2−</sub>	2			4	2	5, 10, 13	
	t <sub>4+3−</sub>	3			4	3	5, 10, 13	
	t <sub>4−3+</sub>	3			4	3	5, 10, 13	
Rise Time (20 to 80%)	t <sub>2+</sub>	2			4	2	5, 10, 13	
	t <sub>3+</sub>	3			4	3	5, 10, 13	
Fall Time (20 to 80%)	t <sub>2−</sub>	2			4	2	5, 10, 13	
	t <sub>3−</sub>	3			4	3	5, 10, 13	

# MC10114

## ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					(V <sub>CC</sub> ) Gnd
			V <sub>IHH</sub> *	V <sub>ILH</sub> *	V <sub>IHL</sub> *	V <sub>ILL</sub> *	V <sub>EE</sub>	
			−30°C	+0.110	−0.890	−1.890	−2.890	−5.2
			+25°C	+0.190	−0.850	−1.810	−2.850	−5.2
			+85°C	+0.300	−0.825	−1.700	−2.825	−5.2
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V <sub>CC</sub> ) Gnd
			V <sub>IHH</sub> *	V <sub>ILH</sub> *	V <sub>IHL</sub> *	V <sub>ILL</sub> *	V <sub>EE</sub>	
Power Supply Drain Current	I <sub>E</sub>	8					8	1, 16
Input Current	I <sub>inH</sub>	4					8	1, 16
	I <sub>inL</sub>	4					8, 4	1, 16
Output Voltage Logic 1	V <sub>OH</sub>	2					8	1, 16
		3					8	1, 16
Output Voltage Logic 0	V <sub>OL</sub>	2					8	1, 16
		3					8	1, 16
Threshold Voltage Logic 1	V <sub>OHA</sub>	2					8	1, 16
		3					8	1, 16
Threshold Voltage Logic 0	V <sub>OLA</sub>	2					8	1, 16
		3					8	1, 16
Reference Voltage	V <sub>BB</sub>	11					8	1, 16
Common Mode Rejection Test	V <sub>OH</sub>	2	4	5	5	4	8	1, 16
		3					8	1, 16
	V <sub>OL</sub>	2		5	5	4	8	1, 16
		3	4	5			8	1, 16
Switching Times (50Ω Load)							−3.2 V	+2.0 V
Propagation Delay	t <sub>4+2+</sub>	2					8	1, 16
	t <sub>4−2−</sub>	2					8	1, 16
	t <sub>4+3−</sub>	3					8	1, 16
	t <sub>4−3+</sub>	3					8	1, 16
Rise Time (20 to 80%)	t <sub>2+</sub>	2					8	1, 16
	t <sub>3+</sub>	3					8	1, 16
Fall Time (20 to 80%)	t <sub>2−</sub>	2					8	1, 16
	t <sub>3−</sub>	3					8	1, 16

\* V<sub>IHH</sub> = Input Logic 1 level shifted positive one volt for common mode rejection tests

V<sub>ILH</sub> = Input Logic 0 level shifted positive one volt for common mode rejection tests

V<sub>IHL</sub> = Input Logic 1 level shifted negative one volt for common mode rejection tests

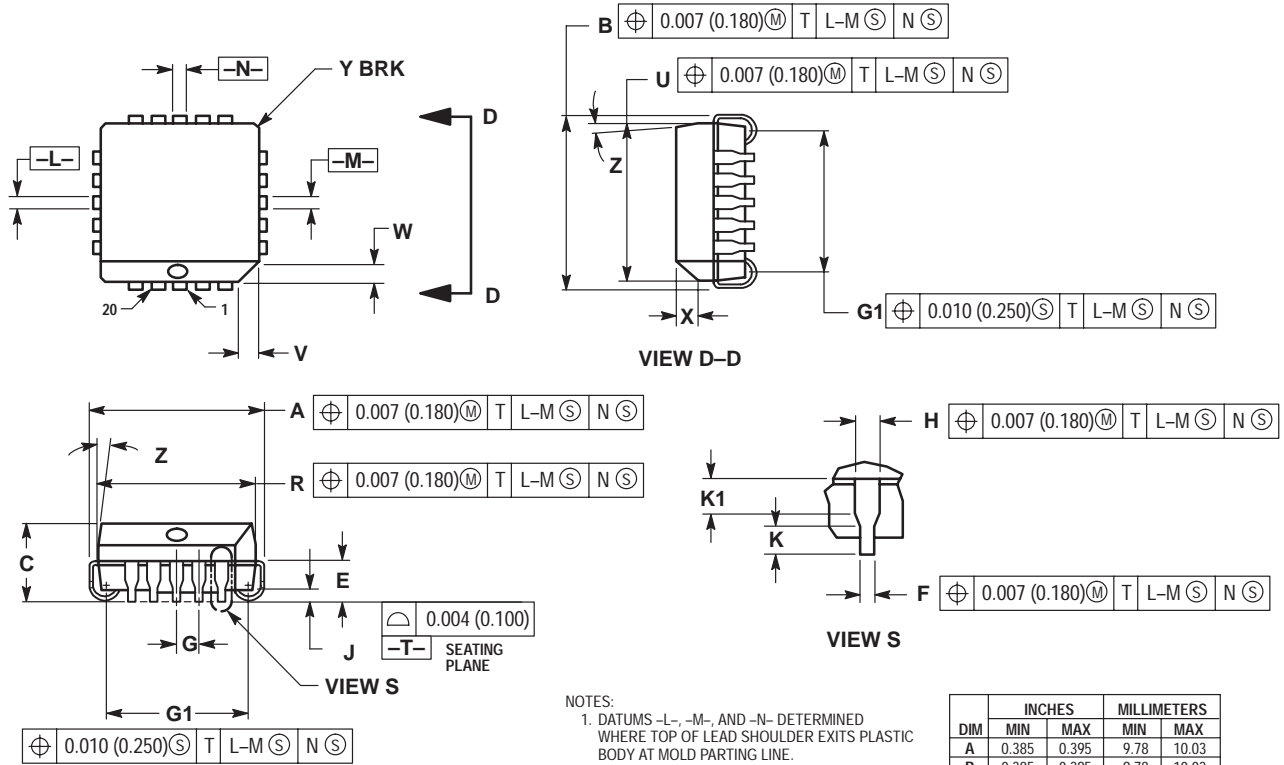
V<sub>ILL</sub> = Input Logic 0 level shifted negative one volt for common mode rejection tests

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

# MC10114

## PACKAGE DIMENSIONS

PLCC-20  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



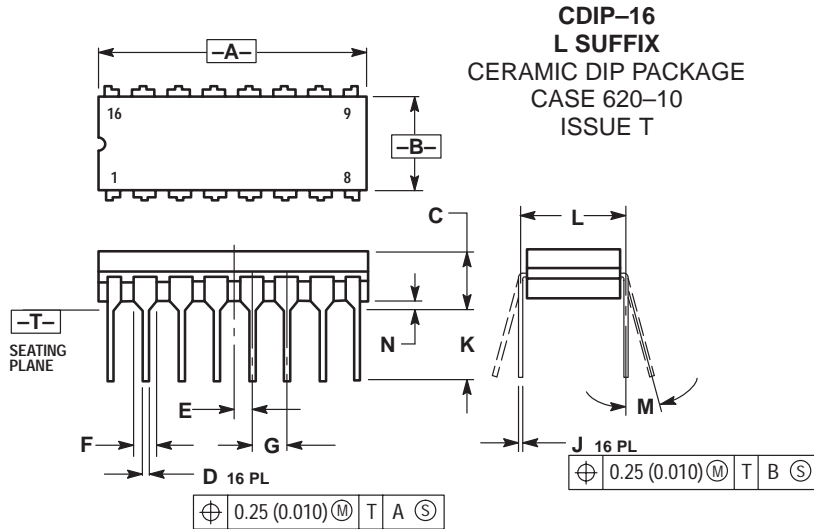
### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

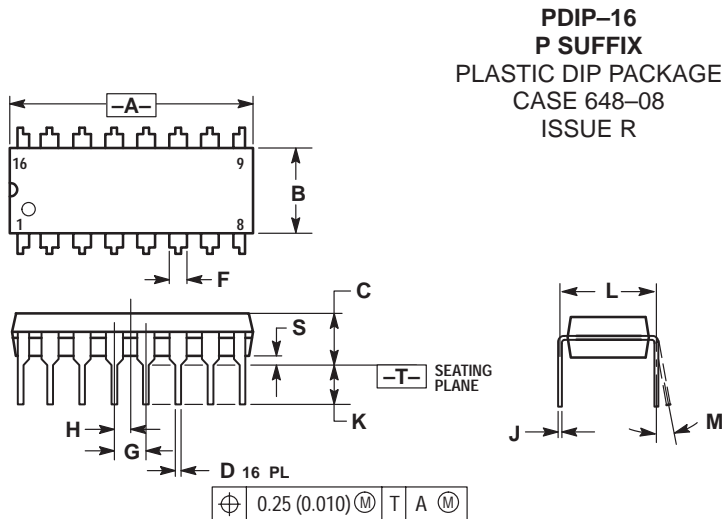
# MC10114

## PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

## **Notes**

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### North America Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

### EUROPE: LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (M–F 2:30pm to 5:00pm Munich Time)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (M–F 2:30pm to 5:00pm Toulouse Time)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (M–F 1:30pm to 5:00pm UK Time)  
**Email:** ONlit@hibbertco.com

### ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong 800-4422-3781  
**Email:** ONlit-asia@hibbertco.com

### JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549  
**Phone:** 81-3-5740-2745  
**Email:** r14525@onsemi.com

**Fax Response Line:** 303-675-2167  
800-344-3810 Toll Free USA/Canada

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.