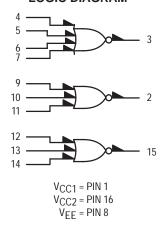
Triple 4-3-3-Input NOR Gate

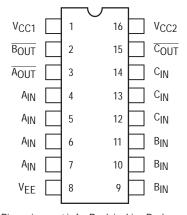
The MC10106 is a triple 4–3–3 input NOR gate.

- $P_D = 30 \text{ mW typ/gate (No Load)}$
- $t_{pd} = 2.0 \text{ ns typ}$
- t_r , $t_f = 2.0$ ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



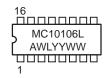
ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS

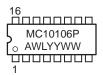


CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot YY = Year

WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping		
MC10106L	CDIP-16	25 Units / Rail		
MC10106P	PDIP-16	25 Units / Rail		
MC10106FN	PLCC-20	46 Units / Rail		

ELECTRICAL CHARACTERISTICS

		Test Limits								
	Pin Under Symbol Test		−30°C		+25°C			+85°C		1 1
Characteristic		0.114.01	Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Drain Current	ΙΕ	8		23		17	21		23	mAdc
Input Current	l _{inH}	4		425			265		265	μAdc
	linL	4	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	VOH	3 2	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc
Output Voltage Logic 0	V _{OL}	3 2	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc
Threshold Voltage Logic 1	Vона	3 2	-1.080 -1.080		-0.980 -0.980			-0.910 -0.910		Vdc
Threshold Voltage Logic 0	V _{OLA}	3 2		-1.655 -1.655			-1.630 -1.630		-1.595 -1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t ₄₊₃₋ t ₄₋₃₊	3 3	1.0 1.0	3.1 3.1	1.0 1.0	2.0 2.0	2.9 2.9	1.0 1.0	3.3 3.3	
Rise Time (20 to 80%)	t ₃₊	3	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
Fall Time (20 to 80%)	t ₃ _	3	1.1	3.6	1.1	2.0	3.3	1.1	3.7	

ELECTRICAL CHARACTERISTICS (continued)

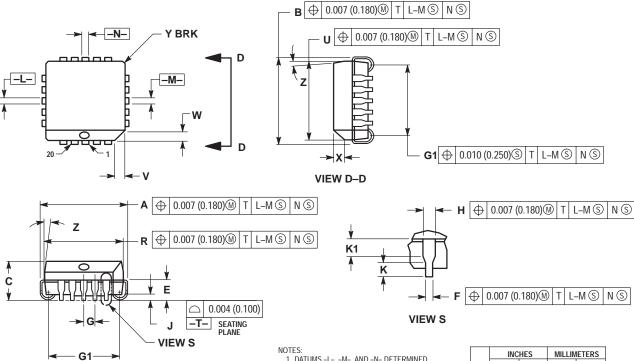
					TEST VO	LTAGE VALU	JES (Volts)		
@ Test Temperature			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}		
	–30°C			-0.890	-1.890	-1.205	-1.500	− 5.2	
			+25°C	-0.810	-1.850	-1.105	-1.475	− 5.2	
			+85°C	-0.700	-1.825	-1.035	-1.440	− 5.2	
	Pin			TEST V	OLTAGE AP	PLIED TO P	INS LISTED I	BELOW	
Characteri	istic	Symbol	Under Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	(V _{CC})
Power Supply Drain (Current	ΙE	8					8	1, 16
Input Current		linH	4	4				8	1, 16
		l _{inL}	4		4			8	1, 16
Output Voltage	Logic 1	Vон	3 2					8 8	1, 16 1, 16
Output Voltage	Logic 0	V _{OL}	3 2	4 9				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	Vона	3 2				4 9	8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V _{OLA}	3 2			4 9		8 8	1, 16 1, 16
Switching Times	(50Ω Load)					Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay		t ₄₊₃₋ t ₄₋₃₊	3 3			4 4	3 3	8 8	1, 16 1, 16
Rise Time	(20 to 80%)	t3+	3			4	3	8	1, 16
Fall Time	(20 to 80%)	t3_	3			4	3	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



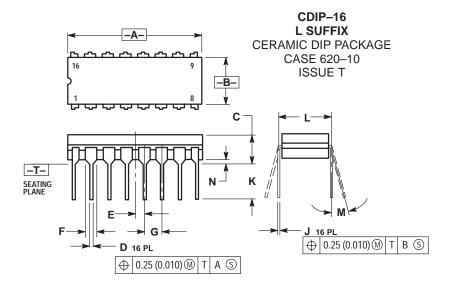
⊕ 0.010 (0.250)⑤ T L-M ⑤ N ⑤

- DATUMS -L-, -M-, AND -N- DETERMINED
 WHERE TOP OF LEAD SHOULDER EXITS PLASTIC WILLY LOVE LEAD STOUDER EXTRA FRAST BODY AT MOLD PARTING LINE.

 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD
- FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
 4. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. 5. CONTROLLING DIMENSION: INCH.
- 6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

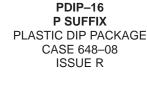
	INC	HES	MILLIN	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX		
Α	0.385	0.395	9.78	10.03		
В	0.385	0.395	9.78	10.03		
С	0.165	0.180	4.20	4.57		
Ε	0.090	0.110	2.29	2.79		
F	0.013	0.019	0.33	0.48		
G	0.050	BSC	1.27	BSC		
Н	0.026	0.032	0.66	0.81		
J	0.020		0.51			
K	0.025		0.64			
R	0.350	0.356	8.89	9.04		
U	0.350	0.356	8.89	9.04		
٧	0.042	0.048	1.07	1.21		
W	0.042	0.048	1.07	1.21		
Х	0.042	0.056	1.07	1.42		
Υ		0.020		0.50		
Z	2°	10 °	2 °	10 °		
G1	0.310	0.330	7.88	8.38		
K1	0.040		1.02			
G1	0.310		7.88			

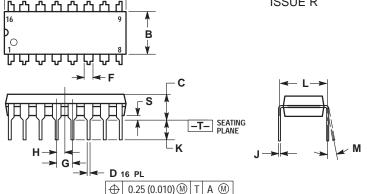


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
 DIMENSION L TO CENTER OF LEAD WHEN
- FORMED PARALLEL.
 DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC

	INC	HES	MILLIMETERS		
DIM	MIN MAX		MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
С		0.200		5.08	
D	0.015	0.020	0.39	0.50	
E	0.050) BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62	BSC	
M	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	ETERS	
DIM	MIN MAX		MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10°	0 °	10 °	
S	0.020	0.040	0.51	1.01	

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