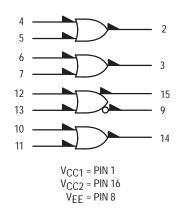
Quad 2-Input OR Gate

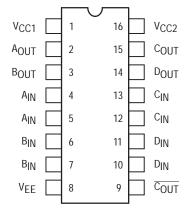
The MC10103 is a quad 2-input OR gate. The MC10103 provides one gate with OR/NOR outputs.

- PD = 25 mW typ/gate (No Load)
- $t_{pd} = 2.0 \text{ ns typ}$
- t_r , $t_f = 2.0$ ns typ (20%-80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



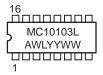
ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS

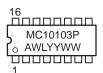


CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot

YY = Year

WW = Work Week

ORDERING INFORMATION

| Device | Package | Shipping | | |
|-----------|---------|-----------------|--|--|
| MC10103L | CDIP-16 | 25 Units / Rail | | |
| MC10103P | PDIP-16 | 25 Units / Rail | | |
| MC10103FN | PLCC-20 | 46 Units / Rail | | |

ELECTRICAL CHARACTERISTICS

| | Test Lin | | | | Test Limits | at Limits | | | | |
|------------------------------------|--|----------------------|------------------|------------------|------------------|------------|------------------|------------------|------------------|------|
| | | Pin Under Test | −30°C | | +25°C | | | +85°C | | 1 |
| Characteristic | Symbol | | Min | Max | Min | Тур | Max | Min | Max | Unit |
| Power Supply Drain Current | ΙE | 8 | | 29 | | 21 | 26 | | 29 | mAdc |
| Input Current | l _{inH} | 4* | | 390 | | | 245 | | 245 | μAdc |
| | linL | 4* | 0.5 | | 0.5 | | | 0.3 | | μAdc |
| Output Voltage Logic 1 | VOH | 2 9 | -1.060 -1.060 | -0.890 -0.890 | -0.960 -0.960 | | -0.810 -0.810 | -0.890 -0.890 | -0.700 -0.700 | Vdc |
| Output Voltage Logic 0 | VOL | 2 9 | -1.890 -1.890 | -1.675 -1.675 | -1.850 -1.850 | | -1.650 -1.650 | -1.825 -1.825 | -1.615 -1.615 | Vdc |
| Threshold Voltage Logic 1 | VOHA | 2 9 | -1.080 -1.080 | | -0.980 -0.980 | | | -0.910 -0.910 | | Vdc |
| Threshold Voltage Logic 0 | VOLA | 2 9 | | -1.655 -1.655 | | | -1.630 -1.630 | | -1.595 -1.595 | Vdc |
| Switching Times (50 Ω Load) | | | | | | | | | | ns |
| Propagation Delay | t ₄₊₂₊ t ₁₂₊₉ | 2 9 | 1.0 1.0 | 3.1 3.1 | 1.0 1.0 | 2.0 2.0 | 2.9 2.9 | 1.0 1.0 | 3.3 3.3 | |
| Rise Time (20 to 80%) | t ₂₊ | 2 | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | |
| Fall Time (20 to 80%) | t ₂ _ | 2 | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | |

^{*} Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS (continued)

| | | | | | TEST VO | LTAGE VALU | JES (Volts) | | |
|----------------------|-------------|--|--------------------|--------------------|--------------------|---------------------|---------------------|--------------|----------------|
| @ Test Temperature | | | V _{IHmax} | V _{ILmin} | VIHAmin | V _{ILAmax} | VEE | | |
| –30°C | | | -0.890 | -1.890 | -1.205 | -1.500 | -5.2 | | |
| | | | +25°C | -0.810 | -1.850 | -1.105 | -1.475 | -5.2 | |
| | | | +85°C | -0.700 | -1.825 | -1.035 | -1.440 | − 5.2 | |
| Pin | | | TEST V | OLTAGE AP | PLIED TO P | INS LISTED | BELOW | | |
| 1 1 - | | | Under Test | V _{IHmax} | V _{ILmin} | V _{IHAmin} | V _{ILAmax} | VEE | (VCC) |
| Power Supply Drain (| Current | ΙE | 8 | | | | | 8 | 1, 16 |
| Input Current | | linH | 4* | 4* | | | | 8 | 1, 16 |
| | | l _{inL} | 4* | | 4* | | | 8 | 1, 16 |
| Output Voltage | Logic 1 | Vон | 2 9 | 4.5 | | | | 8 8 | 1, 16 1, 16 |
| Output Voltage | Logic 0 | VOL | 2 9 | 12, 13 | | | | 8 8 | 1, 16 1, 16 |
| Threshold Voltage | Logic 1 | Vона | 2 9 | | | 4, 5 | 12, 13 | 8 8 | 1, 16 1, 16 |
| Threshold Voltage | Logic 0 | VOLA | 2 9 | | | 12, 13 | 4, 5 | 8 8 | 1, 16 1, 16 |
| Switching Times | (50Ω Load) | | | | | Pulse In | Pulse Out | -3.2 V | +2.0 V |
| Propagation Delay | | t ₄₊₂₊ t ₁₂₊₉ _ | 2 9 | | | 4 12 | 2 9 | 8 8 | 1, 16 1, 16 |
| Rise Time | (20 to 80%) | t ₂₊ | 2 | | | 4 | 2 | 8 | 1, 16 |
| Fall Time | (20 to 80%) | t ₂ _ | 2 | | | 4 | 2 | 8 | 1, 16 |

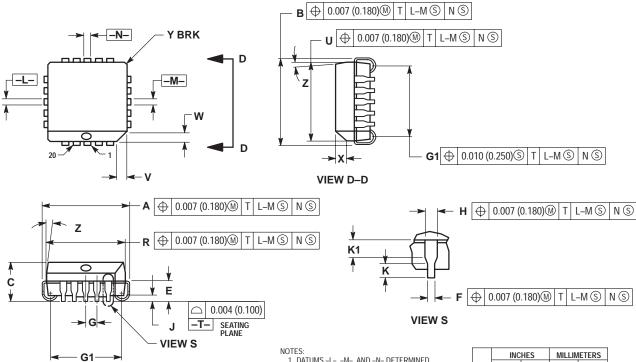
^{*} Individually test each input applying V_{IH} or V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



NOTES:

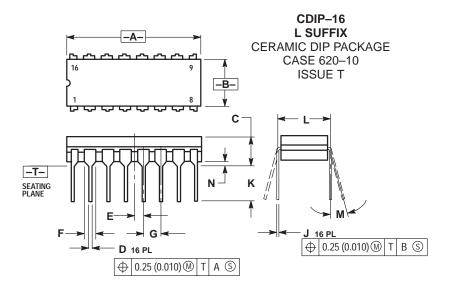
⊕ 0.010 (0.250)⑤ T L-M ⑤ N ⑤

- DATUMS -L-, -M-, AND -N- DETERMINED
 WHERE TOP OF LEAD SHOULDER EXITS PLASTIC WILLY LOVE LEAD STOUDER EXTENSIVE SOLUTION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD
- FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
 4. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. 5. CONTROLLING DIMENSION: INCH.
- 6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

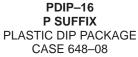
| | INC | HES | MILLIMETERS | | | | |
|-----|-------|-------|-------------|-------|--|--|--|
| DIM | MIN | MAX | MIN | MAX | | | |
| Α | 0.385 | 0.395 | 9.78 | 10.03 | | | |
| В | 0.385 | 0.395 | 9.78 | 10.03 | | | |
| С | 0.165 | 0.180 | 4.20 | 4.57 | | | |
| Ε | 0.090 | 0.110 | 2.29 | 2.79 | | | |
| F | 0.013 | 0.019 | 0.33 | 0.48 | | | |
| G | 0.050 | BSC | 1.27 | BSC | | | |
| Н | 0.026 | 0.032 | 0.66 | 0.81 | | | |
| J | 0.020 | | 0.51 | | | | |
| K | 0.025 | | 0.64 | | | | |
| R | 0.350 | 0.356 | 8.89 | 9.04 | | | |
| U | 0.350 | 0.356 | 8.89 | 9.04 | | | |
| ٧ | 0.042 | 0.048 | 1.07 | 1.21 | | | |
| W | 0.042 | 0.048 | 1.07 | 1.21 | | | |
| Χ | 0.042 | 0.056 | 1.07 | 1.42 | | | |
| Υ | | 0.020 | | 0.50 | | | |
| Z | 2° | 10 ° | 2 ° | 10 ° | | | |
| G1 | 0.310 | 0.330 | 7.88 | 8.38 | | | |
| K1 | 0.040 | | 1.02 | | | | |
| | | | | | | | |

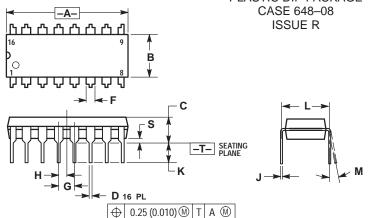
PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| | INC | HES | MILLIMETERS | | |
|-----|-------|---------|-------------|-------|--|
| DIM | MIN | MIN MAX | | MAX | |
| Α | 0.750 | 0.785 | 19.05 | 19.93 | |
| В | 0.240 | 0.295 | 6.10 | 7.49 | |
| С | | 0.200 | | 5.08 | |
| D | 0.015 | 0.020 | 0.39 | 0.50 | |
| E | 0.050 |) BSC | 1.27 BSC | | |
| F | 0.055 | 0.065 | 1.40 | 1.65 | |
| G | 0.100 | BSC | 2.54 BSC | | |
| Н | 0.008 | 0.015 | 0.21 | 0.38 | |
| K | 0.125 | 0.170 | 3.18 | 4.31 | |
| L | 0.300 | BSC | 7.62 BSC | | |
| M | 0° | 15° | 0 ° | 15° | |
| N | 0.020 | 0.040 | 0.51 | 1.01 | |





- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

 5. ROUNDED CORNERS OPTIONAL.

| | INC | HES | MILLIMETERS | | |
|-----|-------|-------|-------------|-------|--|
| DIM | MIN | MAX | MIN | MAX | |
| Α | 0.740 | 0.770 | 18.80 | 19.55 | |
| В | 0.250 | 0.270 | 6.35 | 6.85 | |
| С | 0.145 | 0.175 | 3.69 | 4.44 | |
| D | 0.015 | 0.021 | 0.39 | 0.53 | |
| F | 0.040 | 0.70 | 1.02 | 1.77 | |
| G | 0.100 | BSC | 2.54 BSC | | |
| Н | 0.050 | BSC | 1.27 BSC | | |
| J | 0.008 | 0.015 | 0.21 | 0.38 | |
| K | 0.110 | 0.130 | 2.80 | 3.30 | |
| L | 0.295 | 0.305 | 7.50 | 7.74 | |
| M | 0° | 10 ° | 0 ° | 10 ° | |
| S | 0.020 | 0.040 | 0.51 | 1.01 | |

Notes

Notes

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