

MC100LVE222

Low Voltage 1:15 Differential $\div 1/\div 2$ ECL/PECL Clock Driver

The MC100LVE222 is a low skew 1:15 differential $\div 1/\div 2$ ECL fanout buffer designed with clock distribution in mind. The LVECL/LVPECL input signal pairs can be differential or used single-ended (with VBB output reference bypassed and connected to the unused input of a pair). Either of two fully differential clock inputs may be selected. Each of the four output banks of 2, 3, 4, and 6 differential pairs may be independently configured to fanout 1X or 1/2X of the input frequency. The LVE222 specifically guarantees low output to output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

The fsel pins and CLK_Sel pin are asynchronous control inputs. Any changes may cause indeterminate output states requiring a MR pulse to resynchronize any 1/2X outputs.

To ensure that the tight skew specification is realized, both sides of any differential output pair need to be terminated identically even if only one side is being used. When fewer than all fifteen pairs are used, identically terminate all the output pairs on the same package side whether used or unused. If no outputs on a side are used, then leave all these outputs open (unterminated). This will maintain minimum output skew. Failure to do this will result in a 10–20ps loss of skew margin (propagation delay) in the output(s) in use.

The MC100LVE222, as with most ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE222 to be used for high performance clock distribution in +3.3V systems. Designers can take advantage of the LVE222's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line, terminations are typically used as they require no additional power supplies. All power supply pins must be connected. For more information on using PECL, designers should refer to Application Note AN1406/D. For a SPICE model, see Application Note AN1560/D.

- 200ps Part-to-Part Skew
- 50ps Output-to-Output Skew
- Selectable 1x or 1/2x Frequency Outputs
- Extended Power Supply Range of -3.0V to -5.25V (+3.0V to +5.25V)
- 52-Lead TQFP Packaging
- ESD > 2000V
- Moisture Sensitivity Level 2,
For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",
Oxygen Index 28 to 34
- Transistor Count = 684 devices

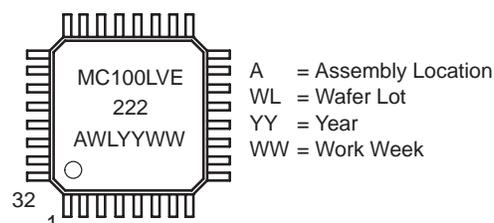


ON Semiconductor
Formerly a Division of Motorola
<http://onsemi.com>



**TQFP
FA SUFFIX
CASE 848D**

MARKING DIAGRAM*



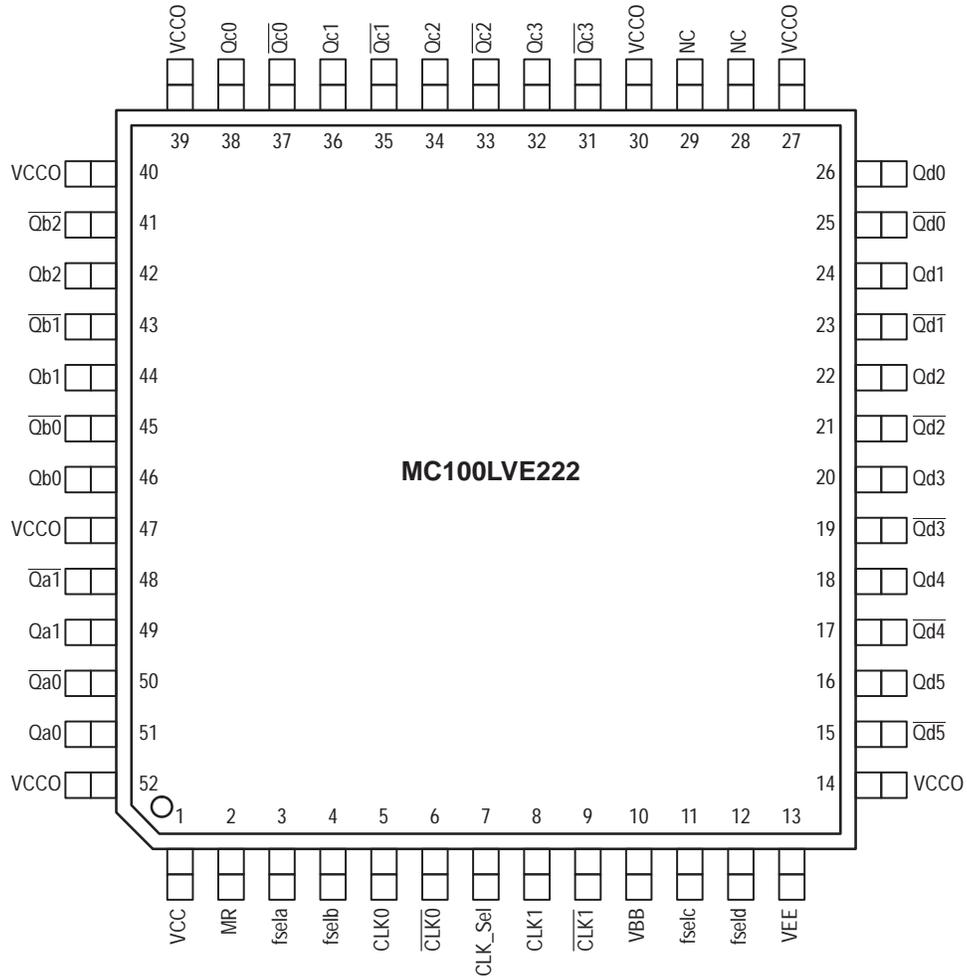
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

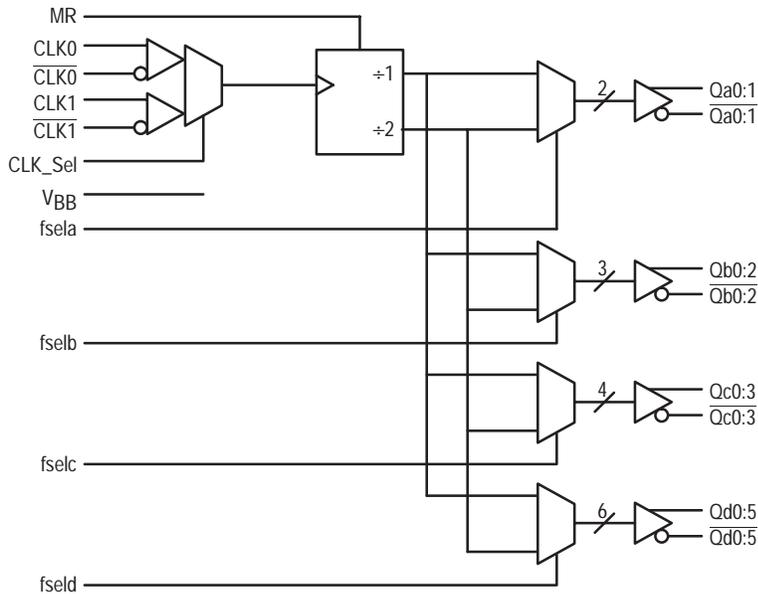
Device	Package	Shipping
MC100LVE222FA	TQFP	800 Units/Tray
MC100LVE222FAR2	TQFP	1500 Tape & Reel

MC100LVE222

Pinout: 52-Lead TQFP (Top View)



LOGIC SYMBOL



FUNCTION TABLE

Input	Function	
	0	1
MR	Active	Reset
CLK_Sel	CLK0	CLK1
fseln	+1	+2

MC100LVE222

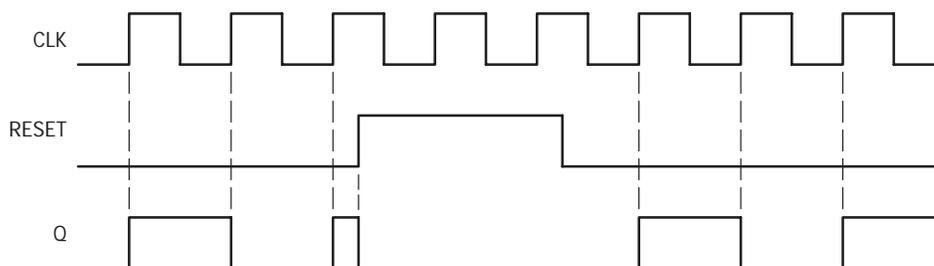


Figure 1. Timing Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply ($V_{CC} = 0V$)	-8.0 to 0	VDC
V_I	Input Voltage ($V_{CC} = 0V$)	0 to -6.0	VDC
I_{out}	Output Current	50 100	mA
	Continuous Surge		
T_A	Operating Temperature Range	-40 to +85	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

ECL DC CHARACTERISTICS

Symbol	Characteristic	-40°C			0°C			25°C			70°C			Unit
		Min	Typ	Max										
V_{OH}	Output HIGH Voltage	-1.085	-1.005	-0.880	-1.025	-0.955	-0.880	-1.025	-0.955	-0.880	-1.025	-0.955	-0.880	V
V_{OL}	Output LOW Voltage	-1.830	-1.695	-1.555	-1.810	-1.705	-1.620	-1.810	-1.705	-1.620	-1.810	-1.705	-1.620	V
V_{IH}	Input HIGH Voltage	-1.165		-0.880	-1.165		-0.880	-1.165		-0.880	-1.165		-0.880	V
V_{IL}	Input LOW Voltage	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475	V
V_{BB}	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{EE}	Power Supply Voltage	-3.0		-5.25	-3.0		-5.25	-3.0		-5.25	-3.0		-5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{IL}	Input $\overline{CLK0}$, $\overline{CLK1}$ LOW Current Others	-300 0.5			-300 0.5			-300 0.5			-300 0.5			μA
I_{EE}	Power Supply Current		122	136		122	136		122	136		125	139	mA

PECL DC CHARACTERISTICS

Symbol	Characteristic	-40°C			0°C			25°C			70°C			Unit
		Min	Typ	Max										
V_{OH}	Output HIGH Voltage ¹	2.215	2.295	2.420	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage ¹	1.470	1.605	1.745	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage ¹	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage ¹	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage ¹	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	3.0		5.25	3.0		5.25	3.0		5.25	3.0		5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{IL}	Input $\overline{CLK0}$, $\overline{CLK1}$ LOW Current Others	-300 0.5			-300 0.5			-300 0.5			-300 0.5			μA
I_{EE}	Power Supply Current		122	136		122	136		122	136		125	139	mA

1. These values are for $V_{CC} = 3.3V$. Level Specifications will vary 1:1 with V_{CC} .

MC100LVE222

ECL AC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = V_{CCO} = \text{GND}$)

Symbol	Characteristic	-40°C			0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max											
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single-ended) MR	1040 990 1100	1140 1140 1250	1240 1290 1400	1060 1010 1130	1160 1160 1280	1260 1310 1430	1080 1030 1170	1180 1180 1320	1280 1330 1470	1120 1070 1220	1220 1220 1370	1320 1370 1520	ps	Note 1. Note 2.
t_{skew}	Within-Device Skew Part-to-Part Skew (Diff)			50 200			50 200			50 200			50 200	ps	Note 3.
V_{PP}	Minimum Input Swing	400			400			400			400			mV	Note 4.
V_{CMR}	Common Mode Range $V_{PP} < 500\text{mV}$ $V_{PP} \geq 500\text{mV}$	$V_{EE} + 1.3$ $V_{EE} + 1.6$		-0.4 -0.4	$V_{EE} + 1.2$ $V_{EE} + 1.5$		-0.4 -0.4	$V_{EE} + 1.2$ $V_{EE} + 1.5$		-0.4 -0.4	$V_{EE} + 1.2$ $V_{EE} + 1.5$		-0.4 -0.4	V	Note 5.
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. $V_{PP}(\text{min})$ is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The $V_{PP}(\text{min})$ is AC limited for the LVE222. A differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}(\text{min})$.

PECL AC CHARACTERISTICS ($V_{EE} = \text{GND}$; $V_{CC} = V_{CCO} = V_{CC}(\text{min})$ to $V_{CC}(\text{max})$)

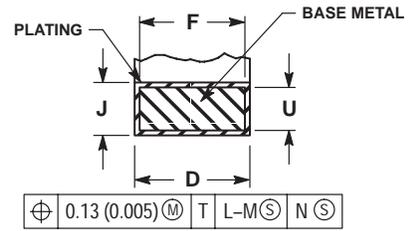
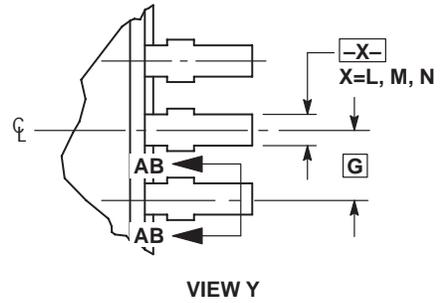
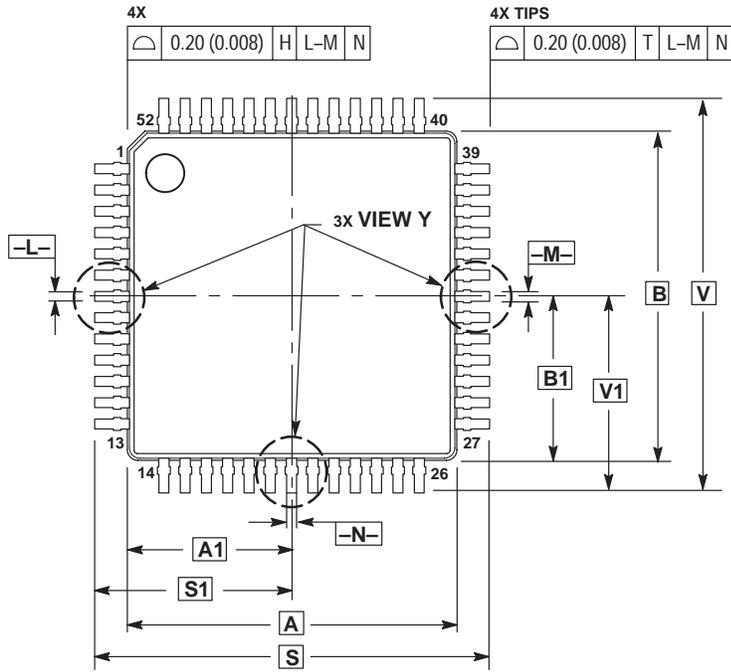
Symbol	Characteristic	-40°C			0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single-ended) MR	1040 990 1100	1140 1140 1250	1240 1290 1400	1060 1010 1130	1160 1160 1280	1260 1310 1430	1080 1030 1170	1180 1180 1320	1280 1330 1470	1120 1070 1220	1220 1220 1370	1320 1370 1520	ps	Note 1. Note 2.
t_{skew}	Within-Device Skew Part-to-Part Skew (Diff)			50 200			50 200			50 200			50 200	ps	Note 3.
V_{PP}	Minimum Input Swing	400			400			400			400			mV	Note 4.
V_{CMR}	Common Mode Range $V_{PP} < 500\text{mV}$ $V_{PP} \geq 500\text{mV}$	1.3 1.6		$V_{CC} - 0.4$ $V_{CC} - 0.4$	1.2 1.5		$V_{CC} - 0.4$ $V_{CC} - 0.4$	1.2 1.5		$V_{CC} - 0.4$ $V_{CC} - 0.4$	1.2 1.5		$V_{CC} - 0.4$ $V_{CC} - 0.4$	V	Note 5.
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. $V_{PP}(\text{min})$ is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The $V_{PP}(\text{min})$ is AC limited for the LVE222. A differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}(\text{min})$.

MC100LVE222

PACKAGE DIMENSIONS

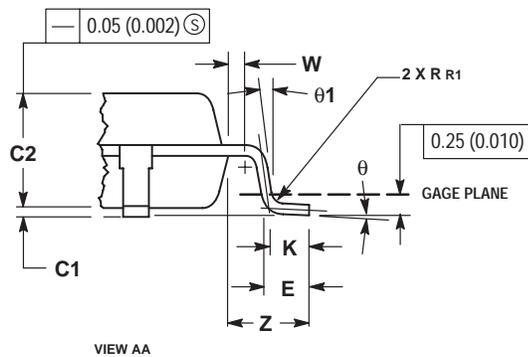
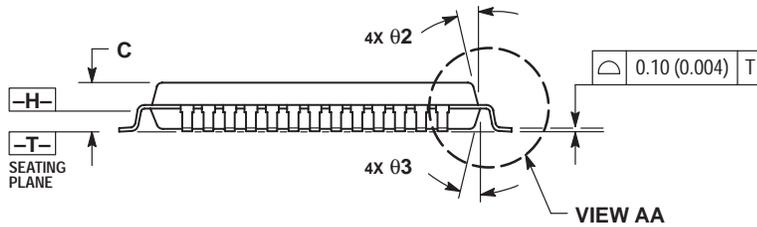
FA SUFFIX
TQFP PACKAGE
CASE 848D-03
ISSUE C



SECTION AB-AB
ROTATED 90° CLOCKWISE

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
- DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.00	BSC	0.394	BSC
A1	5.00	BSC	0.197	BSC
B	10.00	BSC	0.394	BSC
B1	5.00	BSC	0.197	BSC
C	---	1.70	---	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65	BSC	0.026	BSC
J	0.07	0.20	0.003	0.008
K	0.50	REF	0.020	REF
R1	0.08	0.20	0.003	0.008
S	12.00	BSC	0.472	BSC
S1	6.00	BSC	0.236	BSC
U	0.09	0.16	0.004	0.006
V	12.00	BSC	0.472	BSC
V1	6.00	BSC	0.236	BSC
W	0.20	REF	0.008	REF
Z	1.00	REF	0.039	REF
θ	0°	7°	0°	7°
θ1	0°	---	0°	---
θ2	12°	REF	12°	REF
θ3	5°	13°	5°	13°

Notes

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (M-F 1:00pm to 5:00pm Munich Time)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (M-F 1:00pm to 5:00pm Toulouse Time)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (M-F 12:00pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, England, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549
Phone: 81-3-5740-2745
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.