Product Preview

÷2/4, ÷4/5/6 Clock Generation Chip

MC100EP39

The MC100EP39 is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single–ended LVECL or, if positive power supplies are used, LVPECL input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device (see Interfacing section of the ECLinPS™ Data Book DL140/D). If a single–ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EP39 under single–ended input conditions, as a result, this pin can only source/sink up to 0.5mA of current.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip–flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip–flops will attain a random state; therefore, for systems which utilize multiple EP39s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EP39, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/5/6 outputs of a single device.

- 50ps Output–to–Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 75kΩ Internal Input Pulldown Resistors
- >2000V ESD Protection
- Low Voltage V_{EE} Range of –3.0 to –3.8V; –5V Tolerant

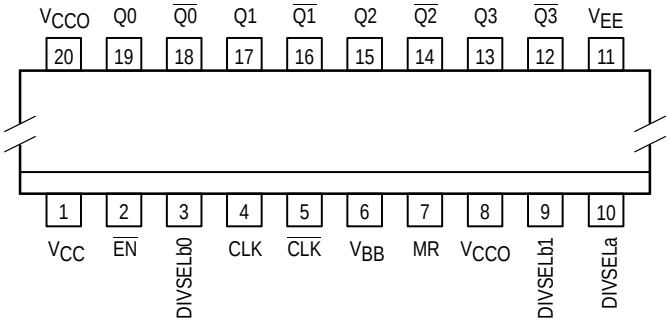
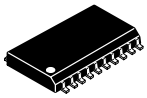


Figure 1. 20–Lead SOIC (Top View)



DW SUFFIX
20–LEAD PLASTIC WIDE SOIC PACKAGE
CASE 751D–05

PIN NAMES

PIN	FUNCTION
CLK	Diff Clock Inputs
$\overline{EN}$	Sync Enable
MR	Master Reset
V_{BB}	Reference Output
Q0, Q1	Diff ÷2/4 Outputs
Q2,Q3	Diff ÷4/5/6 Outputs
DIVSEL	Frequency Select Input

FUNCTION TABLES

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

Z = Low–to–High Transition
ZZ = High–to–Low Transition

DIVSELa	Q0:1 OUTPUTS
0	Divide by 2
1	Divide by 4

DIVSELb0	DIVSELb1	Q2:3 OUTPUTS
0	0	Divide by 4
1	0	Divide by 6
0	1	Divide by 5
1	1	Divide by 5

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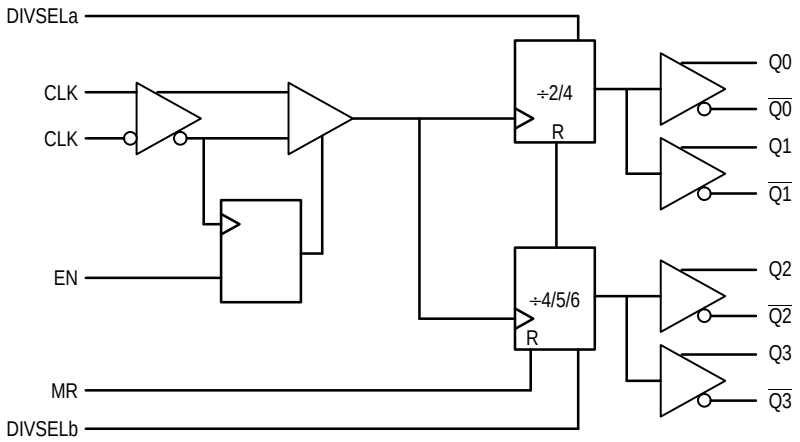


Figure 2. Logic Diagram

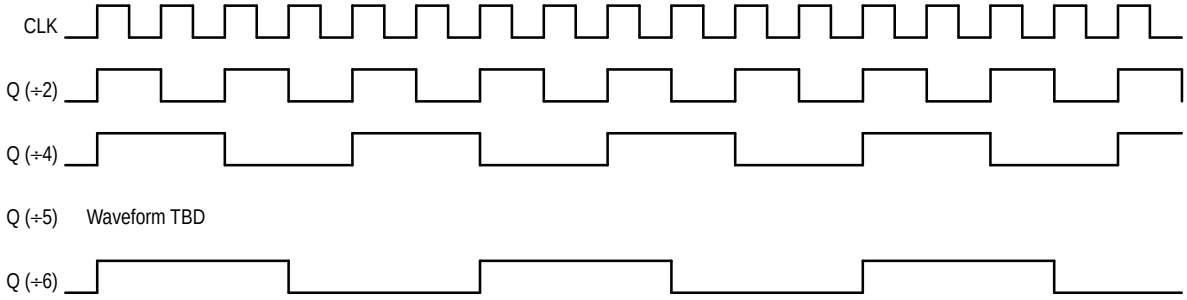


Figure 3. Timing Diagrams

DC CHARACTERISTICS (V_{EE} = –3.8V to –3.0; V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50			50			50			54		mA
V_{BB}	Output Reference Voltage		Note 1.			Note 1.			Note 1.			Note 1.		V
I_{IH}	Input High Current			150			150			150			150	μA

1. $V_{BB} = V_{CC} – 1.425 \pm 75mV$

DC CHARACTERISTICS (V_{EE} = –5V; $V_{CC} = V_{CCO}$ = GND; T_A = 0°C to + 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions	
V_{OH}	Output HIGH Voltage		$V_{CC} – 1.03 \pm 75mV$		mV	$V_{IN} = V_{IH}$(max)	Loading with 50Ω to – 2.0V
V_{OL}	Output LOW Voltage		$V_{CC} – 1.82 \pm 75mV$		mV	or V_{IL}(min)	
V_{OHA}	Output HIGH Voltage				mV	$V_{IN} = V_{IH}$(min)	
V_{OLA}	Output LOW Voltage				mV	or V_{IL}(max)	
V_{IH}	Input HIGH Voltage		1022.5		mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage		1642.5		mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5			μA	$V_{IN} = V_{IL}$(min)	

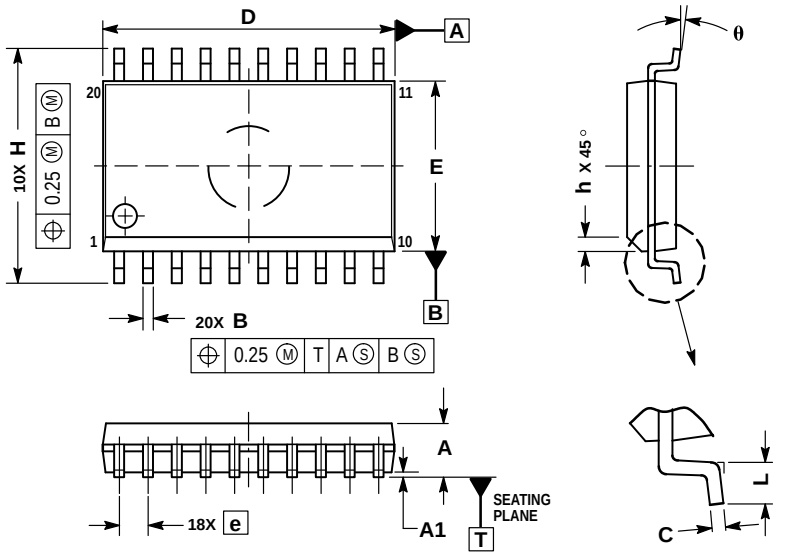
AC CHARACTERISTICS (V_{EE} = –3.8V to –3.0; V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		1500			1500			1500			1500		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK → Q (Diff) CLK → Q (S.E.) MR → Q		860 860 750			880 880 750			900 900 760			950 950 780		ps
t_{SKEW}	Within–Device Skew (Note 2.) $Q_0 - Q_3$			50			50			50			50	ps
	Part–to–Part $Q_0 - Q_3$ (Diff)			200			200			200			200	
t_S	Setup Time $\overline{EN} \rightarrow \overline{CLK}$ DIVSEL → CLK		300 450			300 450			300 450			300 450		ps
t_H	Hold Time $\overline{CLK} \rightarrow \overline{EN}$ CLK → Div_Sel		150 200			150 200			150 200			150 200		ps
V_{PP}	Minimum Input Swing (Note 3.) CLK		300			300			300			300		mV
V_{CMR}	Common Mode Range (Note 4.) V_{PP} < 500mV V_{PP} ≥ 500mV	–2.0 –1.8		–0.4 –0.4	–2.1 –1.9		–0.4 –0.4	–2.1 –1.9		–0.4 –0.4	–2.1 –1.9		–0.4 –0.4	V
t_{RR}	Reset Recovery Time			100			100			100			100	ps
t_{PW}	Minimum Pulse Width CLK MR		600 800			600 800			600 800			600 800		ps
t_r, t_f	Output Rise/Fall Times Q (20% – 80%)		415			415			415			415		ps

2. Skew is measured between outputs under identical transitions.
3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak–to–peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC WIDE SOIC PACKAGE
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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