PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μPD16315

1/4- to 1/12-DUTY FIP™(VFD) CONTROLLER/DRIVER

DESCRIPTION

The μPD16315 is a FIP (fluorescent Indicator Panel, or Vacuum Fluorescent Display) controller/driver that is driven on a 1/4- to 1/12- duty factor. It consists of 16 segment output lines, 4 grid output lines, 8 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the μPD16315 through a three-line serial interface. This FIP controller/driver is ideal as a peripheral device for a single-chip microcomputer.

FEATURES

- Multiple display modes (16-segment & 12-digit to 24-segment & 4-digit)
- Key scanning (16 × 2 matrix)
- Dimming circuit (eight steps)
- High-voltage output (V_{DD} – 35 V MAX.)
- LED ports (4 chs., 20 mA MAX.)
- No external resistors necessary for driver outputs (P-ch open-drain + pull-down resistor output)
- Serial interface (CLK, STB, D_{IN}, D_{OUT})

ORDERING INFORMATION

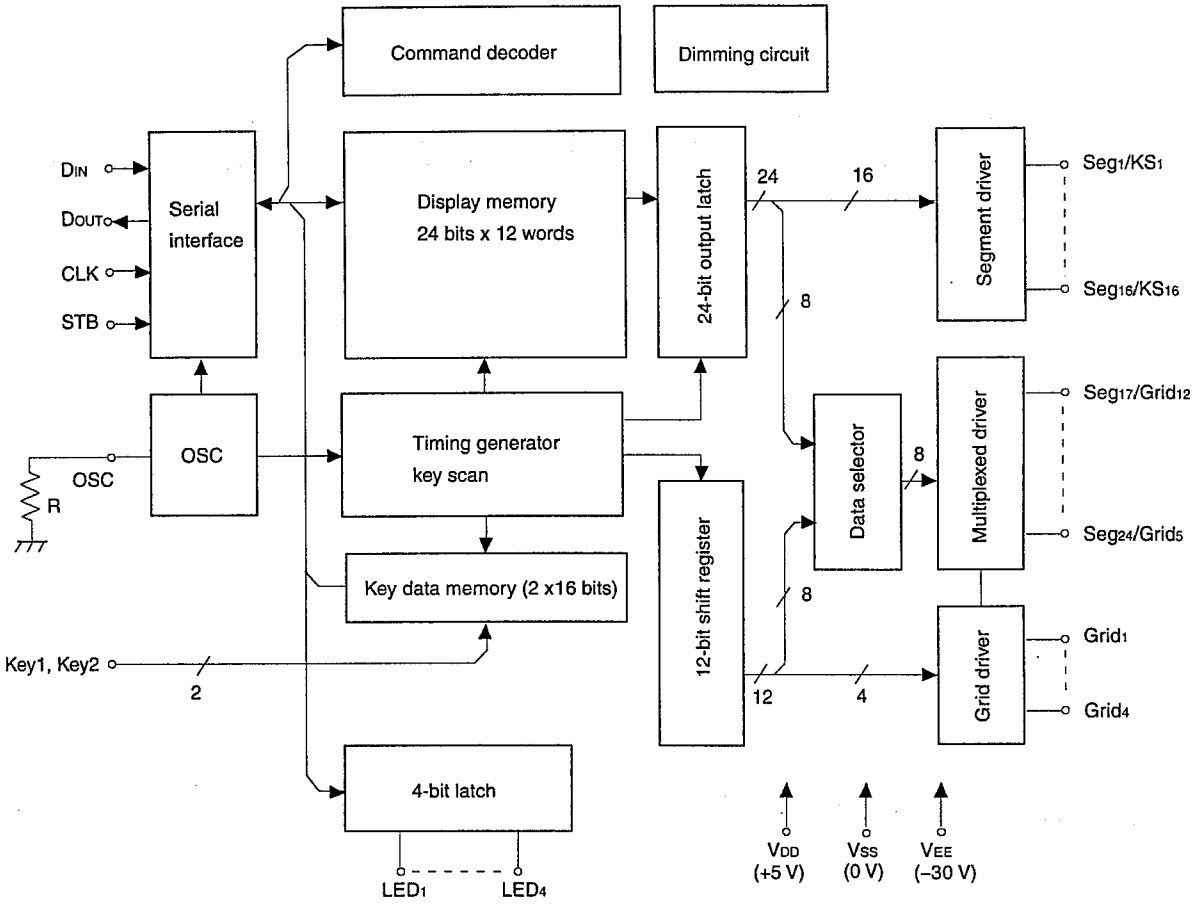
Part Number	Package
μPD16315GB-3BS	44-pin Plastic QFP (10 x 10)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Document No. S14074EJ3V0PM00 (3rd edition)
Date Published September 1999 NS CP(K)
Printed in Japan

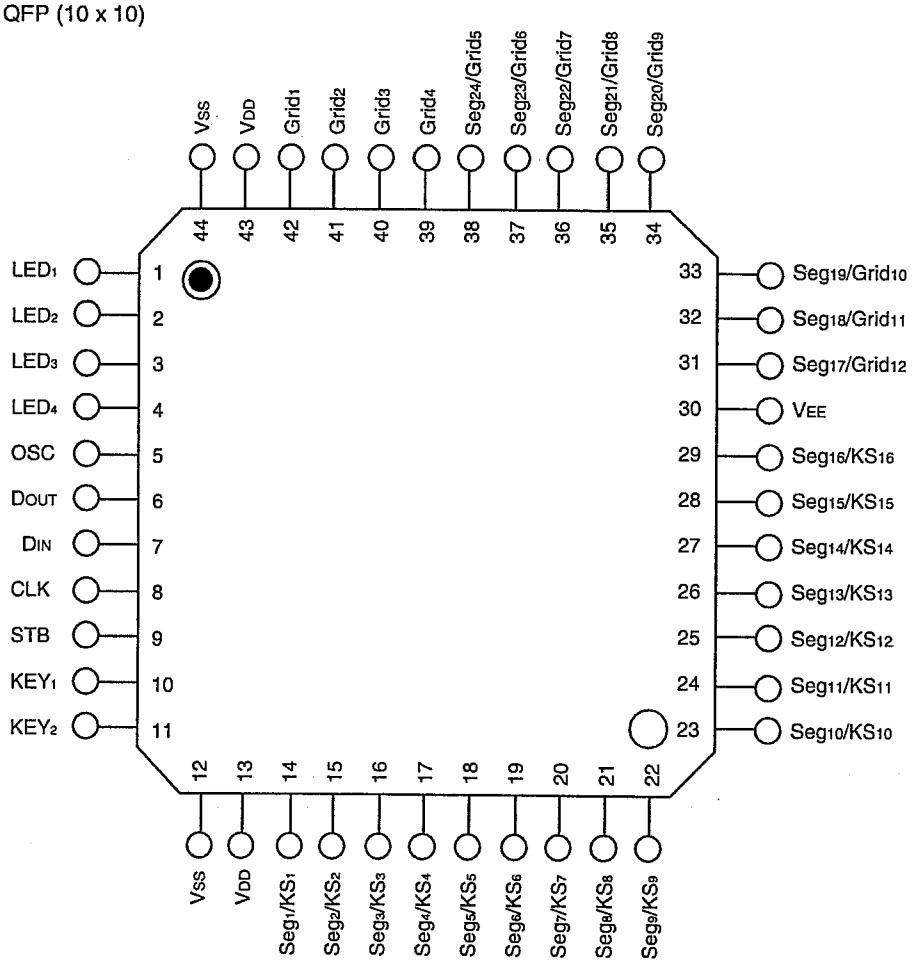
The mark ★ shows major revised points.

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

44-pin Plastic QFP (10 x 10)



Caution Use all of the power supply pins.

PIN FUNCTION

Symbol	Pin Name	Pin No.	Description
D_{IN}	Data input	7	Input serial data at rising edge of shift clock, starting from the low order bit.
D_{OUT}	Data output	6	Output serial data at the falling edge of the shift clock, starting from low order bit. This is N-ch open-drain output pin.
STB	Strobe	9	Initializes serial interface at the rising or falling edge of the μPD16315. It then waits for reception of a command. Data input after STB has fallen is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While STB is high, CLK is ignored.
CLK	Clock input	8	Reads serial data at the rising edge, and outputs data at the falling edge.
OSC	Oscillator pin	5	Connect resistor to this pin to determine the oscillation frequency to this pin. Connect resistor between this pin and GND (V_{SS}).
Seg_1/KS_1 to Seg_{16}/KS_{16}	High-voltage output (Segment)	14 to 29	Segment output pins (Dual function as key source)
$Grid_1$ to $Grid_4$	High-voltage output (grid)	39 to 42	Grid output pins
$Seg_{17}/Grid_{12}$ to $Seg_{24}/Grid_5$	High-voltage output (segment/grid)	31 to 38	These pins are selectable for segment or grid driving.
LED_1 to LED_4	LED output	1 to 4	CMOS output, +20 mA MAX.
KEY_1, KEY_2	Key data input	10, 11	Data input to these pins is latched at the end of the display cycle.
★ V_{DD}	Logic power	13, 43	5 V ± 10 %
★ V_{SS}	Logic ground	12, 44	Connect this pin to system GND.
★ V_{EE}	Pull-down level	30	V_{DD} – 35 V MAX.

DISPLAY RAM ADDRESS AND DISPLAY MODE

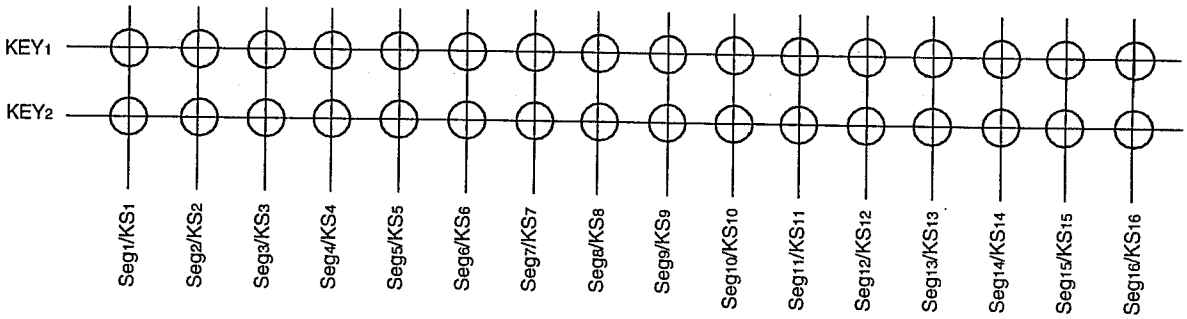
The display RAM stores the data transmitted to the μPD16315 through the serial communication. The addresses are allocated in 8-bit units.

Seg_1	Seg_4	Seg_8	Seg_{12}	Seg_{16}	Seg_{20}	Seg_{24}	
$00H_L$	$00H_U$	$01H_L$	$01H_U$	$02H_L$	$02H_U$		DIG_1
$03H_L$	$03H_U$	$04H_L$	$04H_U$	$05H_L$	$05H_U$		DIG_2
$06H_L$	$06H_U$	$07H_L$	$07H_U$	$08H_L$	$08H_U$		DIG_3
$09H_L$	$09H_U$	$0AH_L$	$0AH_U$	$0BH_L$	$0BH_U$		DIG_4
$0CH_L$	$0CH_U$	$0DH_L$	$0DH_U$	$0EH_L$	$0EH_U$		DIG_5
$0FH_L$	$0FH_U$	$10H_L$	$10H_U$	$11H_L$	$11H_U$		DIG_6
$12H_L$	$12H_U$	$13H_L$	$13H_U$	$14H_L$	$14H_U$		DIG_7
$15H_L$	$15H_U$	$16H_L$	$16H_U$	$17H_L$	$17H_U$		DIG_8
$18H_L$	$18H_U$	$19H_L$	$19H_U$	$1AH_L$	$1AH_U$		DIG_9
$1BH_L$	$1BH_U$	$1CH_L$	$1CH_U$	$1DH_L$	$1DH_U$		DIG_{10}
$1EH_L$	$1EH_U$	$1FH_L$	$1FH_U$	$20H_L$	$20H_U$		DIG_{11}
$21H_L$	$21H_U$	$22H_L$	$22H_U$	$23H_L$	$23H_U$		DIG_{12}

b0	b3	b4	b7
XXH_L		XXH_U	
Lower 4 bits		Higher 4 bits	

KEY MATRIX AND KEY-INPUT DATA STORAGE RAM

The key matrix is made up of a 16 × 2 matrix, as shown below.



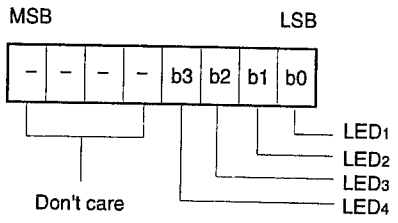
The data of each key is stored as follows, and is read with the read command starting from the least significant bit.

KEY1	KEY2	KEY1	KEY2	KEY1	KEY2	KEY1	KEY2
Seg1/KS1		Seg2/KS2		Seg3/KS3		Seg4/KS4	
Seg5/KS5		Seg6/KS6		Seg7/KS7		Seg8/KS8	
Seg9/KS9		Seg10/KS10		Seg11/KS11		Seg12/KS12	
Seg13/KS13		Seg14/KS14		Seg15/KS15		Seg16/KS16	
b0	b1	b2	b3	b4	b5	b6	b7

Reading Sequence

LED PORT

Data is written to the LED port with the write command, starting from the least significant bit. "L" output when the bit of this port is 0, and "H" output when the bit is 1. The data of bits after the 5th bit are ignored.



Remark On power application, all the LED ports are "L" output.

COMMANDS

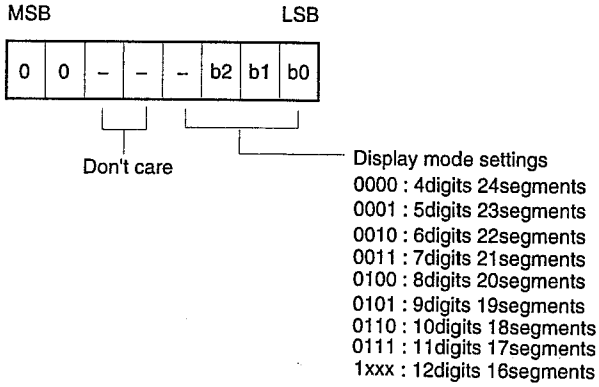
Commands set the display mode and status of the FIP driver.

The first 1 byte input to the μPD16315 through the DIN pin after the STB pin has fallen is regarded as a command. If STB is set high while commands/data are transmitted, serial communication is initialized, and the commands/data being transmitted are invalid (however, the commands/data previously transmitted remain valid).

(1) Display mode setting commands

These commands initialize the μPD16315 and select the number of segments and the number of grids (1/4- to 1/12- duty, 16 segments to 24 segments).

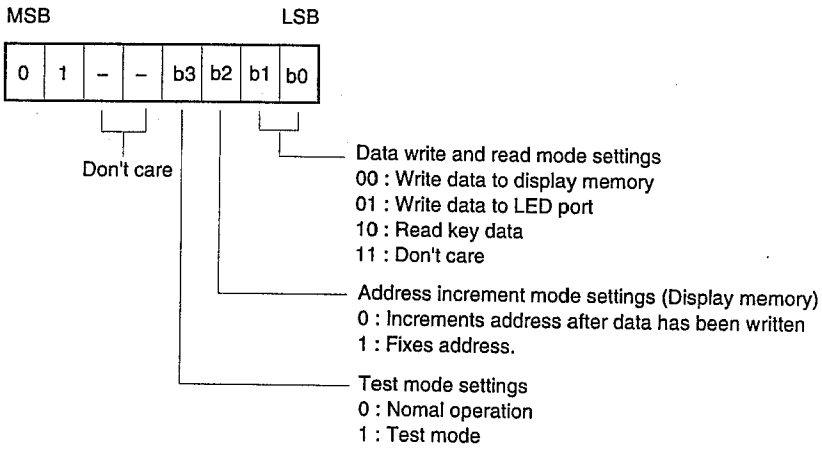
When these commands are executed, the display is forcibly turned off, and key scanning is also stopped. To resume display, the display command "ON" must be executed. If the same mode is selected, however, nothing happens.



Remark On power application, the 12-digit, 16-segment mode is selected.

(2) Data setting commands

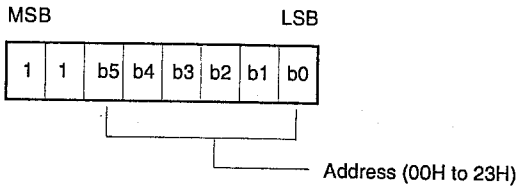
These commands set data write and data read modes.



Remark On power application, the normal operation and address increment modes are set.

(3) Address setting commands

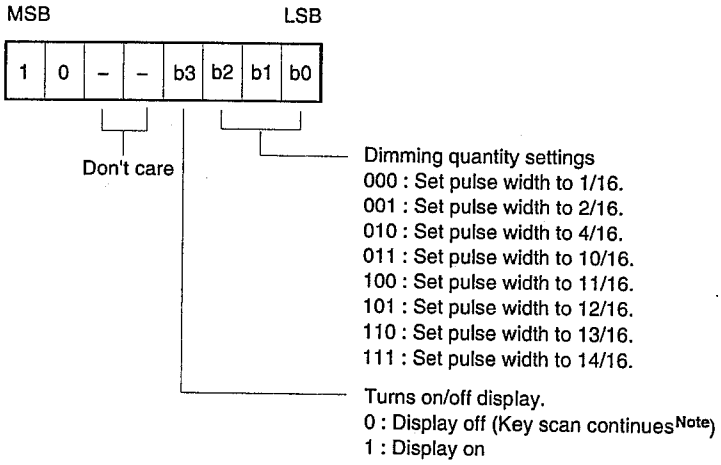
These commands set an address of the display memory.



Remarks 1. If address 24H or higher is set, data is ignored, until a valid address is set.

2. On power application, the address is set to 00H.

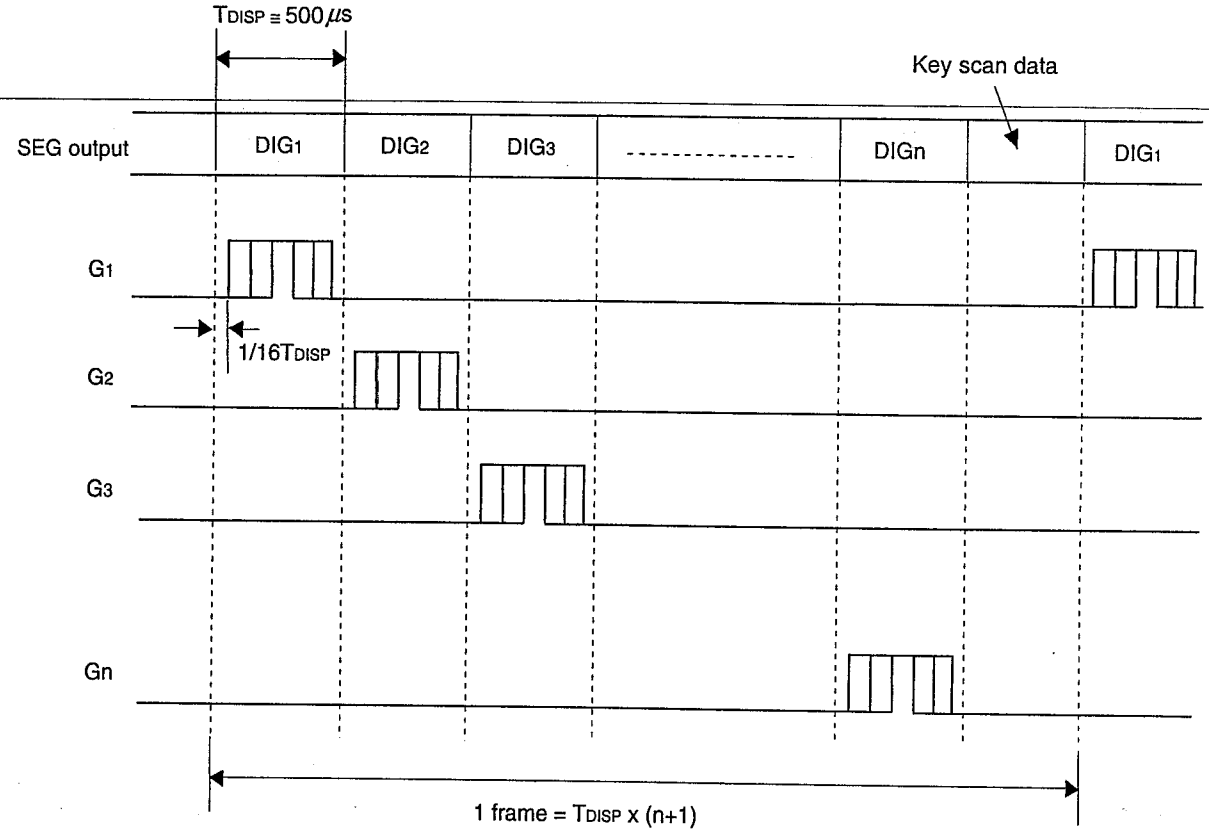
(4) Display control commands



Note On power application, key scanning is stopped.

Remark On power application, the 1/16 pulse width is set and the display is turned off.

KEY SCANNING AND DISPLAY TIMING



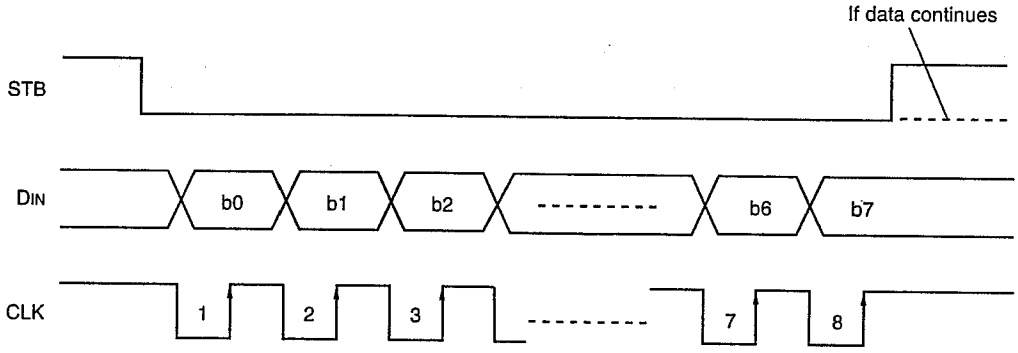
Remark One cycle of key scanning consists of two frame, and data in a 16 × 2 matrix is stored in RAM.

Key Scan Expansion

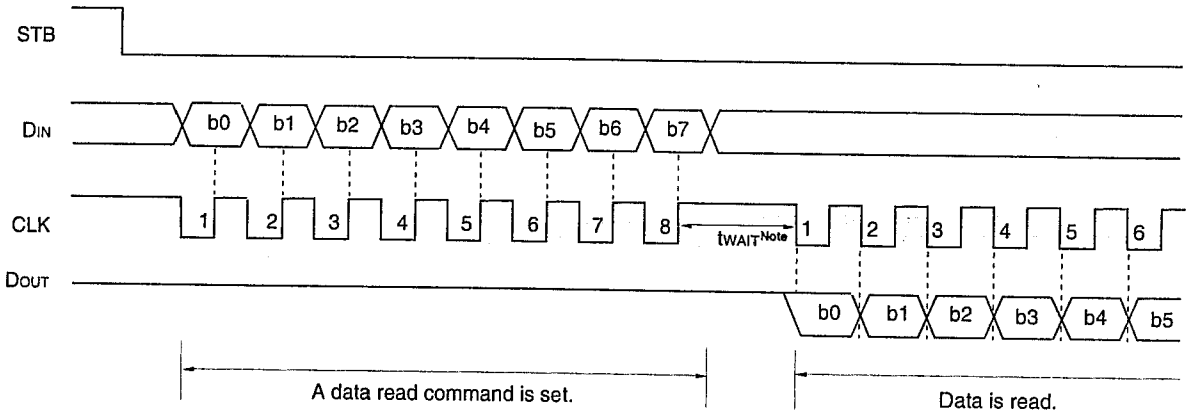
1st frame	DIGn	1	2	3	4	5	6	7	8	DIG1
2nd frame		9	10	11	12	13	14	15	16	

SERIAL COMMUNICATION FORMAT

Reception (command/data write)



Transmission (data read)



Note When data is read, a wait time t_{WAIT} of 1 μs is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

Remark Because the DOUT pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor (1 kΩ to 10 kΩ) to this pin.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V_{DD}	−0.5 to +6.0	V
Driver Supply Voltage	V_{EE}	V_{DD} + 0.5 to V_{DD} − 40	V
Logic Input Voltage	V_{I1}	−0.5 to V_{DD} + 0.5	V
FIP Driver Output Voltage	V_{O2}	V_{EE} − 0.5 to V_{DD} + 0.5	V
LED Driver Output Current	I_{O1}	±20	mA
FIP Driver Output Current	I_{O2}	−40 (grid) −15 (segment)	mA
Power Dissipation	P_D	800[Note]	mW
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note Derate at −6.4 mW/°C at T_A = 25 °C or higher.

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = −20 to 70 °C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{DD}	4.5	5	5.5	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD}	V
Driver Supply Votlage	V_{EE}	0		V_{DD} − 35	V

Remark Maximum power consumption $P_{MAX.}$ = FIP driver dissipation + R_L dissipation + LED driver dissipation + dynamic power consumption

Where segment current = 3 mA, grid current = 15 mA, and LED current = 20 mA,

FIP driver dissipation = number of segments × 6 + number of grids/(number of grids + 1) × 30 (mW)

R_L dissipation ≅ $(V_{DD} - V_{EE})^2/50 \times$ (number of segments + 1) (mW)

LED driver dissipation = number of LEDs × 20 (mW)

Dynamic power consumption = $V_{DD} \times 5$ (mW)

Electrical Characteristics (T_A = –20 to +70 °C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, V_{EE} = V_{DD} – 35 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V_{OH1}	LED_1 - LED_4, I_{OH1} = –15 mA	V_{DD} – 1			V
Low-Level Output Voltage	V_{OL1}	LED_1 - LED_4, I_{OL1} = +15 mA			1	V
Low-Level Output Voltage	V_{OL2}	D_{OUT}, I_{OL2} = 4 mA			0.4	V
High-Level Output Current	I_{OH21}	V_O = V_{DD} – 2 V, Seg_1/ KS_1 to Seg_{16}/ KS_{16}	–3			mA
High-Level Output Current	I_{OH22}	V_O = V_{DD} – 2 V, $Grid_1$ to $Grid_4$ Seg_{17}/ $Grid_{12}$ to Seg_{24}/ $Grid_5$	–15			mA
Driver Leakage Current	I_{OLEAK}	V_O = V_{DD} – 35 V, driver off			–10	μA
Output Pull-Down Resistor	R_L	Driver output	40	65	120	kΩ
Input Current	I_I	V_I = V_{DD} or V_{SS}			±1	μA
High-Level Input Voltage	V_{IH}		0.7 V_{DD}			V
Low-Level Input Voltage	V_{IL}				0.3 V_{DD}	V
Hysteresis Voltage	V_H	CLK, D_{IN}, STB		0.35		V
Dynamic Current Consumption	I_{DDdyn}	Under no load, display off			5	mA

Switching Characteristics (T_A = –20 to +70 °C, V_{DD} = 4.5 to 5.5 V, V_{EE} = –30 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Oscillation Frequency	f_{OSC}	R = 82 kΩ		350	500	650	kHz
Propagation Delay Time	t_{PLZ}	CLK → D_{OUT}				300	ns
	t_{PZL}	C_L = 15 pF, R_L = 10 kΩ				100	ns
Rise Time	t_{TZH1}	C_L = 300 pF	Seg_1/KS_1 to Seg_{16}/KS_{16}			2	μs
	t_{TZH2}		$Grid_1$ to $Grid_4$, Seg_{17}/$Grid_{12}$ to Seg_{24}/$Grid_5$			0.5	μs
Fall Time	t_{THZ}	C_L = 300 pF, Seg_n, $Grid_n$				160	μs
Maximum Clock Frequency	$f_{MAX.}$	Duty = 50 %		1			MHz
Input Capacitance	C_I					15	pF