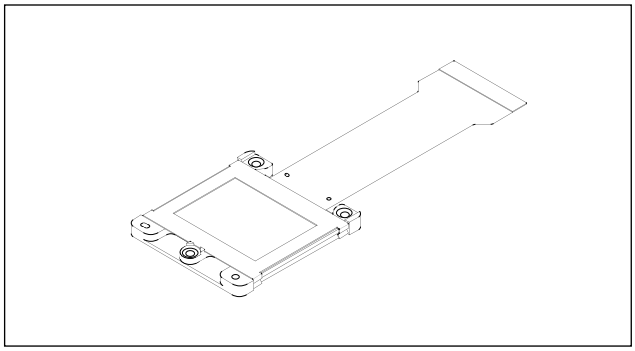
SONY

LCX012BL

3.3cm (1.3-inch) Black-and-White LCD Panel



Description

The LCX012BL is a 3.3cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with built-in peripheral driving circuit. Use of three panels in combination with the LCX012BL provides a full-color representation. The striped arrangement suitable for data projectors is capable of displaying fine text and vertical lines.

The adoption of advanced on-chip black matrix realizes high picture quality without cross talk by incorporating high luminance screen and cross talk free circuit.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.

Using Sony's timing generator "CXD2442Q" sends timing signal necessary for LCD panel drive by identificating computer supporting VGA automatically, and supports double-speed processed NTSC/PAL.

Features

- The number of active dots: 312,000 (1.3-inch; 3.3cm in diagonal)
- Accepts the computer requirements of VGA platform (640 x 480)
- High optical transmittance: 25% (typ.)
- Supports NTSC/PAL by processing the video signal at double speed
- Built-in cross talk free circuit
- High contrast ratio with normally white mode: 250 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function

Element Structure

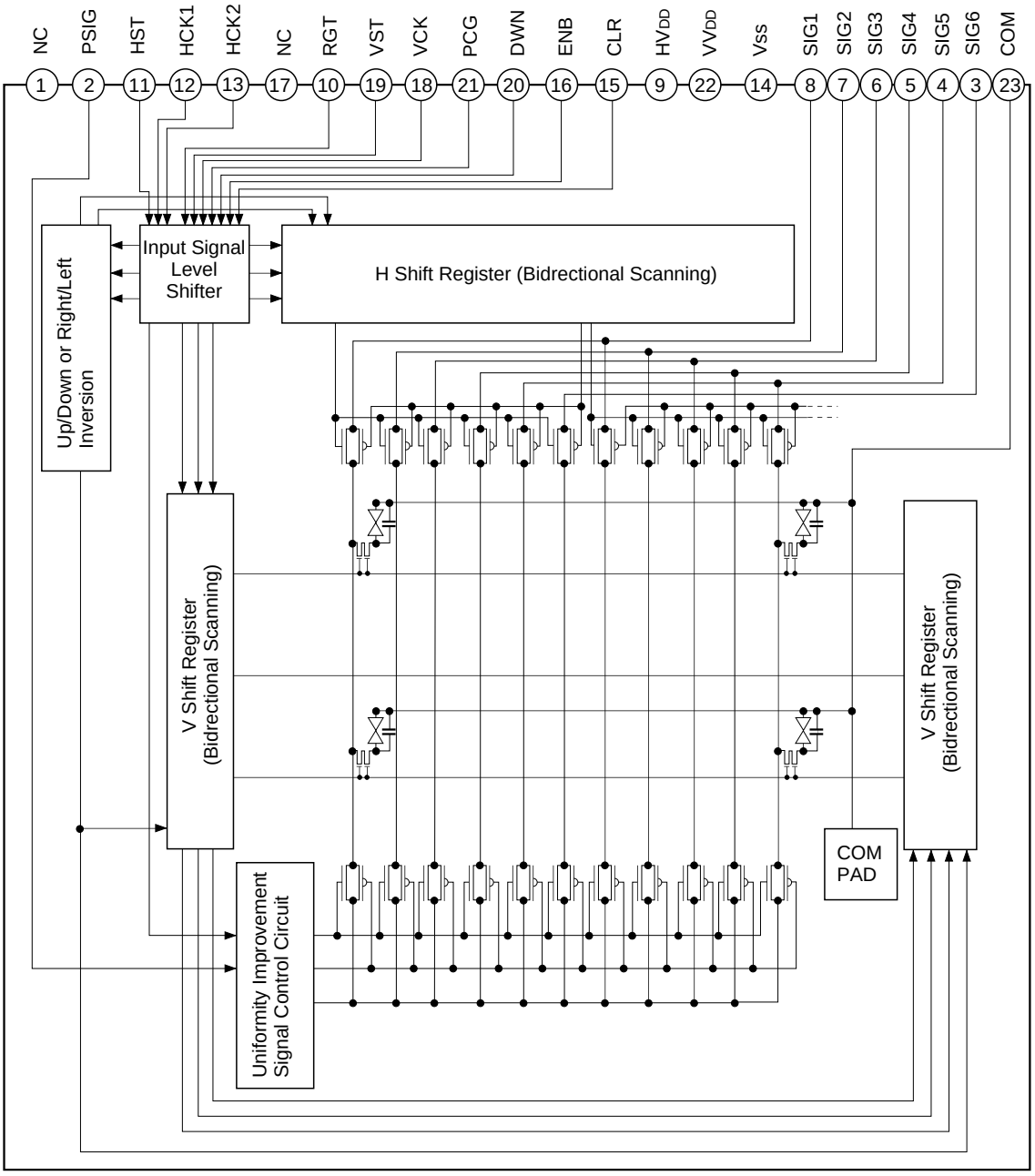
- Dots: 644 (H) $\times$ 484 (V) = 311,696
- Built-in peripheral driver using polycrystalline silicon super thin film transistors.

Applications

- Liquid crystal data projectors
- Liquid crystal projectors, etc.

E96512-ST

Block Diagram



Absolute Maximum Ratings (V_{SS} = 0V)

• H driver supply voltage	HV_{DD}	–1.0 to +20	V
• V driver supply voltage	VV_{DD}	–1.0 to +20	V
• Common pad voltage	COM	–1.0 to +17	V
• H shift register input pin voltage	HST, HCK1, HCK2, RGT	–1.0 to +17	V
• V shift register input pin voltage	VST, VCK, PCG, CLR, ENB, DWN	–1.0 to +17	V
• Video signal input pin voltage	SIG1, SIG2, SIG3, SIG4, SIG5, SIG6, PSIG	–1.0 to +15	V
• Operating temperature	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

Operating Conditions (V_{SS} = 0V)

Supply voltage

HV_{DD} 15.5 ±0.5 V

VV_{DD} 15.5 ±0.5 V

Input pulse voltage (Vp-p of all input pins except video signal and uniformity improvement signal input pins)

Vin 5.0 ±0.5 V

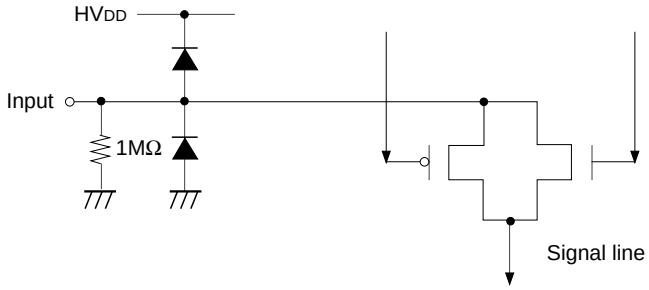
Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC	NC; Open	13	HCK2	Clock pulse for H shift register drive
2	PSIG	Uniformity improvement signal	14	V_{SS}	GND (H, V drivers)
3	SIG6	Video signal 6 to panel	15	CLR	Improvement pulse (1) for uniformity
4	SIG5	Video signal 5 to panel	16	ENB	Enable pulse for gate selection
5	SIG4	Video signal 4 to panel	17	NC	NC; Open
6	SIG3	Video signal 3 to panel	18	VCK	Clock pulse for V shift register drive
7	SIG2	Video signal 2 to panel	19	VST	Start pulse for V shift register drive
8	SIG1	Video signal 1 to panel	20	DWN	Drive direction pulse for V shift register (H: normal, L: reverse)
9	HV_{DD}	Power supply for H driver	21	PCG	Improvement pulse (2) for uniformity
10	RGT	Driver direction pulse for H shift register (H: normal, L: reverse)	22	VV_{DD}	Power supply for V driver
11	HST	Start pulse for H shift register drive	23	COM	Common voltage of panel
12	HCK1	Clock pulse for H shift register drive	24	TEST	Test; Open

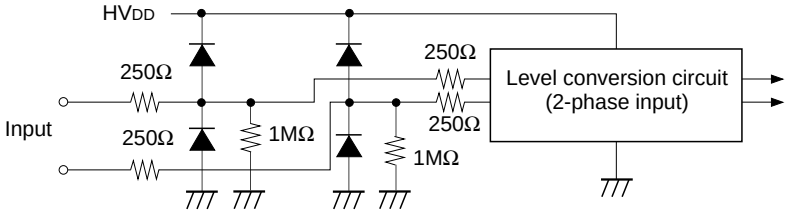
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supply. In addition, protective resistors are added to all pins except video signal input. All pins are connected to V_{SS} with a high resistance of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (The resistor value: typ.)

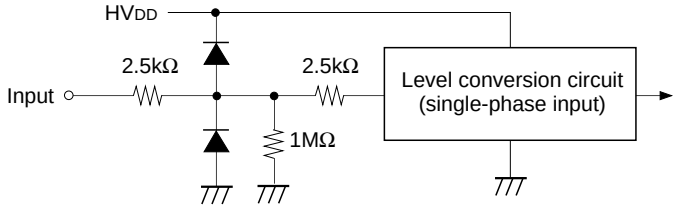
(1) SIG1, SIG2, SIG3, SIG4, SIG5, SIG6, PSIG



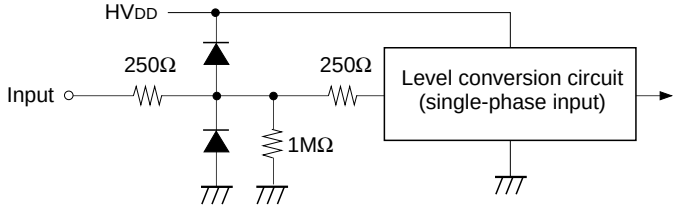
(2) HCK1, HCK2



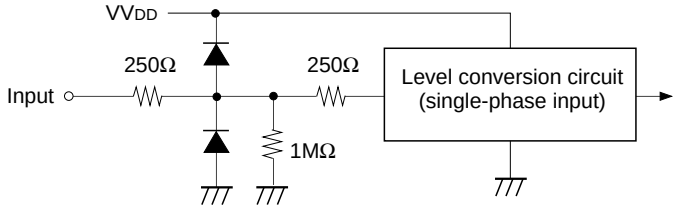
(3) RGT



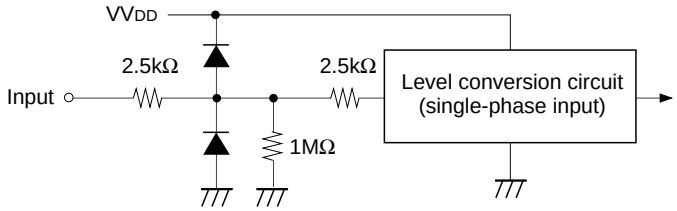
(4) HST



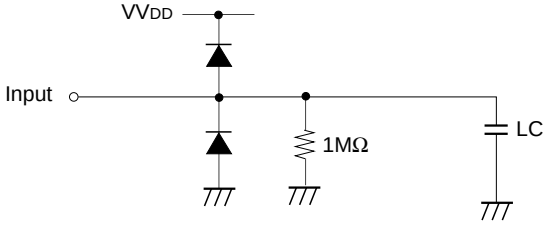
(5) PCG, VCK



(6) VST, CLR, ENB, DWN



(7) COM



Input Signals

1. Input signal voltage conditions

(V_{SS} = 0V)

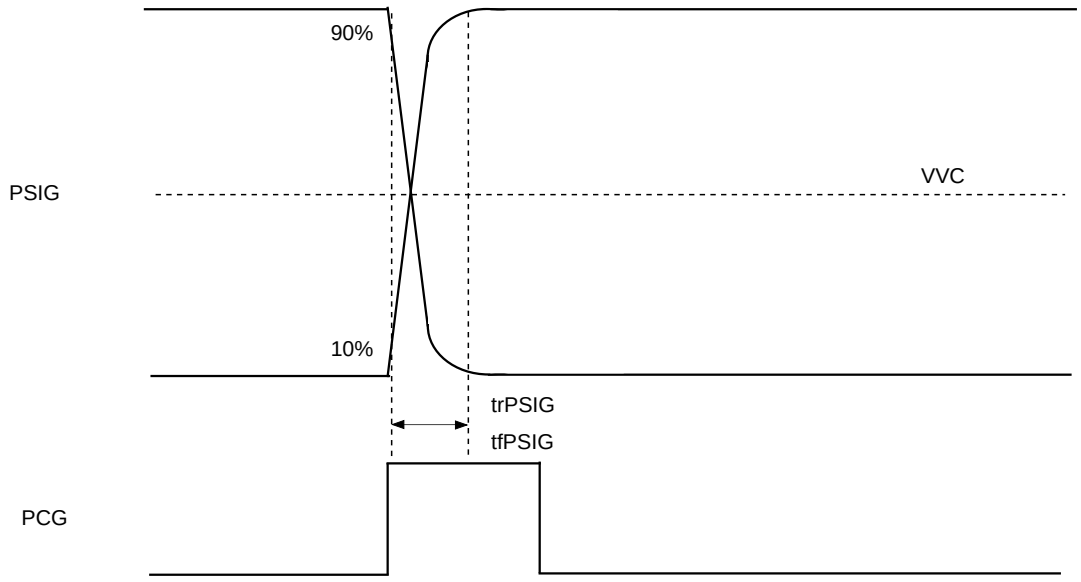
Item		Symbol	Min.	Typ.	Max.	Unit
H driver input voltage	(Low)	VHIL	–0.5	0.0	0.4	V
	(High)	VHIH	4.5	5.0	5.5	V
V driver input voltage	(Low)	VVIL	–0.5	0.0	0.4	V
	(High)	VVIH	4.5	5.0	5.5	V
Video signal center voltage		VVC	6.8	7.0	7.2	V
Video signal input range*1 (SIG1 to 6)		Vsig	VVC – 4.5	7.0	VVC + 4.5	V
Common voltage of panel*2		Vcom	VVC – 0.5	VVC – 0.4	VVC – 0.3	V
Uniformity improvement signal input voltage (PSIG)*3		Vpsig	VVC ± 3.3	VVC ± 3.5	VVC ± 3.7	V

*1 input signal shall be symmetrical to VVC.

*2 The typical value of the common pad voltage may lower its suitable voltage according to the set construction to use. In this case, use the voltage of which has maximum contrast as typical value. When the typical value is lowered, the maximum and minimum values may lower.

*3 Input a uniformity improvement signal PSIG in the same polarity with video signals SIG1 to 6 and which is symmetrical to VVC. Also, the rising and falling of PSIG are synchronized with the rising of PCG pulse, and the rise time trPSIG and fall time tfPSIG are suppressed within 800ns (as shown in a diagram below).

Input waveform of uniformity improvement signal PSIG



Level Conversion Circuit

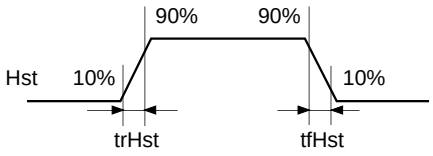
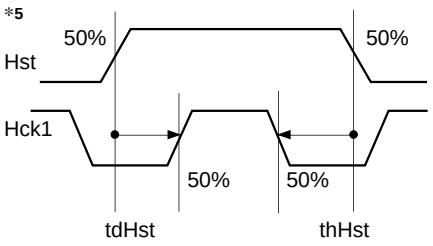
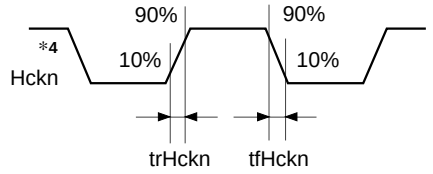
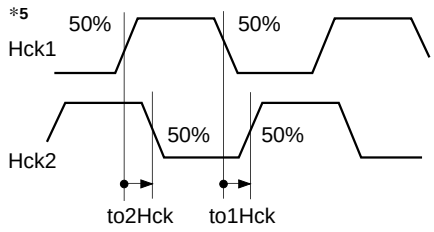
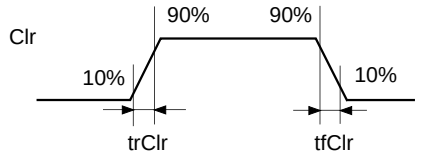
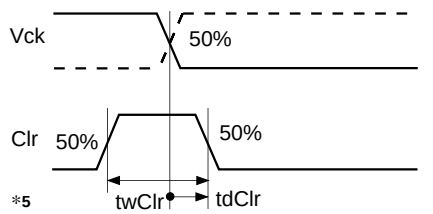
The LCX012BL has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to HV_{DD} or VV_{DD}. The V_{CC} of external ICs are applicable to 5 ± 0.5V.

2. Clock timing conditions (Ta = 25°C) (VGA mode: fHCKn = 2.5MHz, fVCK = 15.7kHz)

	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst	—	—	30	ns
	Hst fall time	tfHst	—	—	30	
	Hst data set-up time	tdHst	30	100	170	
	Hst data hold time	thHst	30	100	170	
HCK	Hckn rise time*4	trHckn	—	—	30	
	Hckn fall time*4	tfHckn	—	—	30	
	Hck1 fall to Hck2 rise time	to1Hck	–15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	–15	0	15	
CLR	Clr rise time	trClr	—	—	100	
	Clr fall time	tfClr	—	—	100	
	Vck rise/fall → Clr fall time	Tdclr	–100	0	100	
	Clr pulse width	twClr	2400	2500	2600	
VST	Vst rise time	trVst	—	—	100	
	Vst fall time	tfVst	—	—	100	
	Vst data set-up time	tdVst	5	15	25	µs
	Vst data hold time	thVst	5	15	25	
VCK	Vck rise time	trVck	—	—	100	ns
	Vck fall time	tfVck	—	—	100	
ENB	Enb rise time	trEnb	—	—	100	
	Enb fall time	tfEnb	—	—	100	
	Vck rise/fall to Enb rise time	toEnb	400	500	600	
	Enb pulse width	twEnb	2400	2500	2600	
PCG	Pcg rise time	trPcg	—	—	30	
	Pcg fall time	tfPcg	—	—	30	
	Pcg rise to Vck rise/fall time	toVck	500	800	1000	
	Pcg pulse width	twPcg	900	1000	1100	

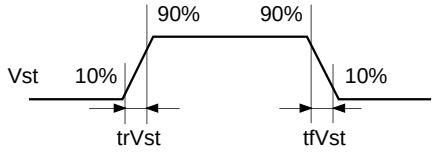
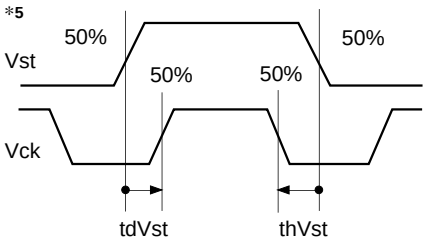
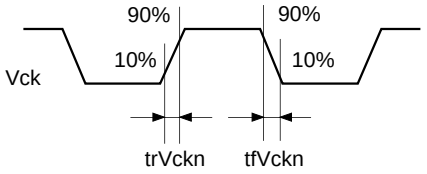
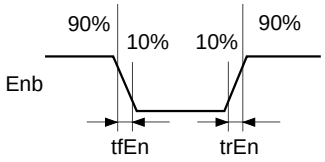
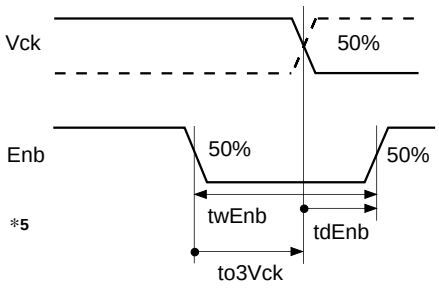
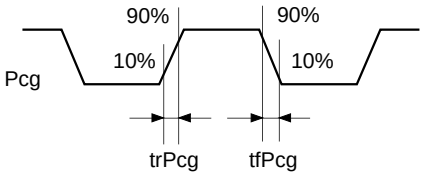
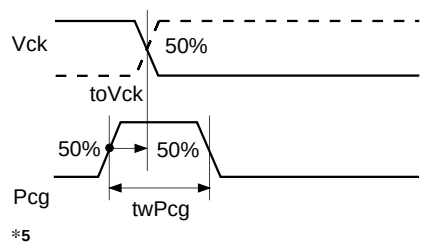
*4 Hckn means Hck1 and Hck2.

<Horizontal Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
HST	Hst rise time	trHst		O Hckn*4 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst fall time	tfHst		
	Hst data set-up time	tdHst		O Hckn*4 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst data hold time	thHst		
HCK	Hckn rise time*4	trHckn		O Hckn*4 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hckn fall time*4	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		
	Hck1 rise to Hck2 fall time	to2Hck		
CLR	Clr rise time	trClr		O Hckn*4 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Clr fall time	tfClr		
	Clr pulse width	twClr		
	Vck rise/fall → Clr fall time	tdClr		

*5 Definitions: The right-pointing arrow (•→) means +.
The left-pointing arrow (←•) means –.
The black dot at an arrow (•) indicates the start of measurement.

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
VST	Vst rise time	trVst		
	Vst fall time	tfVst		
	Vst data set-up time	tdVst		
	Vst data hold time	thVst		
VCK	Vck rise time	trVck		
	Vck fall time	tfVck		
ENB	Enb rise time	trEnb		
	Enb fall time	tfEnb		
	Vck rise/fall to Enb rise time	tdEnb		
	Enb pulse width	twEnb		
PCG	Pcg rise time	trPcg		
	Pcg fall time	tfPcg		
	Pcg rise to Vck rise/fall time	toVck		
	Pcg pulse width	twPcg		

Electrical Characteristics (Ta = 25°C, HV_{DD} = 15.5V, VV_{DD} = 15.5V)

1. Horizontal drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	HCKn	CHckn	—	10	15	pF	
	HST	CHst	—	10	15	pF	
Input pin current	HCK1		–500	–250	—	µA	HCK1 = GND
	HCK2		–1000	–300	—	µA	HCK2 = GND
	HST		–500	–150	—	µA	HST = GND
	RGT		–150	–25	—	µA	RGT = GND
Video signal input pin capacitance		Csig	—	100	150	pF	
Current consumption		IH	—	4.0	6.0	mA	HCKn: HCK1, HCK2 (2.5MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	VCK	CVck	—	10	15	pF	
	VST	CVst	—	10	15	pF	
Input pin current	VCK		–1000	–150	—	µA	VCK = GND
PCG, VST, ENB, CLR, DWN			–150	–25	—	µA	PCG, VST, ENB, CLR, DWN = GND
Current consumption		IV	—	2.0	3.0	mA	VCK: (15.7kHz)

3. Total power consumption of the panel

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (VGA)	PWR	—	100	150	mW

4. Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – V_{SS} input resistance	Rpin	0.4	1	—	MΩ

5. Uniformity improvement signal

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance for uniformity improvement signal	CPSIGon	—	6.5	7.0	nF

Electro-optical Characteristics (Ta = 25°C, VGA mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio		25°C	CR	1	150	250	—	—
Optical transmittance		25°C	T	2	22	25	—	%
V-T characteristics	V_{90}	25°C	RV_{90-25}	3	1.1	1.5	1.8	V
			GV_{90-25}		1.2	1.7	2.0	
			BV_{90-25}		1.3	1.8	2.1	
		60°C	RV_{90-60}		1.0	1.4	1.7	
			GV_{90-60}		1.1	1.5	1.8	
			BV_{90-60}		1.1	1.6	1.9	
	V_{50}	25°C	RV_{50-25}		1.5	1.9	2.2	
			GV_{50-25}		1.6	2.0	2.3	
			BV_{50-25}		1.7	2.1	2.4	
		60°C	RV_{50-60}		1.5	1.8	2.1	
			GV_{50-60}		1.5	1.9	2.2	
			BV_{50-60}		1.6	2.0	2.3	
	V_{10}	25°C	RV_{10-25}		2.0	2.4	2.7	
			GV_{10-25}		2.1	2.5	2.8	
			BV_{10-25}		2.1	2.5	2.8	
		60°C	RV_{10-60}		2.1	2.3	2.6	
			GV_{10-60}		2.1	2.4	2.7	
			BV_{10-60}		2.2	2.5	2.8	
Response time	ON time	0°C	ton0	4	—	36	80	ms
		25°C	ton25		—	14	40	
	OFF time	0°C	toff0		—	106	200	
		25°C	toff25		—	30	70	
Flicker		60°C	F	5	—	–74	–40	dB
Image retention time		25°C	YT60	6	—	0	0	s
Cross talk		25°C	CTK	7	—	—	5	%

Reflection Preventive Processing

When a phase substrate which rotates polarization axis is used to adjust to the polarization direction of polarization screen or prism, use the phase substrate with reflection preventive processed on the surface.
This prevents characteristic deterioration caused by luminous reflection.

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

HV_{DD} = 15.5V, VV_{DD} = 15.5V

VVC = 7.0V, Vcom = 6.6V

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of screen unless otherwise specified.

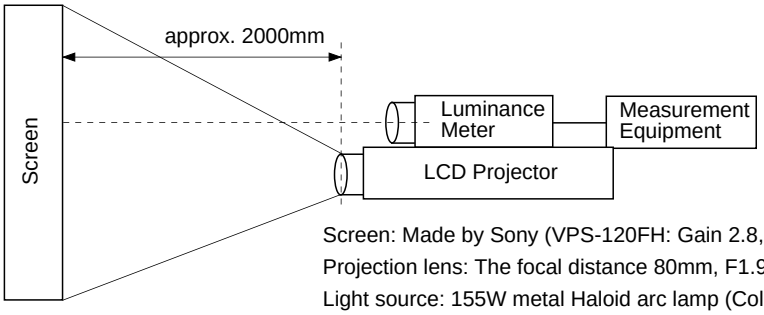
(4) Measurement systems

Two typed of measurement system are used as shown below.

(5) Video input signal voltage (Vsig)

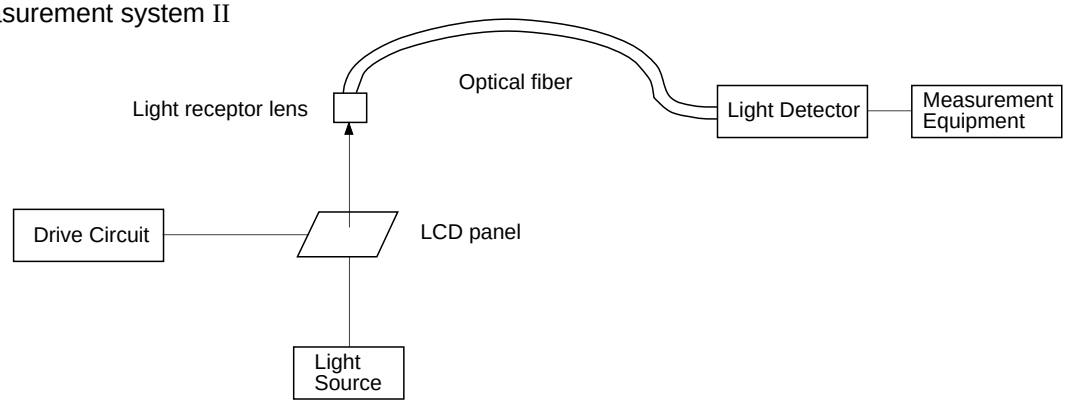
Vsig = 7.0 ±V_{AC} [V] (V_{AC}: signal amplitude)

• Measurement system I



Screen: Made by Sony (VPS-120FH: Gain 2.8, Glass Beaded Type) or an equivalent
Projection lens: The focal distance 80mm, F1.9
Light source: 155W metal Haloid arc lamp (Color temperature 7500K ± 500)
(× 24, Sensor area: 7mmϕ)
Polarizer: Nitto Denko's EG-1224DU or Polatechno's SKN-18242T or equivalent

• Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L\ (White)}{L\ (Black)} \cdots (1)$$

L (White): Surface luminance of the center of the screen at the input signal amplitude V_{AC} = 0.5V.

L (Black): Surface luminance of the center of the screen at V_{AC} = 4.5V.

Both luminosities are measured by System I.

2. Optical Transmittance

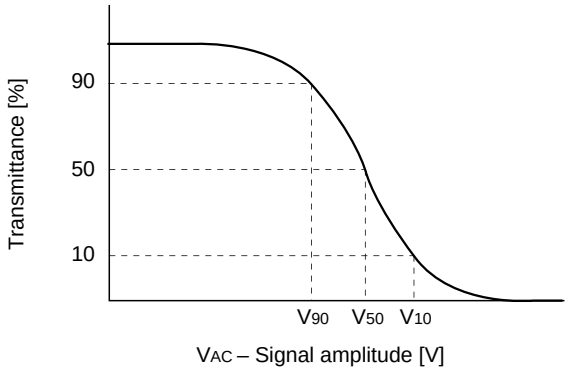
Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{\text{White luminance}}{\text{Luminance of light source}} \times 100\ [\%] \cdots (2)$$

"White luminance" means the maximum luminance at the input signal amplitude V_{AC} = 0.5V on Mesurement System II.

3. V-T Characteristics

V-T characteristics, the relationship between signal amplitude and the transmittance of the panels, are measured by System II. V_{90}, V_{50}, and V_{10} correspond to the each voltage which defines 90%, 50%, and 10% of transmittance respectively.



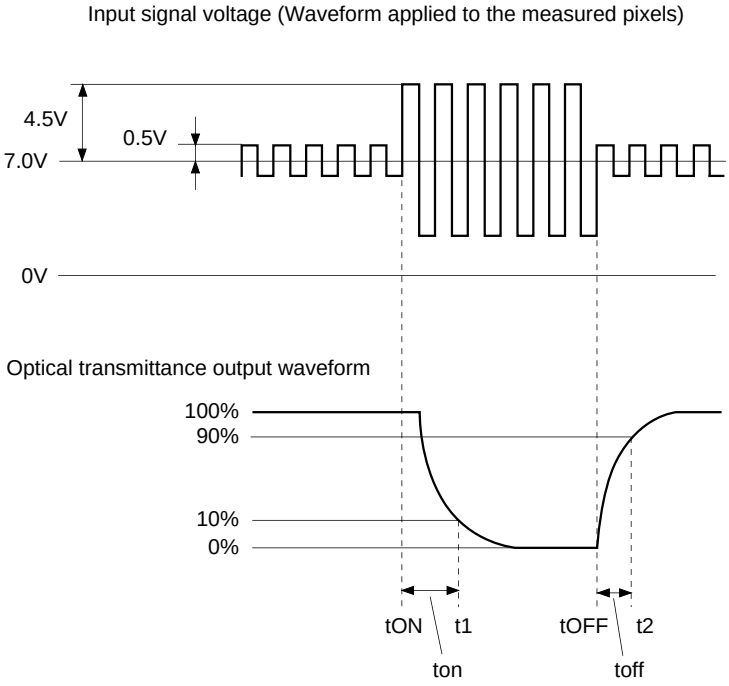
4. Respons Time

Response time ton and toff are defined by the formula (5) and (6) respectively.

ton = t1 – tON ··· (5)
toff = t2 – tOFF ··· (6)

t1: time which gives 10% transmittance of the panel.
t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the right figure.



5. Flicker

Flicker (F) is given by the formula (7). DC and AC (NTSC VGA: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analizer in System II.

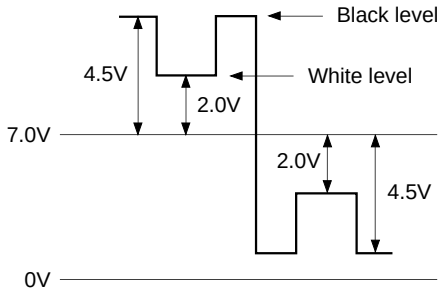
$$F\ [dB] = 20\log\left\{\frac{\text{AC component}}{\text{DC component}}\right\} \cdots (7)$$

* Each input signal condition for gray raster mode is given by
Vsig = 7.0 ± V_{50} [V]
where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T characteristics.

6 Image Retention Time

Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of Vsig = 7.0 ± V_{AC} (V_{AC}: 3 to 4V), judging by sight at V_{AC} that hold the maximum image retention, measure the time till the residual image becomes indistinct.

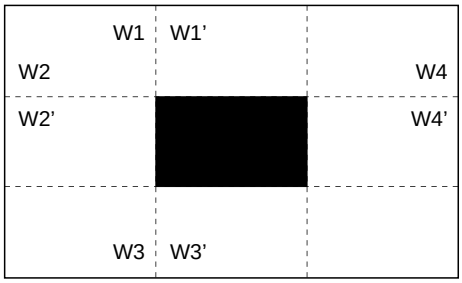
* Monoscope signal conditions:
Vsig = 7.0 ± 4.5 or ± 2.0 [V]
(shown in the right figure)
Vcom = 6.6V



Vsig waveform

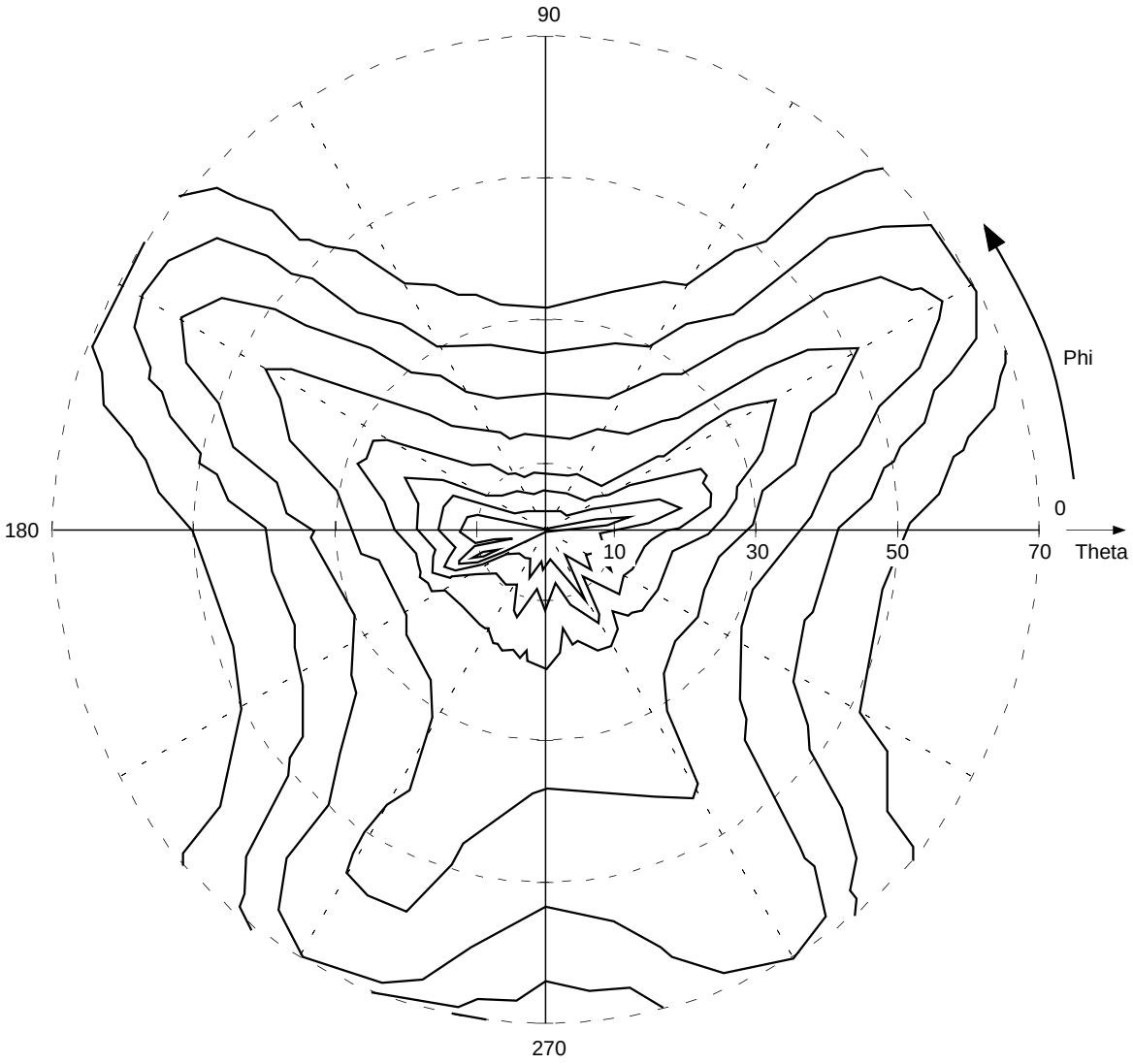
7. Cross Talk

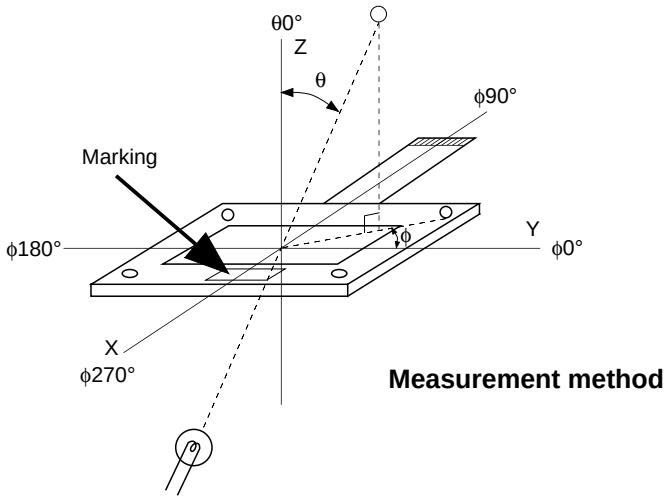
Cross talk is determined by the luminance differences between adjacent areas represented Wi' and Wi (i = 1 to 4) around black window (Vsig = 4.5V/1V)



$$\text{Cross talk value CTK} = \left|\frac{Wi' - Wi}{Wi}\right| \times 100\ [\%]$$

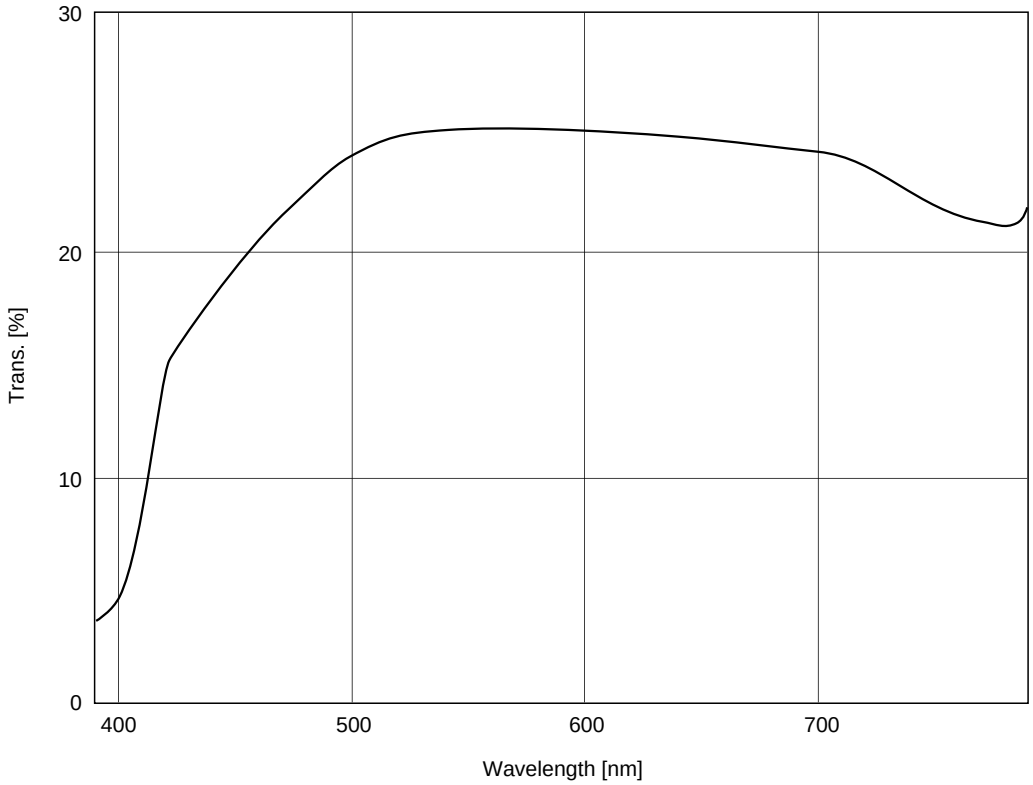
Viewing angle characteristics (Typical Value)





Measurement method

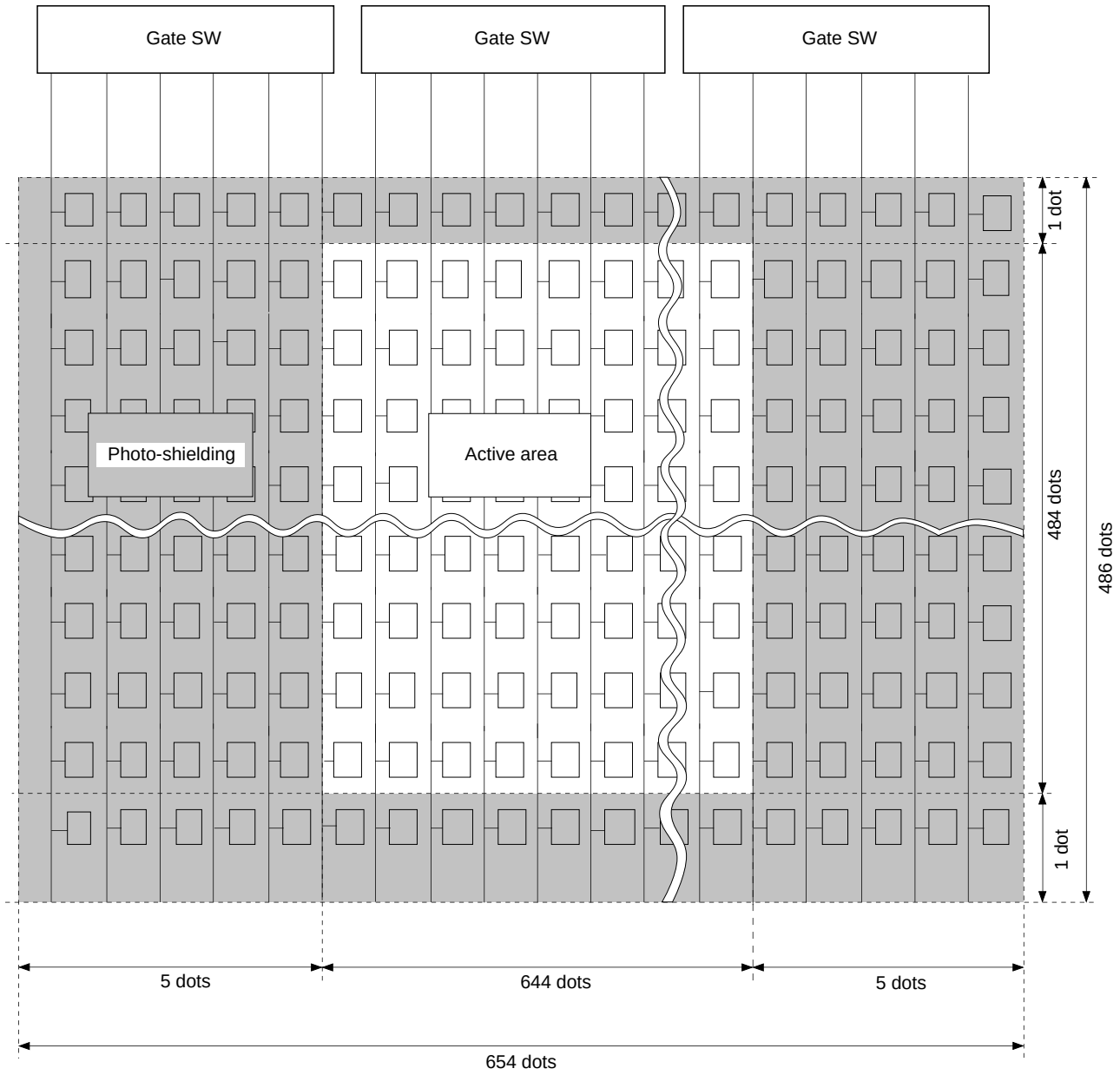
Optical transmittance of LCD panel (Typical Value)



Measurement method: Measurement system II

1. Dot Arrangement

The dots are arranged in a stripe. The shaded area is used for the dark border around the display.



2. LCD Panel Operations

[Description of basic operations]

The basic operations of the LCD panel are shown below based on the VGA mode.

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 484 gate lines sequentially in every horizontal scanning period. Two lines of horizontal electrodes are sequentially selected in NTSC/PAL mode.

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 644 signal electrodes sequentially in a single horizontal scanning period.

- Vertical and horizontal shift registers address one pixel, and then Thin film Transistors (TFTs; two TFTs) turn on to apply a video signal to the dot. The same procedures lead to the entire 484 × 644 dots to display a picture in a single vertical scanning period.

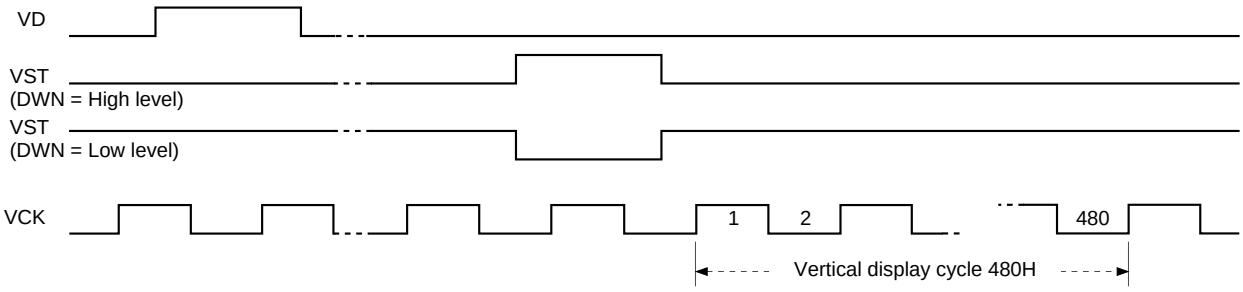
- To change the combination of the horizontal electrode in NTSC/PAL mode, the phase of VCK need to be inverted. Normally, switching every field maximizes vertical resolution.

- The CLR pin is provided to eliminate the shading effect caused by the coupling of selected pulses. While maintaining the CLR at High level, the VV_{DD} potential drops to approximately 9.5V. This pin shall be grounded when not in use.

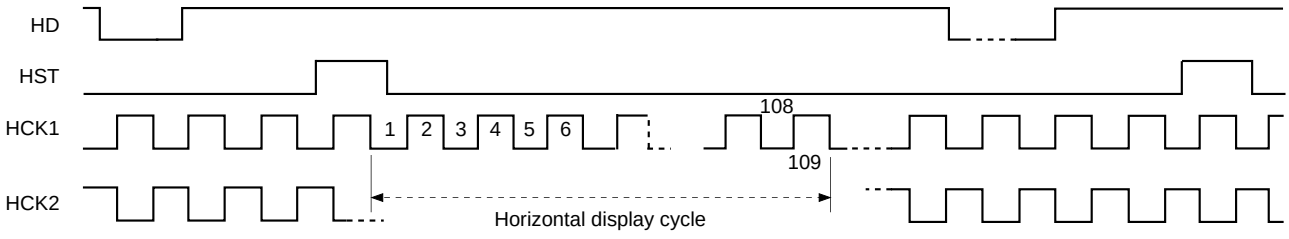
- The video signal shall be input with 1H-inverted system.

- Timing diagrams of the vertical for VGA mode and NTSC/PAL mode and the horizontal display cycle are shown below:

(1) Vertical display cycle (VGA)



(2) Horizontal display cycle



[Description of operating mode]

The LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode

These modes are controlled by two signals (RGT and DWN). The setting mode is shown below.

RGT	Mode
H	Right scan
L	Left scan

DWN	Mode
H	Down scan
L	Up scan

The direction of the right/left and/or up/down mean when Pin 1 marking is located at right side with the pin block upside.

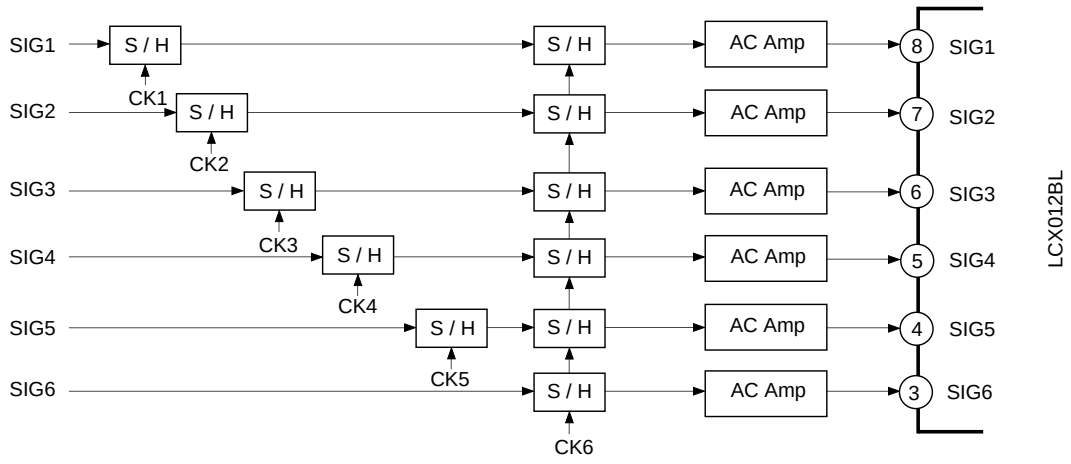
- To improve uniformity, the analog signals PSIG shall be input by synchronizing with SIG1 to SIG6.
- When the up-scan mode (DWN = Low level) is set, the phase of VST shall be inverted

3. 6-dot Simultaneous Sampling and Dot-inverted Drive

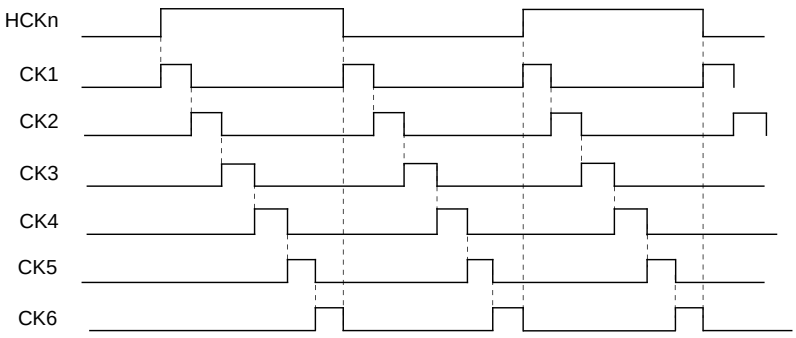
Horizontal driver samples SIG1 to SIG6 signal simultaneously. Which requires the phase matching between SIG1 to SIG6 signals to prevent horizontal resolution from deteriorating. Thus phase matching between each signal is required using an external signal delaying circuit before applying video signal to the LCD panel.

The block diagram of the delaying procedure using sample-and-hold method is as follows.

The following phase relationship diagram indicates the phase setting for the right scan (RGT = High level). For the left scan (RGT = Low level), the phase setting shall be inverted between SIG1 to SIG6 signals.

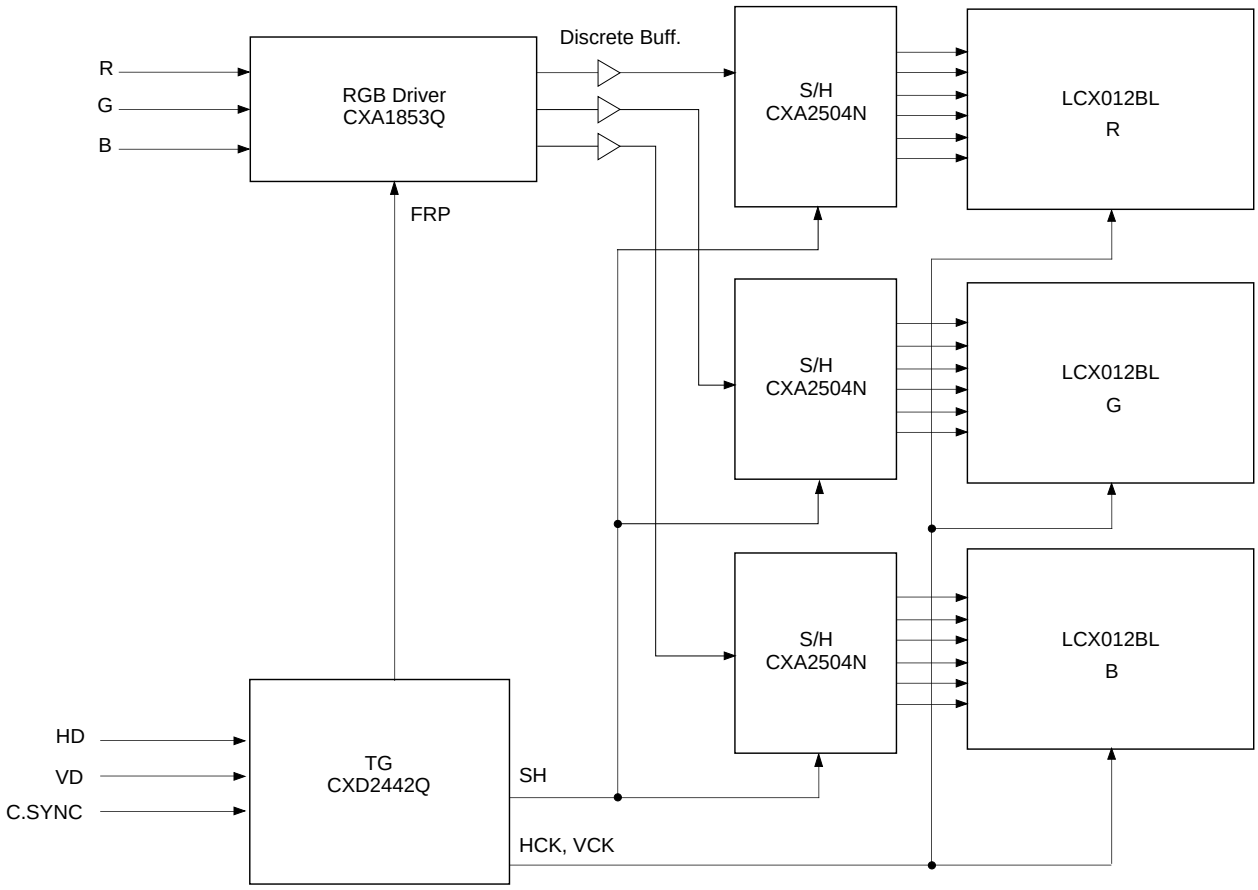


<Phase relationship of delaying sample-and-hold pulses> (right scan)



Display System Block Diagram

An example of display system is shown below.



Notes on Handling

(1) Static charge prevention

Be sure to take following protective measures. TFT-LCD panels are easily damaged by static charge.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install conductive mat on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionozed air to discharge the panels.

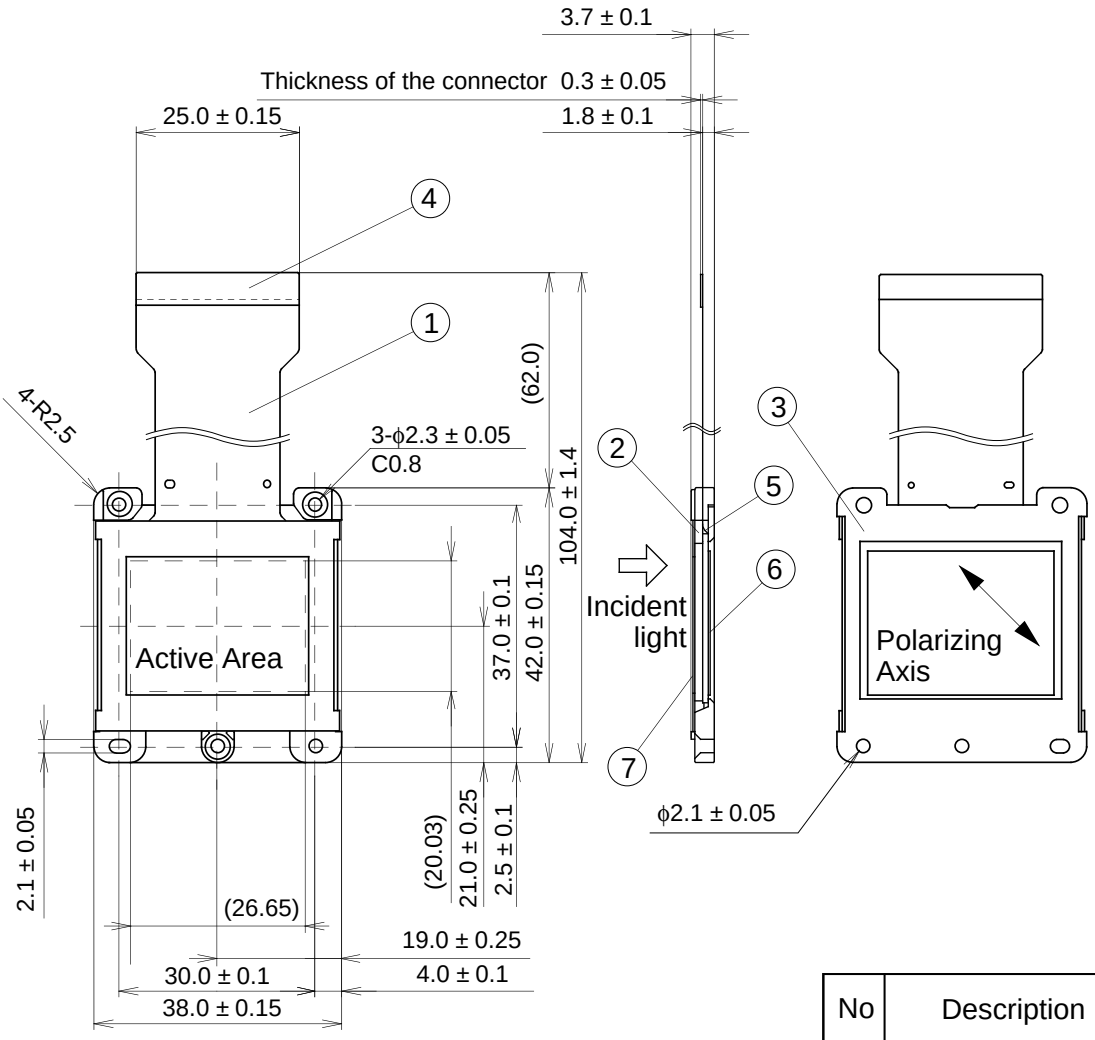
(2) Protection from dust and dirt

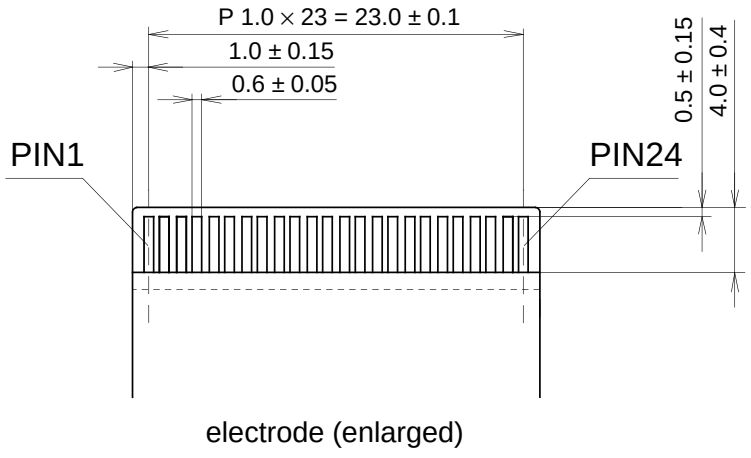
a) Operate in clean environment.
b) When delivered, a surface of a panel (Polarizer) is covered by a protective sheet.
Peel off the protective sheet carefully not to damage the panel.
c) Do not touch the surface of a panel. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stain on the surface.
d) Use ionized air to blow off dust at a panel.

(3) Other handling precautions

a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop a panel.
c) Do not twist or bend a panel or a panel frame.
d) Keep a panel away from heat source.
e) Do not dampen a panel with water or other solvents.
f) Avoid to store or to use a panel in a high temperature or in a high humidity, which may result in panel damages.
g) Minimum bent radius rating for flexible substrates is 1mm.
h) Panel screw torque should not exceed 3kg · cm.

Package Outline Unit: mm





electrode (enlarged)

No	Description
1	F P C
2	Molding material
3	Outside frame
4	Reinforcing board
5	Reinforcing material
6	Polarizing film
7	Cover

weight 7.5g

The rotation angle of the active area relative to H and V is ± 1°.