CMOS IC

SANYO : DIP30S



LC7536LHS

High-Voltage, Two-Channel Electronic Attenuator

[LC7536LHS]

27.2

Package Dimensions

unit:mm

3061-DIP30S

Overview

The LC7536LHS is a two-channel electronic attenuator for volume, balance and loudness controls in stereo audio applications.

The LC7536LHS reads data from a three-line serial bus to control attenuation in 1 dB steps over an 80 dB range, up to a maximum of 96 dB. It features a center tap at 20 dB attenuation for a loudness control using a minimum of external components. A device select pin allows two devices to be connected to the serial bus.

The LC7536LHS operates from 5 V and 10 V supplies and is available in 30-pin DIPs.

Features

- Three-line serial control.
- Two device select.
- Tap at 20 dB attenuation for a loudness control.
- 80 dB attenuation range adjustable in 1 dB steps.
- 96 dB maximum attenuation.
- 75 dB crosstalk rejection.
- 0.022% total harmonic distortion.
- $47k\Omega$ input impedance.
- 5 V and 10 V supplies.
- 30-pin DIP.

Specifications

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V, V_{EE}=0V

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Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max		0 to 12	v
Maximum supply voltage	V _{CC} max		0 to 7	
CLK, DI and CE input voltage range	V _{I1}		0 to V _{CC} +0.3	V
Analog input voltage range	V _{I2}		V _{EE} -0.3 to V _{DD} +0.3	V
Select pin input voltage range	VI3		V _{CC} -0.3 to V _{DD} +0.3	V
Allowable power dissipation	Pd max	Ta≤85°C	250	mW
Operating temperature range	T _{opr}		-40 to +85	°C
Stroage temperature range	T _{stg}		-50 to +125	°C

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Recommended Operating Conditions at Ta = 25 $^{\circ}C,$ V $_{SS}$ = 0 V, V $_{EE}$ = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Analog supply voltage	V _{DD}		V _{CC} +3.2 to 10.0	V
Logic supply voltage	V _{CC}		5	V
Logic supply voltage	VCC		3.6 to 5.5	V

Electrical Characteristics at Ta = 25 °C, V_{CC} = 5 V, V_{DD} = 10 V, V_{EE} = 0 V, V_{SS} = 0 V

Parameter	Symbol	Conditions		Ratings			
Parameter	Symbol	Symbol		typ	max	Unit	
Supply current	IDD				1	mA	
Supply current	ICC				1	IIIA	
Serial bus HIGH-level input voltage	V _{IH1}		0.8V _{CC}		VCC	V	
Select pin HIGH-level input voltage	V _{IH2}		0.8× (V _{DD} -V _{CC}) +V _{CC}		V _{DD}	V	
Serial bus LOW-level input voltage	V _{IL1}		V _{SS}		0.2V _{CC}	V	
Select pin LOW-level input voltage	V _{IL2}		Vcc		0.2× (V _{DD} -V _{CC}) +V _{CC}	V	
Input voltage	VIN		VEE		V _{DD}	V _{P-P}	
Input pulsewidth	t _{ΦW}		20			μs	
Setup time	^t setup		20			μs	
Hold time	^t hold		20			μs	
Operating frequency	fopg				25	kHz	
Output leakage current	IOFF	Analog switches OFF	-10		+10	μA	
Total harmonic distortion	THD	V _{IN} =0.3V, f=1kHz, V _{DD} -V _{EE=10V} , V _{R=} V _{R(max)}		0.022		%	
Crosstalk rejection	Cr	f=20kHz, V _{IN} =1V	60	75		dB	
Maximum attenuation	V ₀	f=20kHz, V _{IN} =1V		96		dB	

Pin Assignment



Block Diagram



Pin Description

Number	Name	Description
1	L5dBIN	Left-channel 5 dB attenutaiton step input. Low-impedance drive. 75 k Ω total resistance.
2	NC	No connection
3	LCT1	
4	LCT2	- Left-channel loudness compensation inputs.
5	L5dBOUT	Left-channel 5 dB attenutaiton step output. Approximately 1 M Ω load resistance.
6	L1dBIN	Left-channel 1 dB attenutaiton step input. Low-impedance drive.
7	NC	No connection
8	L1dBOUT	Left-channel 1 dB attenutaiton step output. 47 k Ω to 1 M Ω load resistance.
9	LVM	Left-channel volume control common. Normally connected to ground.
10	VEE	Ground
11	NC	No connection
12	S	Address select input.
13	V _{DD}	10 V supply
14	V _{SS}	Ground
15	NC	No connection
16	NC	
17	CLK	Clock input.
18	D1	Serial data input.
19	CE	Chip enable input.
20	NC	No connection
21	V _{CC}	5 V supply
22	RVM	Right-channel volume control common. Normally connected to ground.
23	R1dBOUT	Right-channel 1 dB attenutation step otuput. 47 k Ω to 1 M Ω load resistance.
24	NC	No connection
25	R1dBIN	Right-channel 1 dB attenutaiton step input. Low-impedance drive.
26	R5dBOUT	Right-channel 5 dB attenutaiton step output. Approximately 1 M Ω load resistance.
27	RCT2	Right-channel loudness compensation inputs.
28	RCT1	
29	NC	No connection
30	R5dBIN	Right-channel 5 dB attenutaiton step input. Low-impedance drive. 75 k Ω total resistance.

Timing



Functional Description

Data Control

Data is clocked into a 20-bit shift register. When 20 bits have been received, the data is latched and then passed to a level shifter.

Data Format

The 20-bit data word comprises a 4-bit address code, two 4-bit 5 dB attenuation step selectors, two 3-bit 1 dB attenuation step selectors and a loudness control ON/OFF bit as shown in figure 1.



Figure 1. Data format

The voltage on the select input determines the address of the device as shown in table 1. Table 1. Address codes

Select pin	A0	A1	A2	A3
V _{DD}	1	0	0	1
V _{CC}	0	0	0	1

Data bits D0 to D3 select the right-channel attenuation in 5 dB steps as shown in table 2. Similarly, bits D8 to D11 select the left-channel attenuation in 5 dB steps. Table 2. Right-channel 5 dB steps

Attenuation(dB)	D0	D1	D2	D3
0	1	1	1	1
5	0	1	1	1
10	1	0	1	1
15	0	0	1	1
20	1	1	0	1
25	0	1	0	1
30	1	0	0	1
35	0	0	0	1
40	1	1	1	0
45	0	1	1	0
50	1	0	1	0
55	0	0	1	0
60	1	1	0	0
65	0	1	0	0
70	1	0	0	0
75	0	0	0	0

Data bits D4 to D6 select the right-channel attenuation in 1 dB steps as shown in table 3. Similarly, bits D12 to D14 select the left-channel attenuation in 1 dB steps. Table 3. Right-channel 1 dB steps

Attenuation(dB)	D4	D5	D6
0	0	1	1
1	1	0	1
2	0	0	1
3	1	1	0
4	0	1	0
~	0	0	0

Data bits D7 selects loudness control. When D7 is 1, loudness control is ON, and when 0, loudness control is OFF.

Audio Signal

The right-channel audio input signal is input on R5dBIN(5 dB attenuation steps). The output, R5dBout, is fed back to R1dBIN (1 dB attenuation steps). The right-channel audio output is on R1dBOUT. The left-channel audio signal flow is identical.

Typical Application



Figure 2. Typical application

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