# IRF540

*Product Preview*

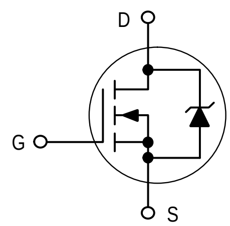
# TMOS E-FET™ Power Field Effect Transistor

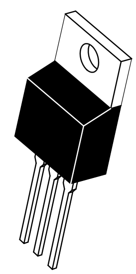
## N–Channel Enhancement–Mode Silicon Gate

**TMOS POWER FET**
**27 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 0.070 OHMS**

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters, and PWM motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature



**CASE 221A–09**
**TO-220AB**

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–to–Source Voltage — Continuous<br>— Non–repetitive ($t_p \le$ 10 ms) | $V_{GS}$<br>$V_{GSM}$ | ±20<br>±40 | Vdc<br>Vpk |
| Drain Current — Continuous<br>— Continuous @ 100°C<br>— Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 27<br>19<br>95 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 145<br>1.16 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy — STARTING $T_J$ = 25°C<br>($V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vdc, PEAK $I_L$ = 27 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 365 | mJ |
| Thermal Resistance — Junction–to–Case<br>— Junction–to–Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 0.86<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

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REV 3

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 100 | — | — | Vdc |
| Temperature Coefficient (Positive) | | | — | 116 | — | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | — | — | 10 | μAdc |
| ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | — | — | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | — | — | 100 | nAdc |
| **ON CHARACTERISTICS(1)** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | Cpk ≥ 2.0(3) | $V_{GS(th)}$ | 2.0 | 2.9 | 4.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | — | 6.8 | — | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 15 Adc) | Cpk ≥ 2.0(3) | $R_{DS(on)}$ | — | 0.047 | 0.070 | Ohms |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 27 Adc) | | $V_{DS(on)}$ | — | — | 1.9 | Vdc |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 15 Adc, $T_J$ = 125°C) | | | — | — | 1.8 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 15 Adc) | | $g_{FS}$ | 6.0 | 15 | — | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | — | 1460 | 1600 | pF |
| Output Capacitance | | $C_{oss}$ | — | 390 | 800 | |
| Transfer Capacitance | | $C_{rss}$ | — | 120 | 300 | |
| **SWITCHING CHARACTERISTICS(2)** | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 4.7 Ω) | $t_{d(on)}$ | — | 11.6 | 30 | ns |
| Rise Time | | $t_r$ | — | 50 | 60 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | — | 26 | 80 | |
| Fall Time | | $t_f$ | — | 19 | 30 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 80 Vdc, $I_D$ = 27 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | — | 50 | 60 | nC |
| | | $Q_1$ | — | 9.0 | — | |
| | | $Q_2$ | — | 26 | — | |
| | | $Q_3$ | — | 20 | — | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage ($I_S$ = 27 Adc, $V_{GS}$ = 0 Vdc) | | $V_{SD}$ | — | 0.93 | 2.4 | Vdc |
| ($I_S$ = 27 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | — | 0.84 | — | |
| Reverse Recovery Time | ($I_S$ = 27 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | — | 110 | — | ns |
| | | $t_a$ | — | 100 | — | |
| | | $t_b$ | — | 10 | — | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | — | 0.67 | — | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the contact screw on tab to center of die) | | $L_d$ | — | 3.5 | — | nH |
| (Measured from the drain lead 0.25″ from package to center of die) | | | — | 4.5 | — | |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_s$ | — | 7.5 | — | |

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $Cpk = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{sigma}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

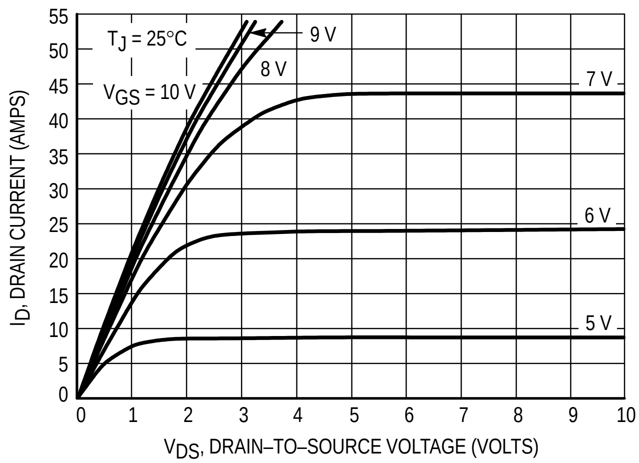



**Figure 1. On–Region Characteristics**

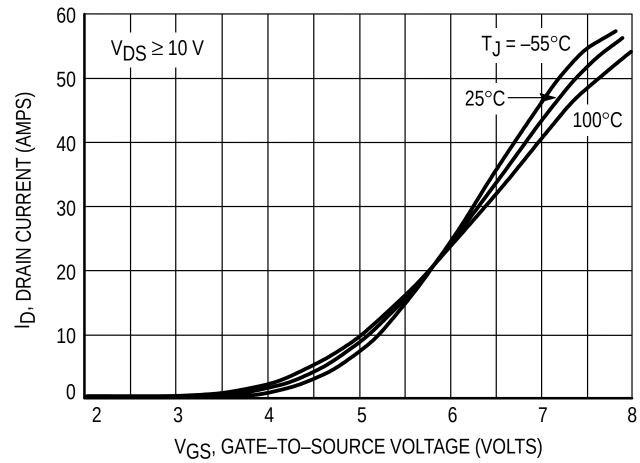



**Figure 2. Transfer Characteristics**

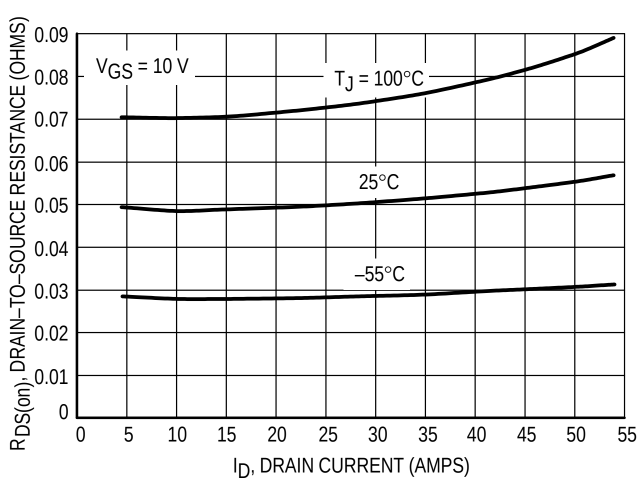



**Figure 3. On–Resistance versus Drain Current and Temperature**

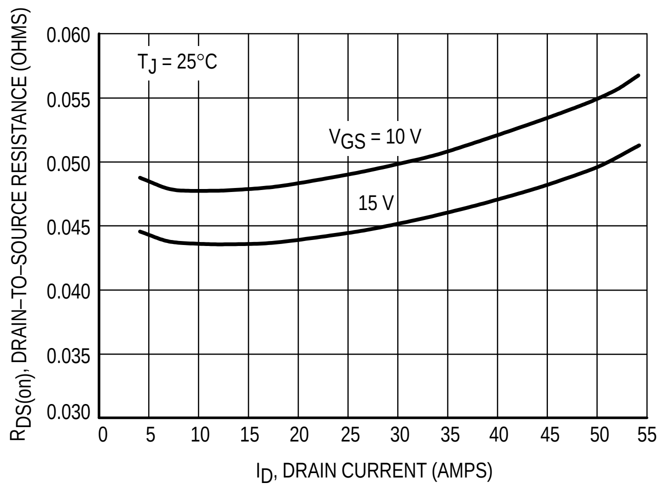



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

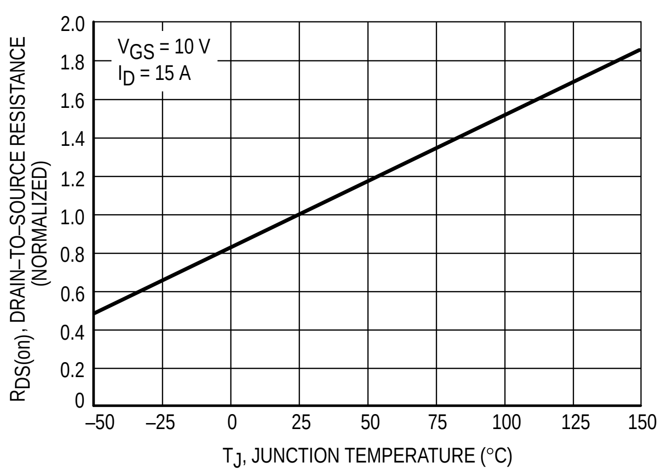



**Figure 5. On–Resistance Variation with Temperature**

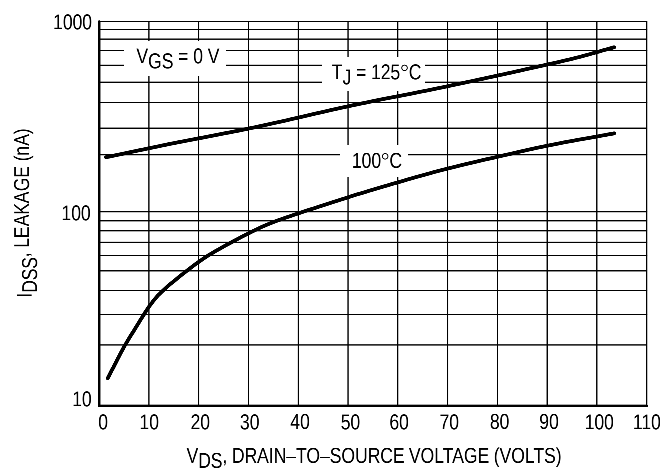



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## TYPICAL ELECTRICAL CHARACTERISTICS

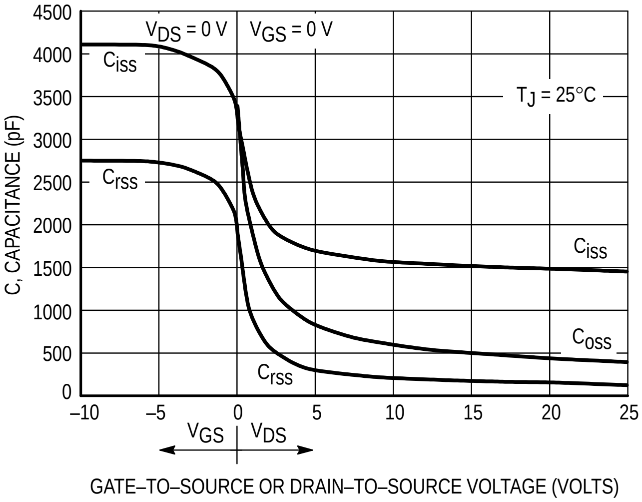



**Figure 7. Capacitance Variation**

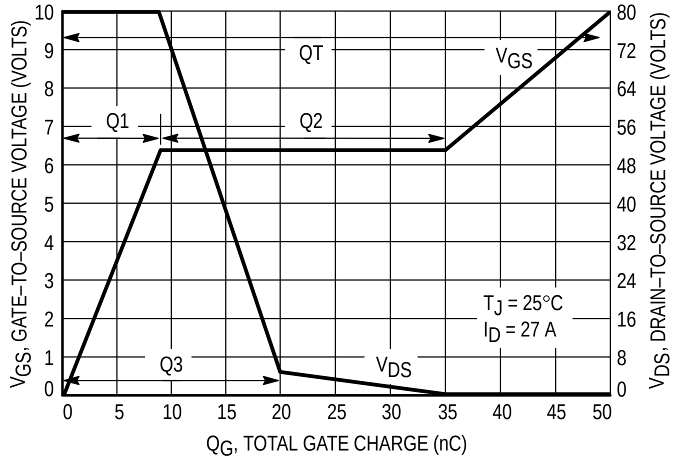



**Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

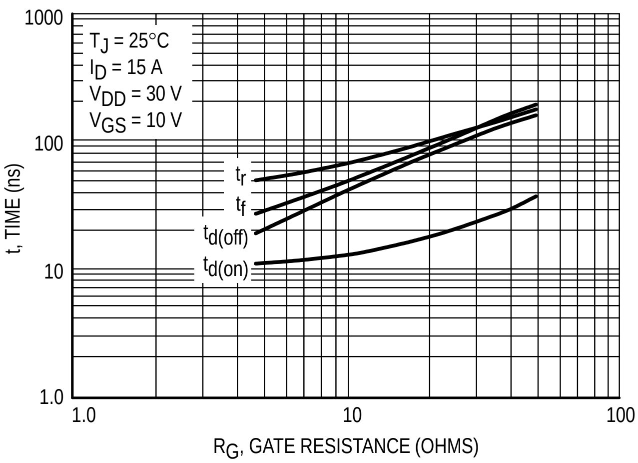



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

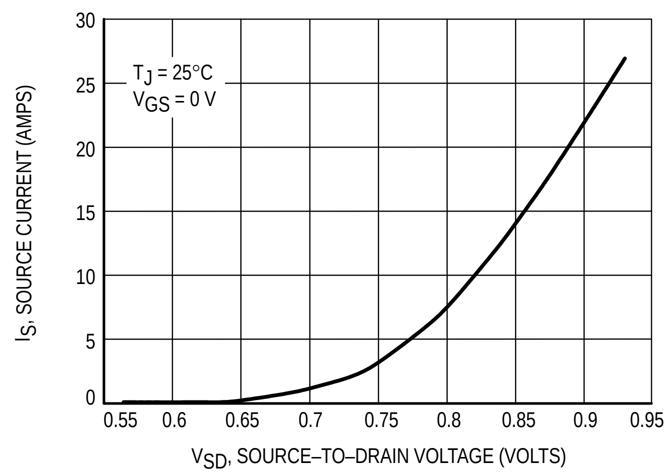



**Figure 10. Diode Forward Voltage versus Current**

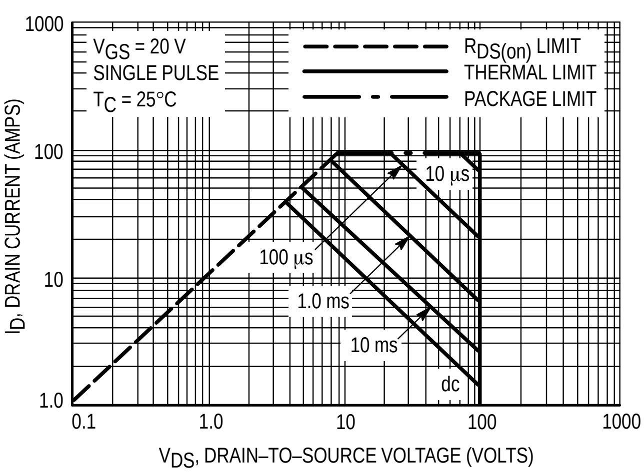



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

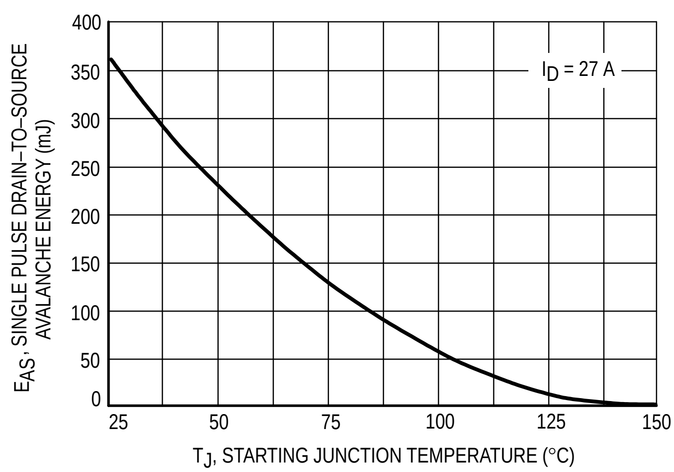



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

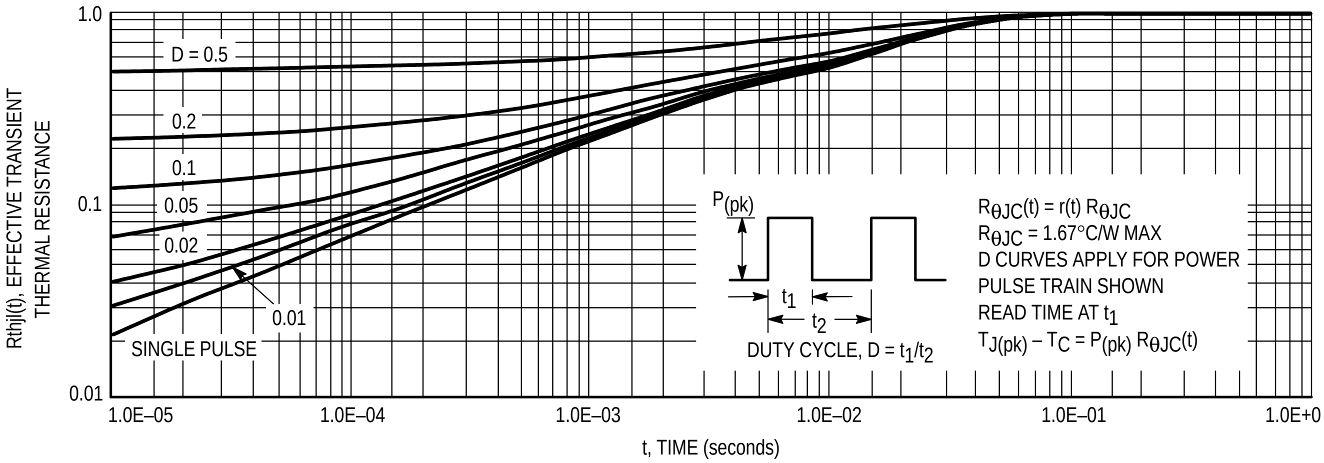
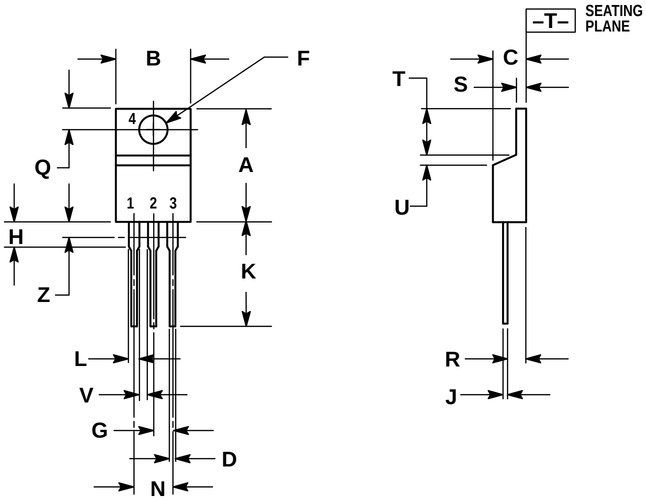



**Figure 13. Thermal Response**

## PACKAGE DIMENSIONS




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.405 | 9.66 | 10.28 |
| C | 0.160 | 0.190 | 4.07 | 4.82 |
| D | 0.025 | 0.035 | 0.64 | 0.88 |
| F | 0.142 | 0.147 | 3.61 | 3.73 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.155 | 2.80 | 3.93 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.39 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | — | 1.15 | — |
| Z | — | 0.080 | — | 2.04 |

**CASE 221A–09**
**(TO–220AB)**
**ISSUE Z**



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