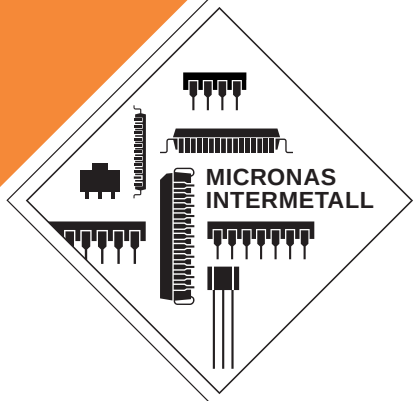

DMA 2271,
DMA 2280,
DMA 2281
C/D/D2–MAC Decoder

Edition August 5, 1991
6251–331–1E

MICRONAS
INTERMETALL

Contents

The DMA 2271, DMA 2280, and DMA 2281 C/D/D2–MAC Decoders

1. Introduction

1.1. General Information

Digital real–time signal processor for processing C/D/D2–MAC video, sound, and data signals digitized by the VCU 2133 Video Codec in digital CTV receivers according to the DIGIT 2000 system of ITT or in analog CTV receivers or in stand–alone C/D/D2–MAC decoders (see Figs. 1–1 to 1–3).

In order to receive TV channels transmitted via satellite or cable network using the newly established C/D/D2–MAC standards instead of PAL or SECAM, decoders are required for decoding the TV video and sound signals. The DMA 2271, DMA 2280, and DMA 2281 are suitable for this purpose, in conjunction with the DIGIT 2000 digital TV system and also for stand–alone solutions.

The DMA 2271 is only able to decode D2–MAC/packet signals, in contrast to the DMA 2280 which decodes D–MAC/packet signals and the DMA 2281 which decodes D2, D or C–MAC/packet signals.

The DMA 2271, DMA 2280, and DMA 2281 are a programmable circuits, produced in CMOS technology and housed in a 68–pin PLCC package. These decoders contain on a single silicon chip the following functions (see Fig. 1–4):

– code converter
– circuitry for clamping, AGC and PLL
– chroma and luma store for expansion of the MAC signal
– chroma and luma interpolating filter
– contrast multiplier with limiter for the luminance signal
– color saturation multiplier with multiplexer
– duobinary decoder (data slicer)
– synchronization
– descrambler and de–interleaver
– packet linker
– packet 0 buffer
– sound decoder and sound multiplexer
– IM bus interface circuit for communicating with the CCU

1.2. Environment

Fig. 1–1 shows the block diagram of a digital CTV receiver system DIGIT 2000, equipped with C/D/D2–MAC and Teletext, and suited for the PAL and SECAM standards. Stand–alone C/D/D2–MAC decoders are shown in Figs. 1–2 and 1–3. These two versions can either be integrated into analog CTV receivers, or can serve as stand–alone C/D/D2–MAC decoders.

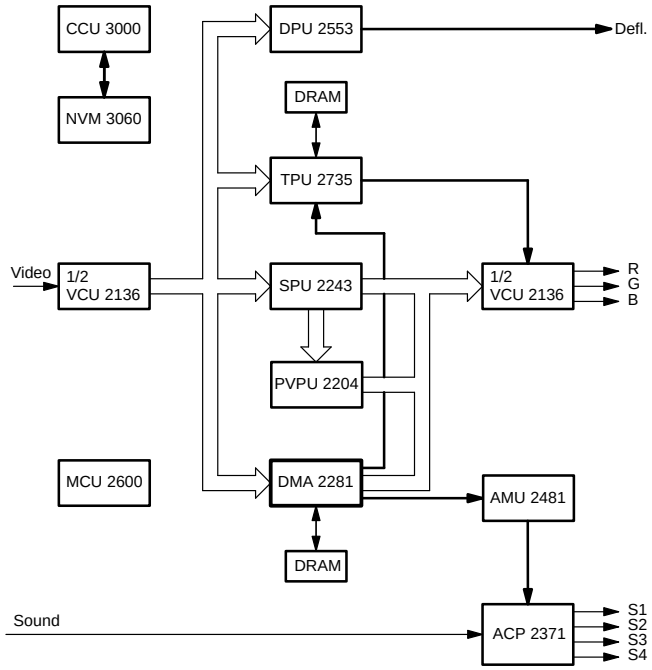

Fig. 1–1: Block diagram for a multistandard CTV receiver according to the DIGIT 2000 system and equipped with D2–MAC

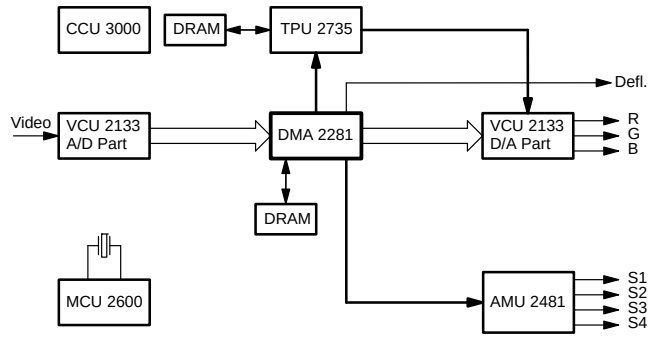

Fig. 1–2: Block diagram for a stand–alone C/D/D2–MAC decoder, equipped with the VCU 2133 Video Codec for A/D and D/A conversion (reduced chroma bandwidth)

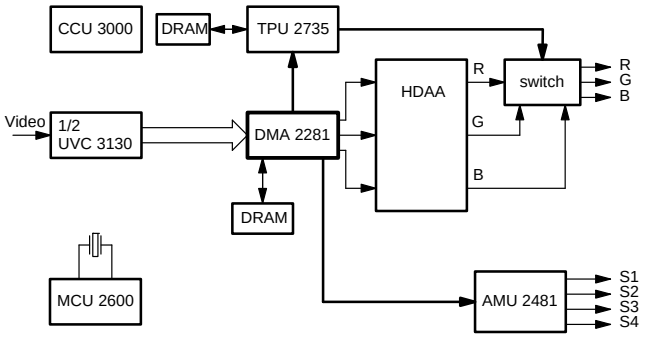

Fig. 1–3: Block diagram for a stand–alone C/D/D2–MAC decoder, equipped with the UVC 3130 for A/D and HDAA or D/A conversion (full chroma bandwidth)

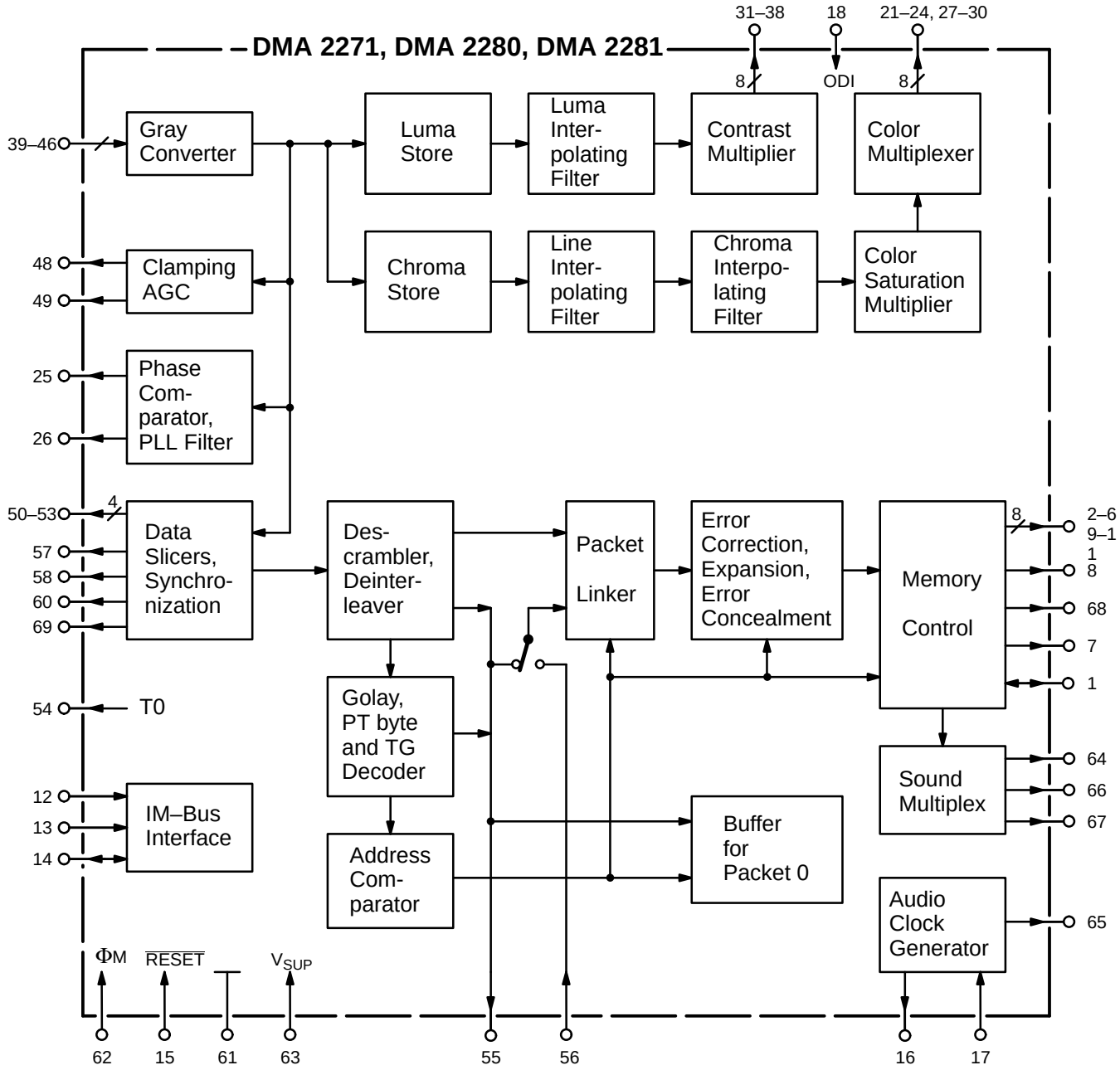

Fig. 1–4: Block diagram of the DMA 2271, DMA 2280, DMA 2281 C/D/D2–MAC decoders

2. Specifications

2.1. Outline Dimensions

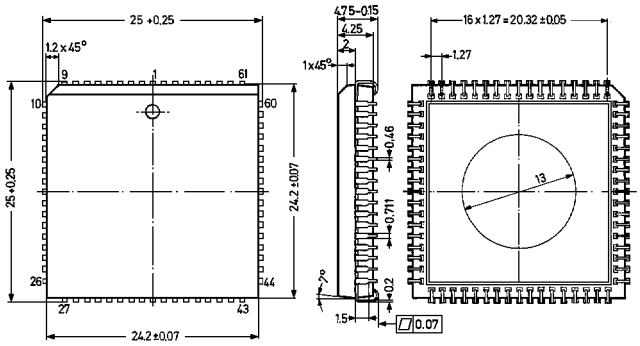

Fig. 2–1: DMA 2271, DMA 2280, DMA 2281 in 68–pin PLCC package

Weight approx. 4.5 g, Dimensions in mm

2.2. Pin Connections

Pin Nr.	Signal Name	Symbol
1	RAM Data Input/Output	RDAT
2	RAM Address Output 0 (LSB)	RA0
3	RAM Address Output 1	RA1
4	RAM Address Output 2	RA2
5	RAM Address Output 3	RA3
6	RAM Address Output 4	RA4
7	RAM Read/Write Output	R/WQ
8	Row Address Select Output	RASQ
9	RAM Address Output 5	RA5
10	RAM Address Output 6	RA6
11	RAM Address Output 7 (MSB)	RA7
12	IM Bus Clock Input	IMC
13	IM Bus Ident Input	IMI
14	IM Bus Data Input/Output	IMD
15	Reset Input	RESQ
16	18.432 MHz Output	XTAL1
17	18.432 MHz Input	XTAL2
18	Output Disable Input	ODI
19	leave vacant	
20	leave vacant	
21	Chroma Output 7 (MSB)	CO7
22	Chroma Output 6	CO6
23	Chroma Output 5	CO5
24	Chroma Output 4	CO4
25	PLL Tuning Data Output	PLLD
26	PLL Tuning Clock Output	PLLC
27	Chroma Output 3	CO3
28	Chroma Output 2	CO2
29	Chroma Output 1	CO1
30	Chroma Output 0 (LSB)	CO0
31	Luma Output 0	LO0
32	Luma Output 1	LO1
33	Luma Output 2	LO2
34	Luma Output 3	LO3
35	Luma Output 4	LO4
36	Luma Output 5	LO5
37	Luma Output 6	LO6
38	Luma Output 7 (MSB)	LO7
39	Baseband Input 7 (MSB)	BI7
40	Baseband Input 6	BI6
41	Baseband Input 5	BI5
42	Baseband Input 4	BI4
43	Baseband Input 3	BI3
44	Baseband Input 2	BI2
45	Baseband Input 1	BI1
46	Baseband Input 0 (LSB)	BI0
47	leave vacant	
48	Clamping Output	CLMP
49	AGC Output	AGC
50	Combined Output for Horizontal Blanking and Key	KEY

51	Combined Output for Horizontal and Vertical Blanking	CBL
52	Data Burst Window Output	DBW
53	Composite Sync Output	CSYNC
54	Test Input/Output	T0
55	Packet Data Output	PDAT
56	Descrambled Packet Data Input	DPDAT
57	Teletext Sync Output	TSYNC
58	Burst Sync Output	BSYNC
59	Burst Data Input/Output	BDAT
60	Burst Clock Output	BCLK
61	Ground	GND
62	Main Clock Input	MCLK
63	Supply Voltage	V_{SUP}
64	Sound Bus Ident Output	SBI
65	Audio Clock Output	ACLK
66	Sound Bus Data Output	SBD
67	Sound Bus Clock Output	SBC
68	Column Address Select Output	CASQ

2.3. Pin Descriptions

Pin 1 – RAM Data Input/Output RDAT (Fig. 2–7)
serves as an output for writing data into the external RAM and as an input for reading data from the external RAM.

Pins 2 to 6 and 9 to 11 – RAM Address Outputs RA0 to RA7 (Fig. 2–10)
These pins are used for addressing the external RAM.

Pin 7 – RAM Read/Write Output R/WQ (Fig. 2–10)
By means of this output the external RAM is switched to read or write mode.

Pin 8 – Row Address Select Output RASQ (Fig. 2–10)
This pin supplies the Row Address Select signal to the external RAM.

Pins 12 to 14 – IM Bus Connection IMC, IMI,IMD (Figs. 2–2 and 2–6)
These pins connect the DMA 2271, DMA 2280 and DMA 2281 to the IM bus. Via the IM bus the DMA 2271, DMA 2280 and DMA 2281 communicate with the CCU 3000 Central Control unit. The data transferred via the IM bus are listed in tables 4–1 to 4–4.

Pin 15 – Reset Input RESQ (Fig. 2–5)
Pin 15 is used for hardware reset. Reset is actuated at Low level, at High level the DMA 2271, DMA 2280, and DMA 2281 are ready for operation.

Pins 16 and 17 – XTAL 1 Output and XTAL 2 Input (Fig. 2–11)
These oscillator pins are used to connect an 18.432 MHz crystal, which determines the ACLK audio clock signal supplied by pin 65. Alternatively, an 18.432 MHz clock may be fed to pin 17.

Pin 18 – Output Disable Input ODI
This input serves for fast switchover of the luma and chroma outputs (L0 to L7 and C0 to C7) to high impedance, which is required if the TV receiver is equipped with Picture–in–picture. Low means outputs active, High means outputs are disabled.

Pin 19 – leave vacant

Pin 20 – leave vacant

Pins 21 to 24 and 27 to 30 – Chroma Outputs C7 to C0 (Fig. 2–8)
Via these pins, the DMA 2271, DMA 2280, and DMA 2281 deliver the digital chrominance signal (R–Y, B–Y) in multiplexed operation to the VCU 2133 Video Codec Unit, where it is converted to an analog signal.

Pin 25 – PLL Tuning Data Output PLLD (Fig. 2–8)
This pin supplies the 12–bit data word containing the PLL tuning information from the PLL filter of the DMA 2271, DMA 2280, and DMA 2281. This information is needed by the voltage controlled oscillator (VCO) contained on the MCU 2600 Clock Generator IC and closes the PLL which determines the main clock signal.

Pin 26 – PLL Tuning Clock Output PLLC (Fig. 2–8)
This pin supplies the data clock signal needed for the serial data transfer of the 12–bit PLL tuning information.

Pins 31 to 38 – Luma Outputs L0 to L7 (Fig. 2–8)
Via these pins, the DMA 2271, DMA 2280 and DMA 2281 deliver the digital luminance signal to the VCU 2133 Video Codec Unit, where it is converted to an analog signal.

Pins 39 to 46 – Baseband Input BI7 to BI0 (Fig. 2–3)
Via these inputs, the DMA 2271, DMA 2280, and DMA 2281 receive the digitized baseband signal from the VCU 2133 Video Codec.

Pin 47 – leave vacant

Pin 48 – Clamping Output CLMP (Fig. 2–9)
This pin supplies a PDM (Pulse Density Modulated) signal for clamping the analog baseband signal at the input of the analog to digital converter.

Pin 49 – AGC Output AGC (Fig. 2–9)
This tristate–controlled output allows automatic gain control (AGC) with a three–level signal. High level means that the input level of the baseband signal is too low, low level means that the input level of the baseband signal is too high. In the high impedance state the level of the baseband signal is in the proper range.

Pin 50 – Combined Output for Horizontal Blanking and Color KEY (Fig. 2–9)
This output is a tristate–controlled output. In conjunction with the input load represented by the VCU 2133 Video codec, the three level blanking and key is produced. High level means active line, high impedance state means horizontal blank and low level means color key.

Pin 51 – Combined Output for Horizontal Blanking and Vertical Blanking CBL (Fig. 2–9)
In conjunction with the input load represented by the VCU 2133 Video Codec, the three level combined blanking pulse is produced. High level means active line, high impedance means horizontal blanking and low level means vertical blanking.

Pin 52 – Data Burst Window DBW (Fig. 2–9)
This output supplies the data burst window signal which can be used to switch an external de–emphasis network. This signal is active high in line 625 and during the data burst in each line.

Pin 53 – Composite Sync Output CSYNC (Fig. 2–8)
This output supplies a composite synchronization signal as it may be used by the DPU 25xx Deflection Processor or by other units which need a composite synchronization signal which is not contained in the MAC baseband signal.

Pin 54 – Test Input/Output T0 (Fig. 2–8)
This pin is used for testing the DMA 2271, DMA 2280, and DMA 2281 during production.

Pin 55 – Packet Data Output PDAT (Fig. 2–10)
PDAT is used to put out each received packet, de–interleaved, with Golay corrected header and with error–corrected BT Byte. This pin used to connect the DMA 2275, DMA 2285 or DMA 2286 Descrambler IC.

Pin 56 – Descrambled Packet Data Input DPDAT (Fig. 2–2)
This pin is used in conjunction with PDAT, if conditional access signals must be descrambled, DPDAT receives the descrambled packet data from the DMA 2275, DMA 2285 or DMA 2286 Descrambler IC.

Pin 57 – Teletext Sync Output TSYNC (Fig. 2–9)
This pin supplies a signal which marks the part of the VBI lines containing Teletext data.

Pin 58 – Burst Sync Output BSYNC (Fig. 2–4)
This connection supplies a synchronization signal for the Burst Data Output. The Sync Pulse marks the Line Synchronization Word LWS of each, and the Clock Run In CRI and Frame Sync Word FSW in line 625.

Pin 59 – Burst Data Output BDAT (Fig. 2–4)
This output supplies the recovered an decoded duobinary data contained in a MAC signal. This signal may serve as an input signal for the TPU 27xx Teletext Processor or the DMA 2275, DMA 2285, DMA 2286 MAC Descrambler processor or for other purposes.

Pin 60 – Burst Clock Output BCLK (Fig. 2–9)
This pin supplies the data clock signal required for the serial data transfer of the Burst Data signal. The frequency of this signal is equal MCLK or MCLK/2 controlled by parameter Data Rate Select DRS via IM Bus.

Pin 61 – Ground GND

Pin 62 – Main Clock Input MCLK (Fig. 2–4)
By means of this input, the DMA 2271, DMA 2280 and DMA 2281 receive the required main clock signal from the MCU 2600 Clock Generator IC.

Pin 63 – Supply V_{SUP}

Pin 64, 66, and 67 – Sound Bus Ident SBI (Fig. 2–9) Data SBD and Clock SBC (Fig. 2–8)
These pins supply the Clock, Data and Ident signals to the AMU 2481 Mixing Unit via the serial three–line Sound Bus.

Pin 65 – Audio Clock Output ACLK (Fig. NO TAG)
This pin supplies the ACLK Audio Clock signal for the AMU 2481.

Pin 68 – Column Address Select CASQ (Fig. 2–10)
This pin supplies the Column Address Select signal for the external RAM.

2.4. Pin Circuits

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter “P” means P–channel, the letter “N” N–channel.

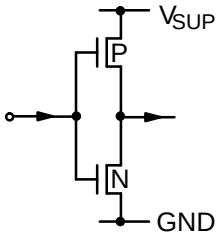

Fig. 2–2:
Input Pins 12, 13, 18 and 56

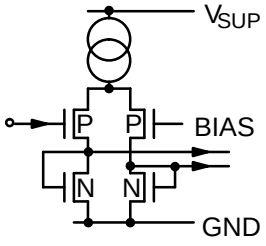

Fig. 2–3:
Input Pins 39 to 46

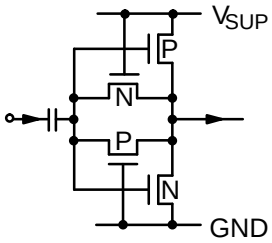

Fig. 2–4:
Input Pin 62

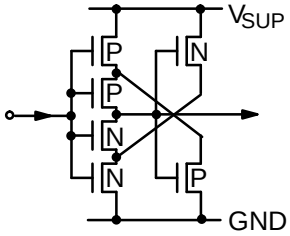

Fig. 2–5:
Input Pin 15

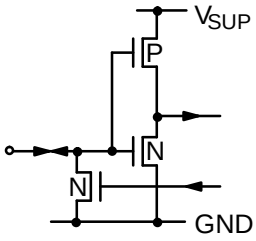

Fig. 2–6:
Input/Output Pin 14

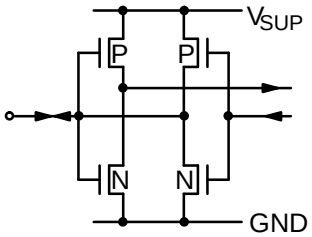

Fig. 2–7:
Input/Output Pin 1

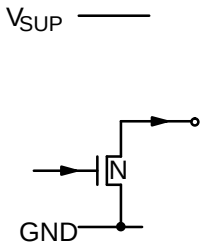

Fig. 2–8:
Output Pins 21 to 38, 48, 52 to 54, 66 and 67

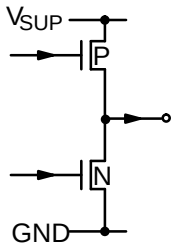

Fig. 2–9:
Output Pins 48 to 52, 57 to 60 and 64

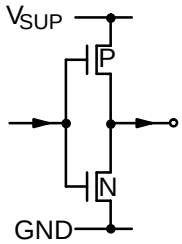

Fig. 2–10:
Output Pins 2 to 11, 55 and 68

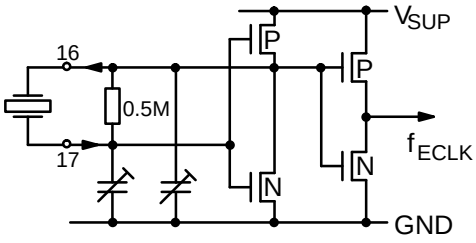

Fig. 2–11:
Crystal Oscillator Pins 16 and 17

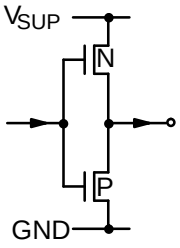

Fig. 2–12:
Output Pin 65

2.5. Electrical Characteristics

All voltages are referred to ground.

2.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+25	°C
V_{SUP}	Supply Voltage	19, 47, 63	–	6	V
V_I	Input Voltage, all Inputs	–	–0.3 V	V_{SUP}	–
V_O	Output Voltage, all Outputs	–	–0.3 V	V_{SUP}	–
I_O	Output Current, all Outputs	–	–10	+10	mA

2.5.2. Recommended Operating Conditions at T_A = 0 to 65 °C, $f_{\Phi M}$ = 20.25 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	19, 47, 63	4.75	5.0	5.25	V
$V_{\Phi MIDC}$	ΦM Clock Input D.C. Voltage	62	1.5	–	3.5	V
$V_{\Phi MIAC}$	ΦM Clock Input A.C. Voltage (p–p)		0.8	–	2.5	V
$\frac{t_{\Phi MIH}}{t_{\Phi MIL}}$	ΦM Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{\Phi MIHL}$	ΦM Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi M}}$	–
V_{REIL}	Reset Input Low Voltage	15	–	–	0.8	V
V_{REIH}	Reset Input High Voltage		2.4	–	–	V
t_{REIL}	Reset Input Low Time		2	–	–	µs
V_{VIL}	Video Input Low Voltage	39 to 46	–	–	2.2	V
V_{VIH}	Video Input High Voltage		2.8	–	–	V

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
$V_{\Phi VIH}$	Video Input Hold Time after ΦM Clock Input	39 to 46, 62	14	–	–	ns
$V_{VIS\Phi}$	Video Input Setup Time before ΦM Clock Input		4	–	–	ns
V_{ODIL}	Outputs Disable Inputs Low Voltage	18	–	–	0.8	V
V_{ODIH}	Outputs Disable Inputs High Voltage		2.4	–	–	V
V_{DSIL}	Descrambled Data Input Low Voltage	56	–	–	0.8	V
V_{DSIH}	Descrambled Data Input High Voltage		2.4	–	–	V
$V_{\Phi AL}$	ΦA Clock Input Low Voltage	17	–	–	0.8	V
$V_{\Phi AH}$	ΦA Clock Input High Voltage		V_{SUP} –0.8V	–	–	–
$\frac{t_{\Phi AH}}{t_{\Phi AL}}$	ΦA Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{\Phi AHL}$	ΦA Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi A}}$	–
$t_{\Phi ALH}$	ΦA Clock Input Low to High Transition Time		–	–	$\frac{0.15}{f_{\Phi A}}$	–
$f_{\Phi A}$	ΦA Clock Input Frequency		–	18.432	–	MHz
V_{IMIL}	IM Bus Input Low Voltage	12 to 14	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	1000	kHz
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input		0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		3.0	–	–	µs
t_{IM3}	ΦI Clock Input High Pulse Time		3.0	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5}	ΦI Clock Input Hold Time after Ident Input High		1.5	–	–	µs
t_{IM6}	ΦI Clock Input Setup Time before Ident End–Pulse Input		6.0	–	–	µs

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{IM7}	IM Bus Data Input Delay Time after ΦI Clock Input	12 to 14	0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End–Pulse Low Time		3.0	–	–	µs

2.5.3. Recommended Crystal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–20	–	+85	°C
f_p	Parallel Resonance Frequency	–	18.432*)	–	MHz
$\frac{\Delta f_p}{f_p}$	Accuracy of Adjustment	–	–	±40	ppm
$\frac{\Delta f_p}{f_p}$	Frequency Deviation versus Temperature	–	–	±40	ppm
R_r	Series Resistance	–	–	50	Ω
C_0	Shunt Capacitance	5.5	–	7.5	pF
C_1	Motional Capacitance	15	–	20	fF
P	Rated Drive Level	–	0.02	–	mW
$\frac{f_p}{f_H}$	Spurious Frequency Attenuation	20	–	–	dB

*) at C_L = 10 pF. This frequency applies for a certain application. For other applications, an appropriate frequency must be chosen.

2.5.4. Characteristics at T_A = 0 to 65 °C, V_{SUP} = 4.75 to 5.25 V, $f_{\Phi M}$ = 20.25 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUP}	Supply Current	63	–	100	130	mA	
$V_{\Phi AOL}$	ΦA Audio Clock Output Low Voltage	65	–	–	2.0	V	$I_{\Phi AO}$ = 0.5 mA
$V_{\Phi AOH}$	ΦA Audio Clock Output High Voltage		3.0	–	–	V	$-I_{\Phi AO}$ = 0.5 m A
$t_{\Phi AHL}$	ΦA Audio Clock Output High to Low Transition Time		–	–	10	ns	
$f_{\Phi A}$	ΦA Audio Clock Output Frequency		–	18.432	–	MHz	
V_{LCOL}	Luma/Chroma Output Low Voltage	21 to 24, 27 to 38	–	–	0.3	V	I_{LCO} = 6 mA
I_{LCOH}	Luma/Chroma Output High Current		–	–	10	µA	V_{LCO} = 5 V
t_{LCOT}	Luma/Chroma Output Transition Time		–	–	10	ns	
$t_{\Phi LCOH}$	Luma/Chroma Output Hold Time after ΦM Clock Input	21 to 24, 27 to 38, 62	12	–	–	ns	
$t_{\Phi LCOS}$	Luma/Chroma Output Setup Time after ΦM Clock Input		–	–	30	ns	
t_{LD}	Luma Output Delay Time after		–194	–	+839	µs	
V_{POL}	PLL Bus Output Low Voltage	25, 26	–	–	0.2	V	I_{PO} = 2 mA
I_{POH}	PLL Bus Output High Current		–	–	10	µA	V_{PO} = 5 V
$f_{\Phi P}$	ΦP Clock Frequency	26	–	$\frac{f_{\Phi M}}{4}$	–	–	
$\frac{t_{\Phi POH}}{t_{\Phi POL}}$	ΦP Clock Output High/Low Ratio		0.8	1	1.25	–	
$t_{PDOS\Phi}$	PLL Data Output Setup Time before ΦP Clock Output	25, 26	20	–	–	ns	
$t_{\Phi PDOH}$	PLL Data Output Hold Time after ΦP Clock Output		80	–	–	ns	
V_{SOL}	S Bus Output Low Voltage	64, 66, 67	–	–	0.2	V	I_{SO} = 2 mA
I_{SOH}	S Bus Output High Current		–	–	10	µA	V_{SO} = 5 V
t_{SOT}	S Bus Output Transition Time		–	–	10	ns	
$f_{\Phi S}$	ΦS S Clock Output Frequency	67	–	$\frac{f_{\Phi A}}{4}$	–	–	
$\frac{t_{S2}}{t_{S1}}$	ΦS S Clock Output High/Low Ratio		0.9	1	1.1	–	
t_{S3}	ΦS S Clock Output Setup Time before Ident End–Pulse Output	64, 67	160	220	–	ns	

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
t_{S4}	S Bus Data Output Setup Time before ΦS S Clock Output	66, 67	100	–	–	ns	
t_{S5}	S Bus Data Output Hold Time after ΦS S Clock Output		100	–	–	ns	
t_{S6}	S Bus Ident End–Pulse Output Low Time	64	300	400	–	ns	
V_{BOL}	Burst Bus Output Low Voltage	58 to 60	–	–	0.4	V	I_{DMO} = 1.6 mA
V_{BOH}	Burst Bus Output High Voltage		2.8	–	–	V	$-I_{DMO}$ = 0.1 mA
t_{BT}	Burst Bus Output Transition Time		–	–	10	ns	
$f_{\Phi B}$	ΦB Burst Bus Clock Frequency	60	–	$\frac{f_{\Phi M}}{2}$ or $f_{\Phi M}$	–	–	
$\frac{t_{B3}}{t_{B2}}$	ΦB Clock Output High/Low Ratio		0.9	1	1.1	–	
t_{B1}	ΦB Clock Output Delay Time after Ident Output	58, 60	–	0	–	–	
t_{B4}	Ident Output Delay Time after ΦB Clock		–	0	–	–	
t_{B5}	Burst Bus Data Output Setup Time before ΦD Clock Output	59, 60	–	50	–	ns	
t_{B6}	Burst Bus Data Output Hold Time after ΦB Clock Output		–	0	–	–	
V_{IMOL}	IM Bus Data Output Low Voltage	14	–	–	0.3	V	I_{IMO} = 6 mA
I_{IMOH}	IM Bus Data Output High Current		–	–	10	µA	V_{IMO} = 5 V
t_4	IM Bus Data Output Setup Time before ΦI Clock Input High	14, 12	0	–	–	–	
t_5	IM Bus Data Output Hold Time after ΦI Clock Input Fall		0	–	–	–	
V_{CLOL}	Clamping Output Low Voltage	48	–	–	0.2	V	I_{CLO} = 2 mA
V_{CLOH}	Clamping Output High Voltage		–	–	V_{SUP} –0.5	V	$-I_{CLO}$ = 1 mA
V_{AGCOL}	AGC Output Low Voltage	49	–	–	0.4	V	I_{AGCO} = 6 mA
I_{AGCOZ}	AGC Output High–Impedance Current		–10	–	+10	µA	V_{AGC} = 0 to 5 V
V_{AGCOH}	AGC Output High Voltage		V_{SUP} –0.5	–	–	V	$-I_{AGC}$ = 1 mA
t_{AGCO}	AGC Output Pulse Duration		–	40	–	ms	
t_{SAGCO}	AGC Output Pulse Start Time		– line No. 624		–	–	
V_{HBCKOL}	Combined Horizontal Blanking & Color Key Output Low Voltage	50	–	–	0.4	V	I_{HBCKO} = 6 mA
I_{HBCKOZ}	Combined Horizontal Blanking and Color Key Output High–Impedance Current		–10	–	+10	µA	V_{HBCKO} = 0 to 5 V

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{HBCKOH}	Combined Horizontal Blanking & Color Key Output High Voltage	50	4.0	–	–	V	$-I_{HBCKO}$ = 0.1 mA
t_{HB2}	Horizontal Blanking Output Time		–	10.5	0	µs	
t_{CK2}	Color Key High Z Output Low Time		–	2.27	–	µs	
t_{CK1}	Color Key Output Delay Time after Horizontal Blanking Output		–	5.5	–	µs	
t_{HB1}	Horizontal Blanking Output Lead Time before Chroma Output High	50, 21 to 24, 27 to 30	5.8	–	18.4	µs	
V_{HVBOL}	Combined Horizontal and Vertical Blanking Output Low Voltage	51	–	–	0.4	V	I_{HVBO} = 6 mA
I_{HVBOZ}	Combined Horizontal and Vertical Blanking Output High–Impedance Current		–10	–	+10	µA	V_{HVBO} = 0 to 5 V
V_{HVBOH}	Combined Horizontal & Vertical Blanking Output High Voltage		4.0	–	–	V	$-I_{HVBO}$ = 0.1 mA
t_{VB1}	Vertical Blanking Output Time		–	0.64	–	ms	
t_{HB2}	Horizontal Blanking Output Time		–	10.5	–	µs	
V_{HBOL}	Horizontal Blanking Output Low Voltage	52	–	–	0.4	V	I_{HBO} = 1.6 mA
V_{HBOH}	Horizontal Blanking Output High Voltage		2.4	–	–	V	$-I_{HBO}$ = 0.1 mA
t_{HB2}	Horizontal Blanking Output Low Time		–	12	–	µs	
V_{CSOL}	Composite Sync Output Low Voltage	53	–	–	0.4	V	I_{CSO} = 1.6 mA
V_{CSOH}	Composite Sync Output High Voltage		2.8	–	–	V	$-I_{CSO}$ = 0.1 mA
t_{CS2}	Composite Sync Output Low Time 1		–	4.8	–	µs	
t_{CS3}	Composite Sync Output Low Time 2		–	2.4	–	µs	
t_{VB2}	Composite Sync Output Delay Time after Vertical Blanking Output	51, 53	–	1.5	–	µs	
t_{CSOLC}	Composite Sync Output Lead Time before Chroma Output	53, 21 to 24, 27 to 30	4.2	–	16.8	µs	
V_{PDOL}	Packet Data Output Low Voltage	55	–	–	0.4	V	I_{PDO} = 1.6 mA
V_{PDOH}	Packet Data Output High Voltage		2.4	–	–	V	$-I_{PDO}$ = 0.1 mA
V_{TSOL}	Teletext Sync Output Low Voltage	57	–	–	0.4	V	I_{TSO} = 1.6 mA
V_{TSOH}	Teletext Sync Output High Voltage		2.4	–	–	V	$-I_{TSO}$ = 0.1 mA

2.5.5. DRAM Interface Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{DIL}	RAM Data Input Low Voltage	1	–	–	0.8	V	
V_{DIH}	RAM Data High Voltage		2.0	–	–	V	
t_{DIS}	RAM Data Input Setup Time before CAS Output High	1, 68	–	–	75	ns	
t_{DIH}	RAM Data Input Hold Time after CAS Output High		0	–	33	ns	
V_{DOL}	RAM Data Output Low Voltage	1	–	–	0.4	V	I_{DO} = 1.6 mA
V_{DOH}	RAM Data Output High Voltage		2.4	–	–	V	$-I_{DO}$ = 0.1 mA
t_{DT}	RAM Data Op. Transition Time		3	–	50	ns	
t_{DHR}	RAM Data Hold Time after $\overline{RAS}$ Low	1, 8, 68	140	–	–	ns	
t_{DS}	RAM Data Setup Time before $\overline{CAS}$ Low		20	–	–	ns	
t_{DH}	RAM Data Output Hold Time after $\overline{CAS}$ Output Low	1, 68	80	–	–	ns	
V_{AOL}	RAM Address Output Low Voltage	2 to 6, 9 to 11	–	–	0.4	V	I_{AO} = 1.6 mA
V_{AOH}	RAM Address Output High Voltage		2.4	–	–	V	$-I_{AO}$ = 0.1 mA
t_{AT}	RAM Address Output Transition Time		3	–	50	ns	
t_{RAH}	Row Address Output Hold Time after $\overline{RAS}$ Output Low	2 to 6, 9 to 11, 8	22	–	–	ns	
t_{ASR}	Row Address Output Setup Time before $\overline{RAS}$ Output Low		30	–	–	ns	
t_{AR}	Column Address Output Hold Time after RAS Output Low	2 to 6, 9 to 11, 68	125	–	–	ns	
t_{CAH}	Column Address Output Hold Time after $\overline{CAS}$ Output		70	–	–	ns	
t_{ASC}	Column Address Output Setup Time before $\overline{CAS}$ Output		10	–	–	ns	
V_{RASOL}	$\overline{RAS}$ Output Low Voltage	8	–	–	0.4	V	I_{RASO} = 1.6 mA
V_{RASOH}	$\overline{RAS}$ Output High Voltage		2.4	–	–	V	$-I_{RASO}$ = 0.1 mA
t_{RAST}	$\overline{RAS}$ Output Transition Time		3	–	50	ns	
t_{RAS}	$\overline{RAS}$ Low Pulsewidth		125	–	3000	ns	
t_{RP}	$\overline{RAS}$ Output Precharge Time		130	–	–	ns	
t_{RSH}	$\overline{RAS}$ Output Hold Time after $\overline{CAS}$ Output Low	8, 68	110	–	–	ns	
V_{CASOL}	$\overline{CAS}$ Output Low Voltage	68	–	–	0.4	V	I_{CASO} = 1.6 mA
V_{CASOH}	$\overline{CAS}$ Output High Voltage		2.4	–	–	V	$-I_{CASO}$ = 0.1 mA
t_{PC}	Page Mode Cycle Time		170	–	–	ns	

DRAM Interface Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
t_{CAST}	$\overline{CAS}$ Output Transition Time	68	3	–	50	ns	
t_{CP}	$\overline{CAS}$ Output Precharge Time		70	–	–	ns	
t_{CAS}	$\overline{CAS}$ Low Pulsewidth		95	–	150	ns	
t_{RCD}	$\overline{CAS}$ Output Delay Time after $\overline{RAS}$ Output	68, 8	45	–	–	ns	
t_{CSH}	$\overline{CAS}$ Output Hold Time after $\overline{RAS}$ Output		170	–	–	ns	
t_{CRP}	$\overline{CAS}$ Output Precharge Time before $\overline{RAS}$ Output		150	–	–	ns	
V_{WOL}	$\overline{WRITE}$ Output Low Voltage	7	–	–	0.4	V	I_{WO} = 1.6 mA
V_{WOH}	$\overline{WRITE}$ Output High Voltage		2.4	–	–	V	$-I_{WO}$ = 0.1 mA
t_{WT}	$\overline{WRITE}$ Output Transition Time		3	–	50	ns	
t_{CWL}	$\overline{WRITE}$ Low before $\overline{CAS}$ High	7, 68	180	–	–	ns	
t_{WCH}	$\overline{WRITE}$ Command Hold Time after $\overline{CAS}$ Low		80	–	–	ns	
t_{RCH}	$\overline{READ}$ Command Hold Time after $\overline{CAS}$ High		50	–	–	ns	
t_{RRH}	$\overline{READ}$ Command Hold Time after $\overline{RAS}$ High	7, 8	20	–	–	ns	

2.5.6. Waveforms

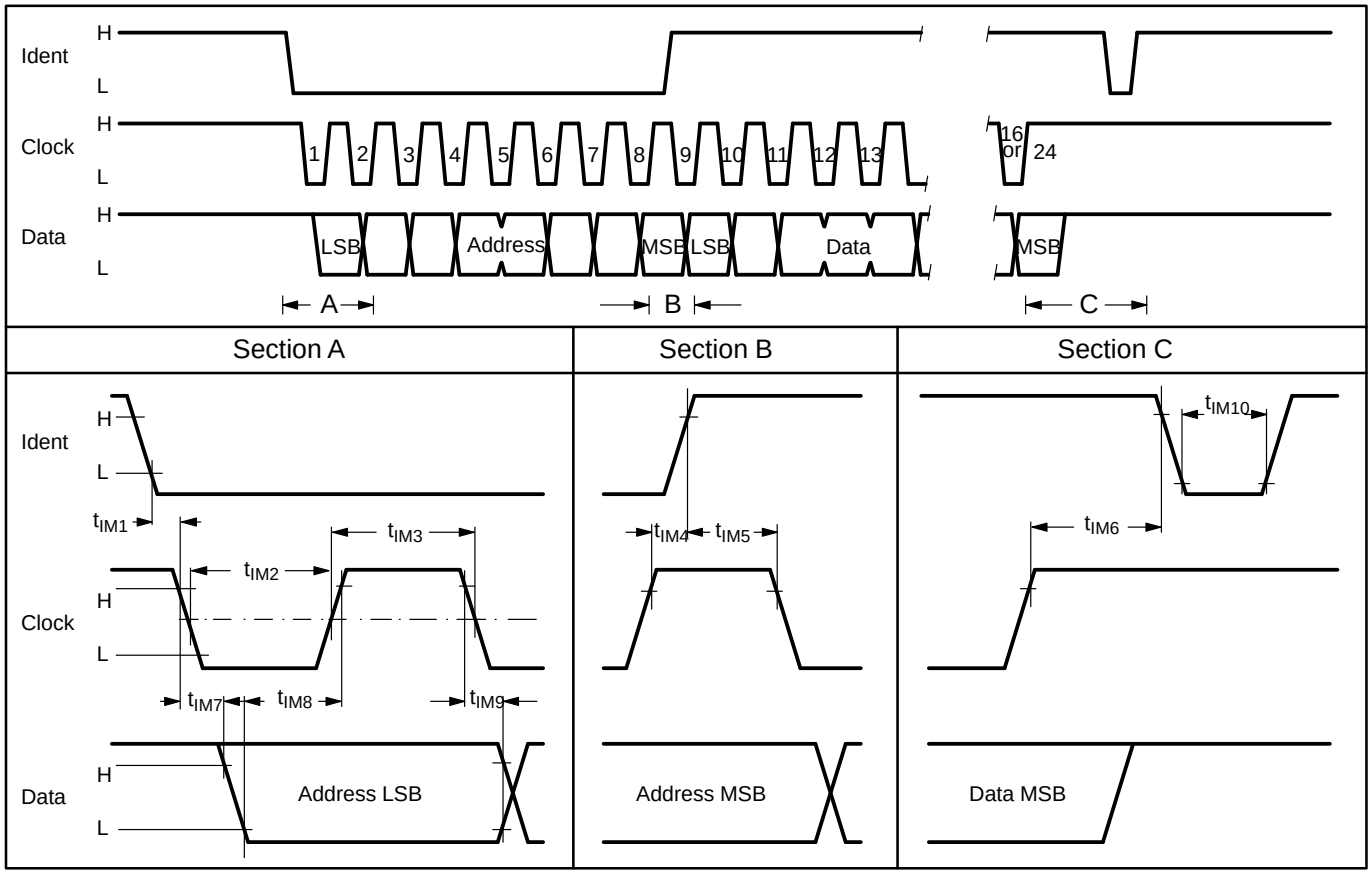

Fig. 2–13: IM bus waveforms

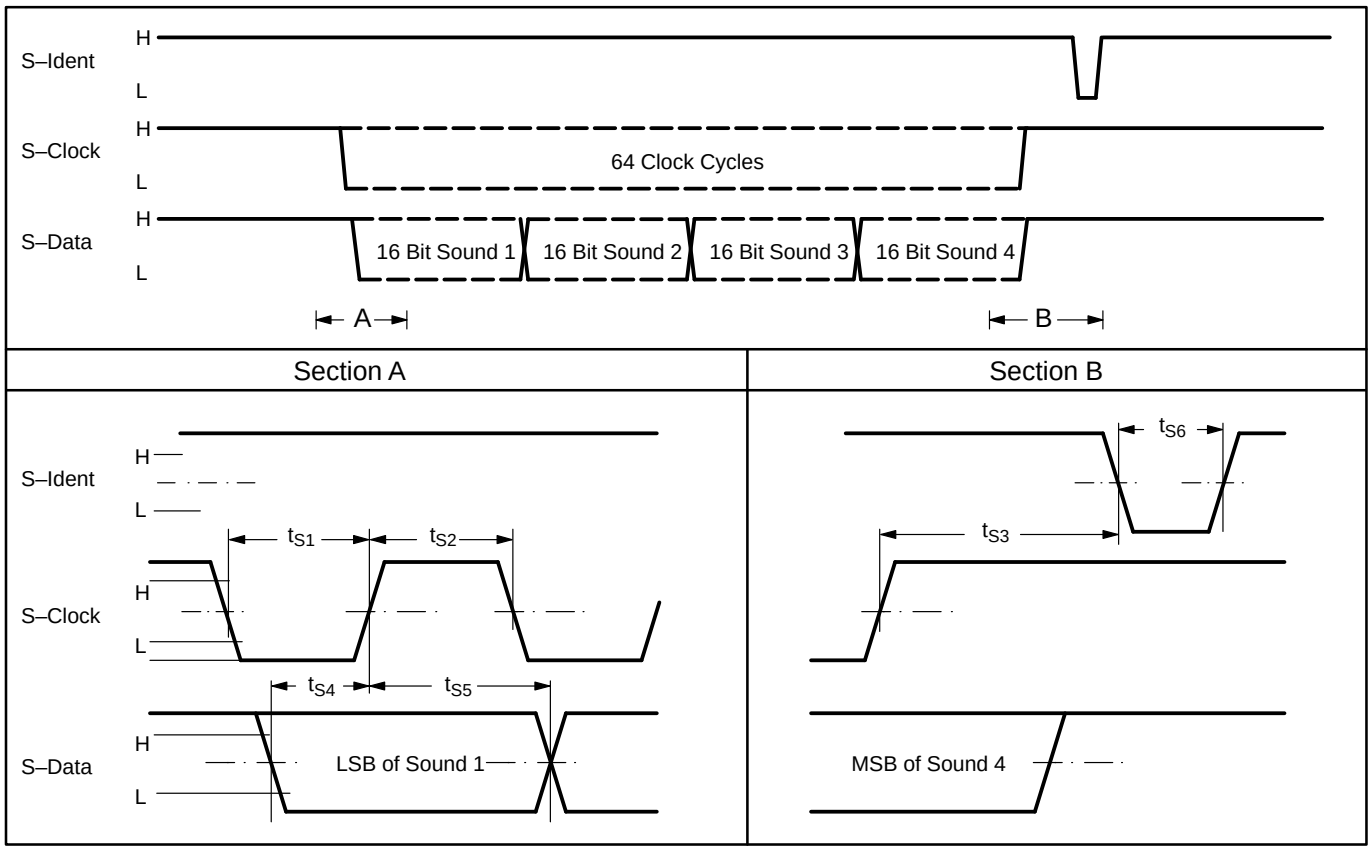

Fig. 2–14: S bus waveforms

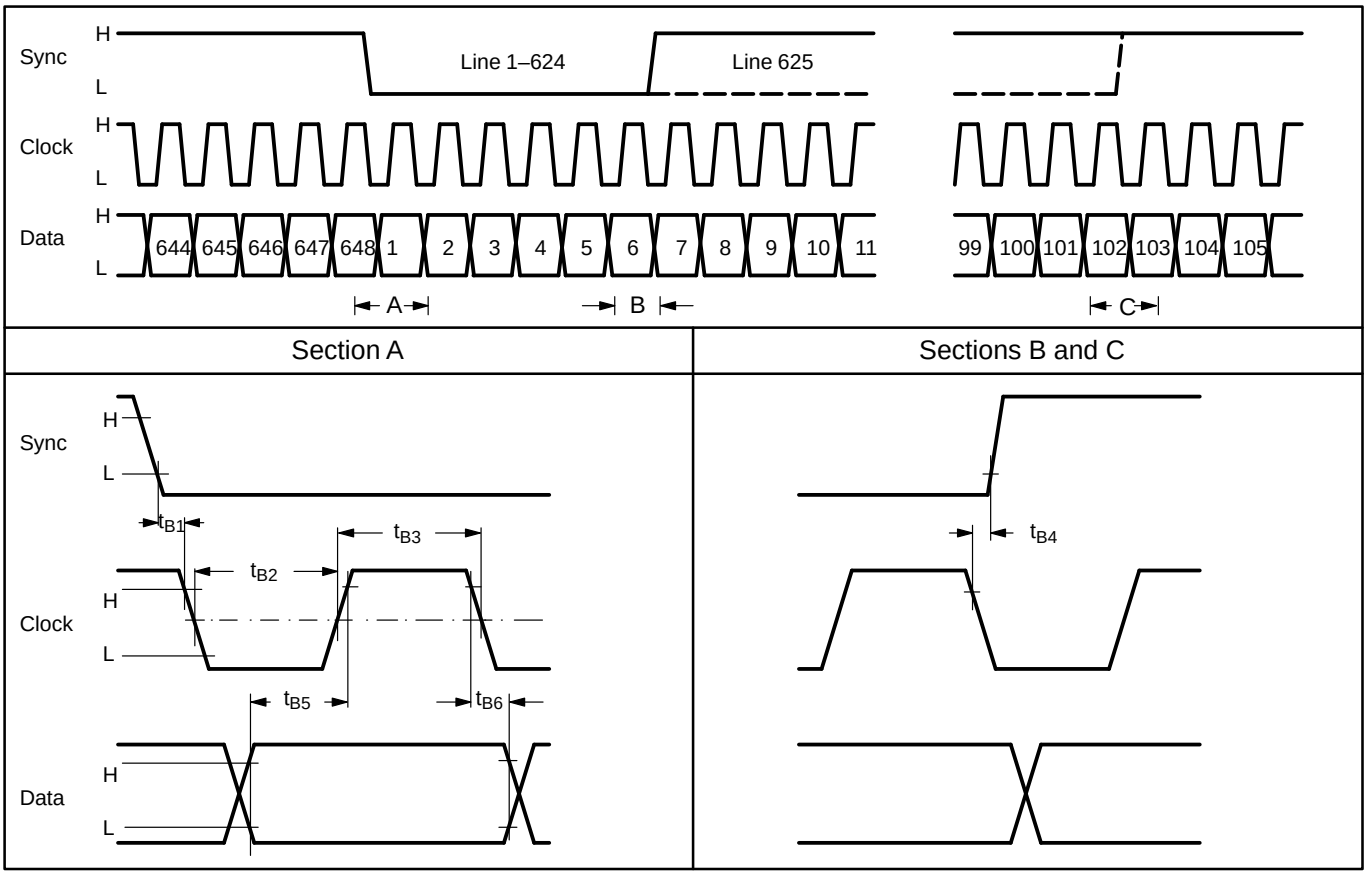

Fig. 2–15: Burst bus waveforms

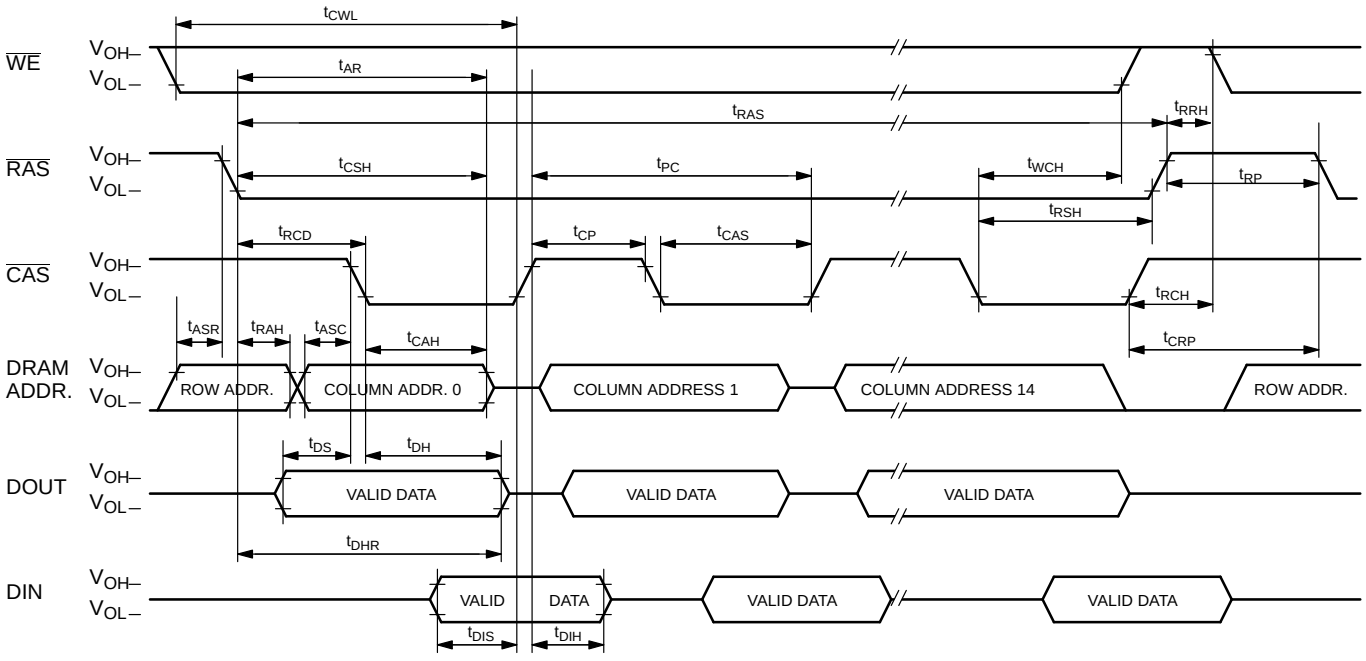

Fig. 2–16: DRAM waveform

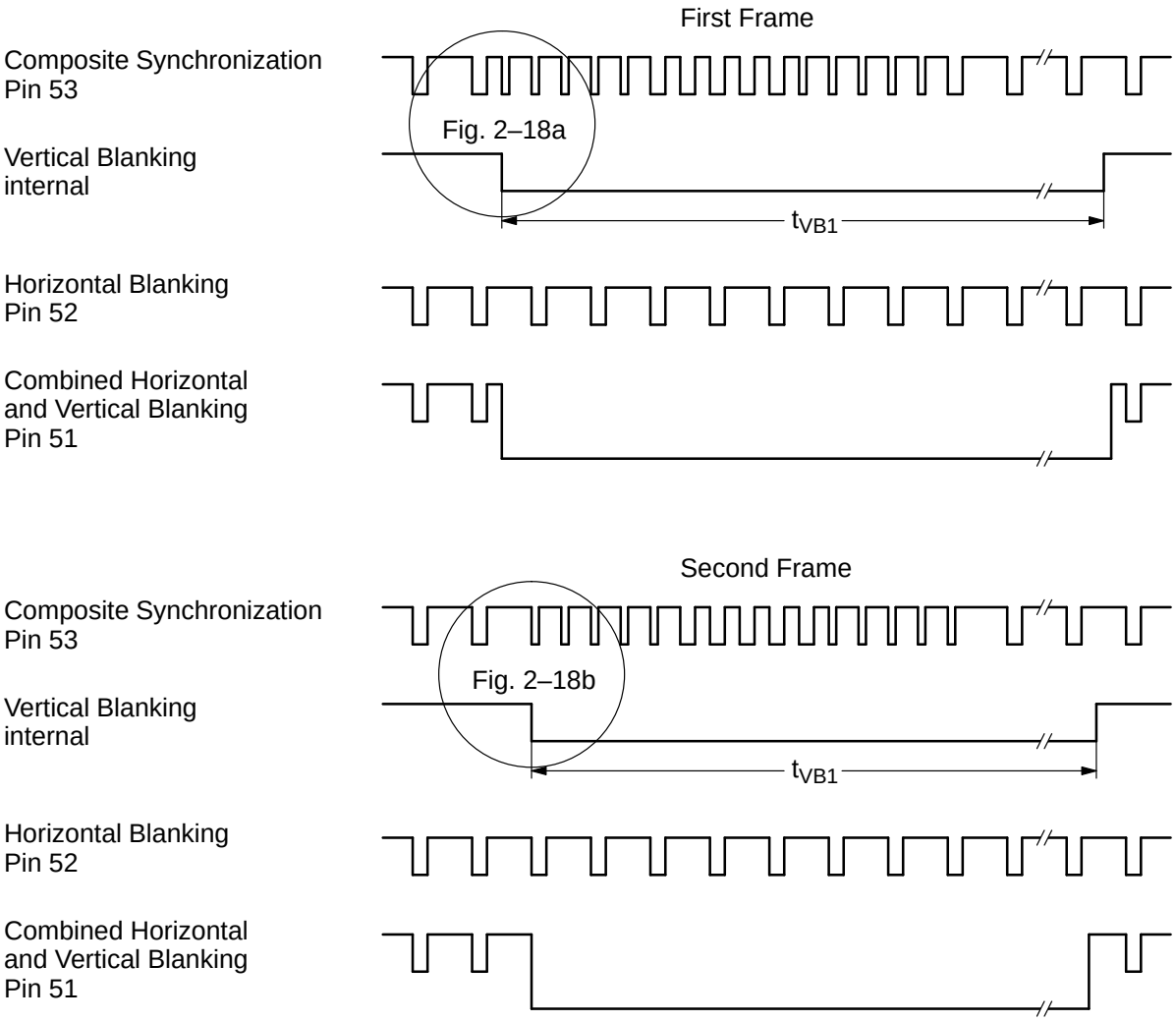

Fig. 2–17: Synchronization signals

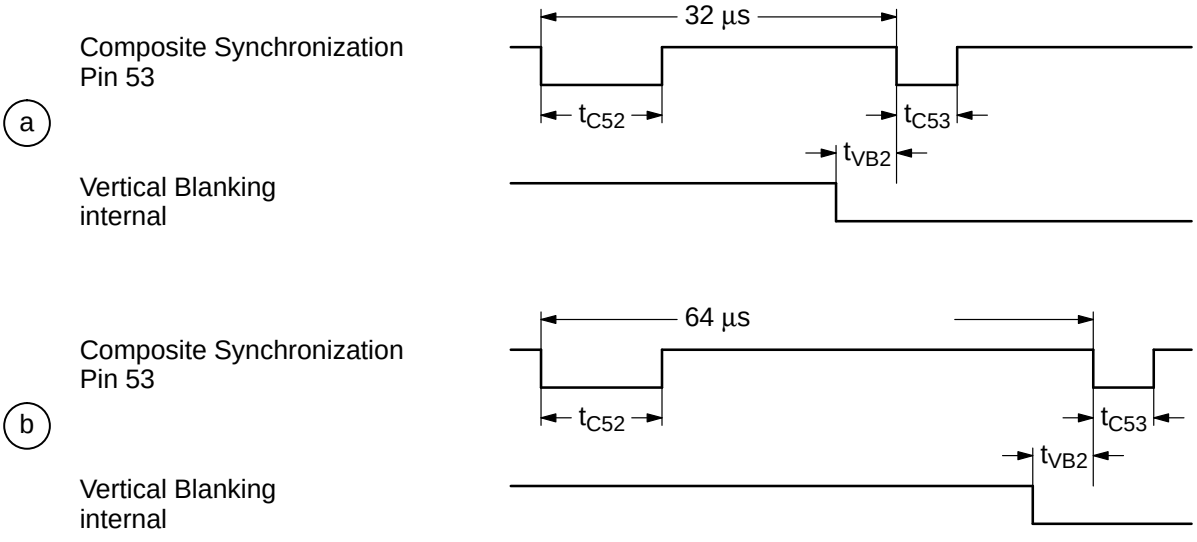

Fig. 2–18: Details of Fig. 2–17

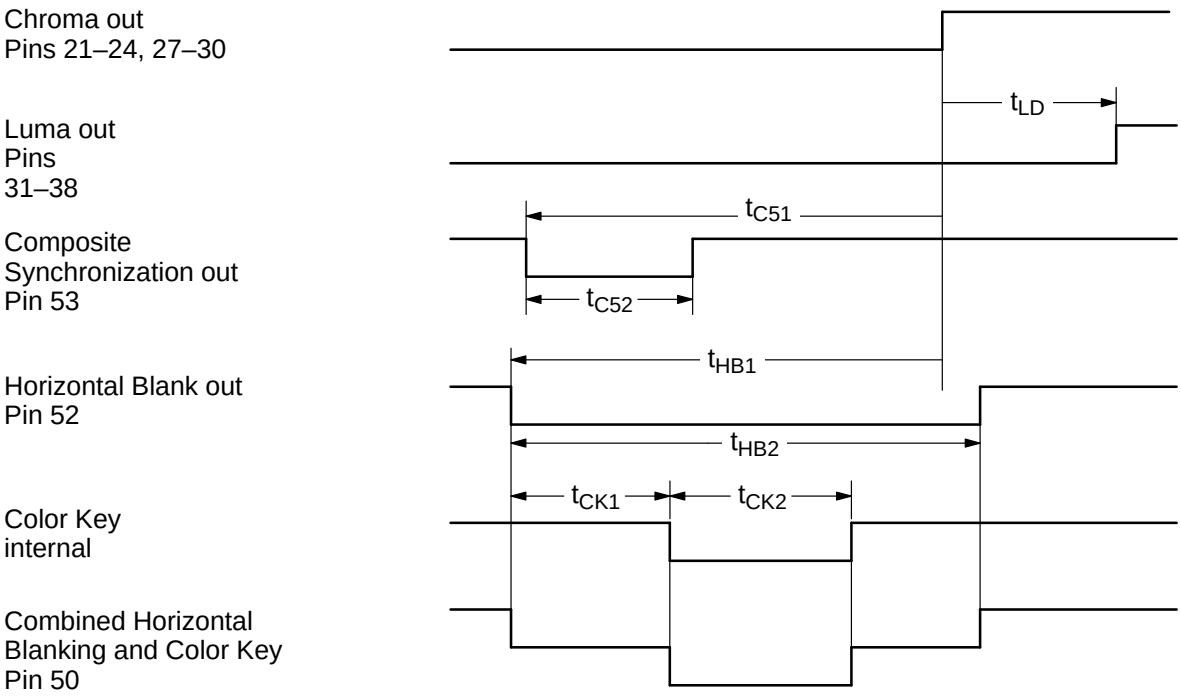

Fig. 2–19: Timing of video and sync signals

2.5.7. Frequency Responses

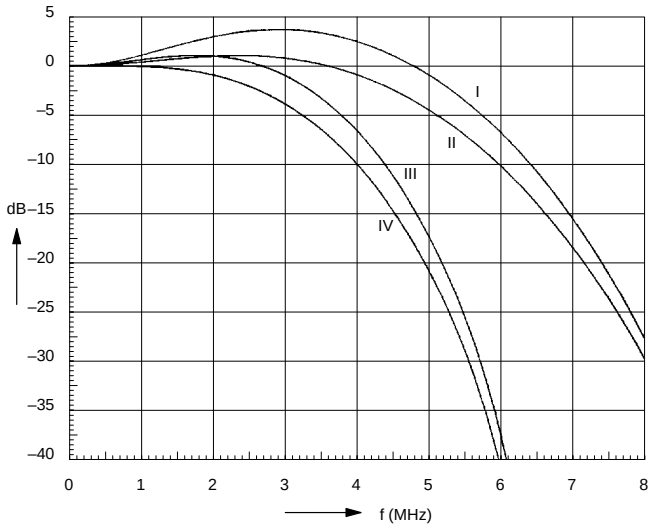

Fig. 2–20: Luminance channel frequency response

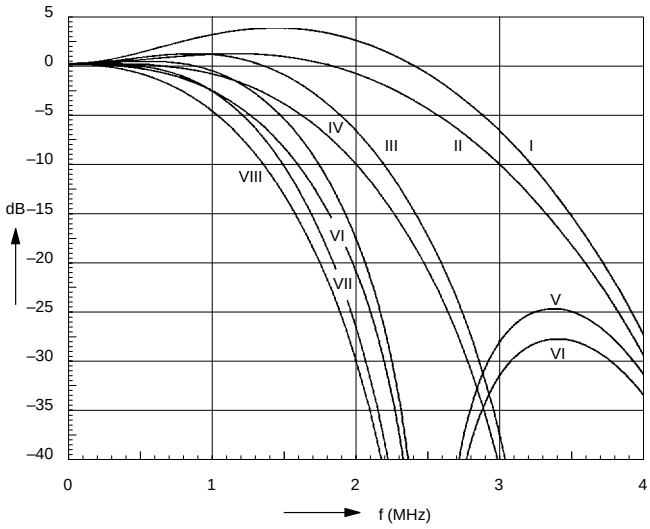

Fig. 2–21: Chrominance channel frequency response

Table 2–1: Selection of the luma filter response

LFI	Curve No.
0	I
1	II
2	III
3	IV

Table 2–2: Selection of the chroma filter response

CFI	Curve No.
0	I
1	II
2	III
3	IV
4	V
5	VI
6	VII
7	VIII

3. Functional Description

The DMA 2271, DMA 2280 and DMA 2281 process the digitized D2–MAC video signal supplied by the VCU 2133 or by the UVC 3130 in the various circuit parts shown in Fig. 1–4. The resulting digital luminance and chrominance signals are then reconverted to analog signals in the VCU or HDAA. The resulting digital audio signals are processed in the AMU 2481 Audio Mixer which provides filtering of the medium–quality channels and allows mixing of the four sound channels. The AMU's digital output signals are reconverted to analog in the ACP 2371 Audio Processor, which additionally carries out functions like adjustment of volume, bass and treble, loudness, etc. Remaining digital data as service and channel information in packet 0 or line 625 can be handled by software via the IM bus or by additional hardware which uses the serial B–Data interface (B–Data, B–Clock and B–Sync). Section 1.2. shows how the DMA 2271, DMA 2280 and DMA 2281 can be used together with other circuits of ITT's DIGIT 2000 digital TV system to realize a multistandard NTSC/PAL/SECAM/C/D/D2–MAC color TV receiver.

To understand the signal processing in the DMA 2271, DMA 2280, and DMA 2281 it may be useful to distinguish three different function blocks, namely:

– Clock and Data Recovery

– Video Processing

– Sound/Data Processing

3.1. Clock and Data Recovery

3.1.1. The Code Converter

This circuit converts the digitized C/D/D2–MAC baseband signal, delivered by the VCU 2133 in a parallel Gray code, into a simple binary–coded signal. The function of the circuit is controlled by the CCU 3000 via the IM bus (see section 4.2.).

3.1.2. The Video Clamping Circuit and the AGC Circuit

The video clamping circuit measures the DC voltage level of the clamp period and, by means of the pulse density modulated signal from pin 48, sets the DC level of the clamp period to a constant 5.5 V. The white and the black levels in line 624 are measured for automatic gain control (AGC pin 49) and the two values are fed to the IM bus interface which organizes the data communication with the CCU.

AGC (pin 49) = high if WL – BL < 224

AGC (pin 49) = high impedance if $224 \leq WL - BL \leq 240$

AGC (pin 49) = low if WL – BL > 240

3.1.3. The Phase Comparator and the PLL Filter

The phase comparator derives the reference signal from the slopes contained in the data burst of each line. Its output signal, an 8–bit word which is passed through a digital lowpass filter, is added to an 8–bit word, VCOA, which is provided by the CCU for adjustment of the crystal frequency. This digital PLL signal is output via pins 25 and 26 and routed to the MCU 2600 Clock Generator IC thus closing the PLL, existing between DMA 2271, DMA 2280, and DMA 2281, VCU 2133 Video Codec and MCU 2600 Clock Generator IC. In this way, the main clock signal FM of the system is in phase with the duobinary–coded signal.

To adjust the crystal frequency, it is possible to render inoperative the PLL by setting PLLO bit 4 in address 201 (Table 4–1). The VCO in the MCU is then free–running and the center frequency can be aligned by varying the data word VCOA (bits 0 to 7) in the IM bus address 14.

3.1.4. The Data Slicer and the Synchronization Circuit

The digitized C/D/D2–MAC baseband signal is filtered by a 5 MHz lowpass filter before being routed to the data slicer. The output of the slicer is connected to pin 59 (B–Data). In phase with the continuous bit stream of 20.25 or 10.125 MBit/s, a clock signal (B–Clock), a synchronization signal (B–Sync) and a signal for Teletext information (TTSYNC) are available at pins 60, 58, and 57 (see Fig. 2–15).

The vertical synchronization pulse, on–chip, is derived from a 64–bit correlator which compares the data stream at the output of the slicer with the fixed Frame Synchronization Word (FSW). Whenever the correlation is equal to or greater than 61 a frame reset pulse is generated. Horizontal synchronization is derived by counting. In phase with the video outputs (L0 to L7, C0 to C7), the various synchronization and blanking signals are outputs at pins 50 to 53 (Fig. 2–17, 2–18 and 2–18).

3.2. Video Processing

The DMA 2271, DMA 2280, and DMA 2281 process the C/D/D2–MAC baseband signal, digitized by the VCU or UVC at a sample frequency of 20.25 MHz. For time expansion, the video samples of each line are stored in an on–chip RAM and read to at the lower frequencies of 13.5 MHz for the luminance signal and 6.75 MHz for the color difference signals.

3.2.1. The Luminance Store

Time expansion of the luminance signal is achieved by digitizing the analog signal at a clock frequency of 20.25 MHz, storing the Bytes, and reading them at a frequency of 13.5 MHz. For this, a fast RAM is provided on–chip.

3.2.2. The Luminance Interpolating Filter

An interpolation from 13.5 MHz to 20.25 MHz is performed in order to overcome the need for a second system clock of 13.5 MHz and to simplify the reconstruction filters placed after the D/A conversion (RGB outputs of the VCU). The interpolation filter has a linear phase and can be switched to broad or narrow bandwidth by means of the CCU via the IM bus (bits 10 and 11, address 201). The different frequency responses are shown in Fig. 2–20 and in Table 2–1.

3.2.3. The Contrast Multiplier

After the luminance interpolating filter is a contrast multiplier. The contrast setting is controlled by the CCU via the IM bus (bits 10 to 15, address 200), depending on the user's instruction. From the contrast multiplier, the digital luminance signal is fed back to the VCU 2133 in the form of an 8–bit signal. In the VCU, this signal is converted from digital to analog and fed to the RGB matrix. The setting range of the contrast multiplier comprises 6 bits (64 steps). If the product at the multiplier's output is higher than the working range, the largest possible number is output.

3.2.4. The Chrominance Store

The chrominance store contains the color information for 3 lines. It is used for time expansion and line interpolation. The input frequency is 20.25 MHz, the output frequency 6.75 MHz.

3.2.5. The Line Interpolating Filter

The color difference signals are transmitted within alternate lines as U and V. A "1, 2, 1" post–filter required to interpolate the color difference information is implemented. The action of the filter is for even lines:

$$U = U_n,\ V = \frac{V_{n-1} + V_{n+1}}{2}$$

and for odd lines:

$$U = \frac{U_{n-1} + U_{n+1}}{2},\ V = V_n$$

3.2.6. The Chrominance Interpolating Filter

After the line interpolating filter the 8–bit color difference signals U and V are routed to the chroma interpolating filter which has linear phase and can be switched to different frequency responses via the IM bus (Fig. NO TAG, Table 2–2) using bits 13 to 15 in address 201. This filter is used for conversion of the sample rate from 6.75 MHz up to 10.125 MHz.

3.2.7. The Color Saturation Multiplier

The digital color difference signals U and V are routed to a color saturation multiplier, whose setting is also controlled by the CCU via the IM bus (address 23). The range of the multiplier comprises 6 bits, with each color difference signal being set independently.

The PAL matrix in the VCU requires a compensation factor of 0.71. This means that the color saturation factor for (B – Y) is equal to 0.71 the color saturation factor for (R – Y). Both factors are calculated in the CCU.

3.2.8. The Color Multiplexer

The color difference signals are transferred back to the VCU 2133 in multiplex via a 4–line bus. Demultiplexing takes place in the VCU. The digital signals are then reconverted to analog. Subsequently they are dematrixed in the RGB matrix together with the Y signal, giving the RGB signals which drive the output amplifiers of the VCU 2133 Video Codec.

The color multiplexer can drive a 4–line bus with an effective sample rate of 5.6025 MHz for each color difference signal or an 8–line bus with a sample rate of 10.125 MHz. This function is controlled by the IM bus (Table 4–1), using bit 6 in address 201.

3.3. Sound/Data Processing

This section begins with a descrambler and de–interleaver. The descrambler uses the same pseudo–random binary sequence (PRBS) generator as is used for the scrambling process. Its clock rate is 10.125 MHz or 20.25 MHz. The de–interleaver corrects the succession of the transmitted packet bits which are interleaved in order to minimize the effect of multiple bit errors.

Table 3–1: Transmission Order

1	95	189	283	377	471	565	659
2	96	190	284	378	472	566	660
		...			...		
		...			...		
		...			...		
93	187	281	375	469	563	657	751
94	188	282	376	470	564	658	(1)

3.3.1. The Golay and PT Byte Decoder

The data format has changed now from data burst format (99 bits) to packet format (751 bits). The header of each packet contains defined addresses for the different sound and data services and four bits representing the sound characteristics. The PT Byte of each packet distinguishes between sound and data packets. After correction of header and PT Byte with the Golay and PT Byte decoder, this information is used for automatic configuration of the DMA 2271, DMA 2280, and DMA 2281.

In addition, the Golay decoder is used for measuring the bit error rate of the transmission channel. The bits in error in each packet header are accumulated over one frame (82 packets). The sum is stored in IM bus register 206 (Table 4–2) and can be read by the CCU which may control different muting functions.

3.3.2. The Address Comparator

The DMA 2271, DMA 2280, and DMA 2281 D2–MAC Decoders are able to treat different sound services automatically by decoding the address field of the packet header. The two continuity bits CI1 and CI0 are used to link successive packets of the same service in case of a 120 Byte sound coding service.

Among the different coding characteristics all combinations are possible. The user can select up to four sound channels simultaneously by programming the sound services via the IM bus (address 203, 194, 195 and 196). These addresses are compared with the address of each transmitted sound packet. At correspondence, this packet is selected and decoded.

3.3.3. The Sound Decoder

The sound decoding section converts all types of selected sound packets into a sequence of 14–bit sound samples. The medium–quality channels are up–sampled to the 32 kHz sampling frequency of the high–quality channels, i.e. every sample of a medium–quality channel is put out twice, the second time as a zero sample. The second part of the interpolation is performed in the AMU 2481 Audio Mixer where two oversampling filters are provided. The error correction section uses a range check and/or Hamming decoder, depending on the sound coding mode. The Hamming decoder is able to correct one error per sample and to detect double errors. The range check uses the highly protected scale factor bits to check the MSBs of each sample. Its error correction and detection abilities are shown in Table 3–2.

Erroneous samples, i.e. samples with uncorrectable errors, are concealed by replacement with interpolated adjacent samples. The storage capacity for buffering the sound samples during processing and for obtaining a smooth, regular output of sound samples is provided by an external 64–K DRAM. To ensure the continuity of output sound samples in case of packet loss or packet gain, the silence information is used and blocks of samples corresponding to “silence” are repeated or omitted.

3.3.4. The Sound Multiplex

After extension from 14 bits to 16 bits, the sound samples of the four channels are loaded into a 64–bit shift register and transferred to the AMU 2481 Audio Mixer via a serial 3–lines S bus. Fig. 2–14 shows the S bus timing.

Table 3–2: Error correction and detection

Scale Factor	Protection Range	Defective Bits	Error Correction	Error Detection
linear:				
111	1	–	–	–
110	2	X13, X12	–	1
101	3	X13, X12, X11	–	2
011	4	X13 → X10	1	2
100	5	X13 → X9	1	3
010	6	X13 → X8	2	3
001	7	X13 → X7	2	4
000	8	X13 → X6	2	4
companded:				
010	6	X9, X8	–	1
001	7	X9, X8, X7	–	2
000	7	X9, X8, X7	–	2

3.3.5. The ΦA Audio Clock

The audio clock ΦA for the AMU 2481 Audio Mixer and the ACP 2371 Audio Processor is also supplied by the DMA 2271, DMA 2280 and DMA 2281 which generate this 18.432 MHz clock by means of the crystal connected to pins 16 and 17 and supply it via pin 65. The frequency of 18.432 MHz is an integer multiple of the sound sampling frequency (32 kHz).

The ΦA audio clock output pin 65 can be switched over to the normal main clock ΦM if a standard other than C/D/D2–MAC is received. For this, bit ACS in address 204 of the IM bus is provided (Table 4–1).

The clock frequency ΦS for the serial S bus is also derived from the audio clock ΦA (pin 65) by dividing by eight (18.432 MHz: 4 = 4.608 MHz)

3.3.6. The Buffer for Packet 0

One packet address (000H) is reserved for service and network identification data. A 720–bit (90 Byte) Buffer is implemented on–chip especially for this, and is controlled by the CCU via the IM bus (bits 8 and 9, address 204). The following conditions must be met to ensure that a received packet is stored in this buffer:

Packet Address	PA =	000H
Packet Type	PT =	F8H
Data Group Type	TG =	selected type in IM bus register 204
Packet 0 Status	P0 =	0 (see IM bus registers 204 and 206)

The packet 0 buffer can be read sequentially from a 16–bit IM bus register (address 210, Table 4–2). One complete read cycle takes about 1.5 ms (IM bus frequency = 1 MHz). It is possible to reset and to clear the buffer via the IM bus in order to repeat the last–read cycle or to receive the next zero packet. Additionally, the last 16 bits of the zero packet are used for error checking. This CRC check calculates the 16–bit syndrom vector of the packet concerned and stores it in an IM bus register. It can then be used by software for error detection.

4. The Three Serial Interfaces

4.1. The S Bus Interface and the S Bus

The S bus has been designed to connect the digital sound output of the DMA 2271, DMA 2280, and DMA 2281 MAC Decoders or the MSP 2400 NICAM Demodulator/Decoder to audio–processing ICs such as the AMU 2481 Audio Mixer or the ACP 2371 Audio Processor etc., and to connect these ICs one to the other. The S bus is a unidirectional, digital bus which transmits the sound information in one direction only, so that it is not necessary to solve priority problems on the bus.

The S bus consists of the three lines: S–Clock, S–Ident, and S–Data. The DMA 2271, DMA 2280, and DMA 2281 or the MSP 2400 generates the signals S–Clock and S–Ident, which control the data transfer to and between the various processors which follow the DMA 2271, DMA 2280, and DMA 2281 or the MSP 2400. For this, the S–Clock and S–Ident inputs of all processors in the system are connected to the S–Clock and S–Ident outputs of the DMA 2271, DMA 2280, and DMA 2281 or the MSP 2400. S–Data output of the DMA 2271, DMA 2280, and DMA 2281 or MSP 2400 is connected to the S–Data input of the next following AMU, the AMU's S–Data output is connected to the ACP's S–Data input and so on.

The sound information is transmitted in frames of 64 bits, divided into four successive 16–bit samples. Each sample represents one sound channel. The timing of a complete transmission of four samples is shown in Fig. 2–14, the times are specified under "Recommended Operating Conditions". The transmission starts with the LSB of the first sample. The S–Clock signal is used to write the data into the receiver's input register. the S–Ident signal marks the end of one frame of 64 bits and is used as latch pulse for the input register. The repetition rate of S–Ident pulses is identical to the sampling rate of the D2–MAC or NICAM sound signal; thus it is possible to transfer four sound channels simultaneously.

The S bus interface of the DMA 2271, DMA 2280, and DMA 2281 mainly consists of an output register, 64–bit wide. The timing to write bit by bit is supplied by the S–Clock signal. In the case of an S–Ident pulse, the contents of the output register are written to the S–Data output.

4.2. The IM Bus Interface and the IM Bus

4.2.1. The IM Bus

The INTERMETALL Bus (IM Bus for short) was designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master, whereas all controlled ICs have purely slave status.

The IM bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 1 MHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. bidirectionality is achieved by using open–drain outputs. The 2.5 ... 1 kOhm pull–up resistor common to all outputs must be connected externally.

The timing of a complete IM Bus transaction is shown in Fig. 5–2. In the non–operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signal to Low level, indicating an address transmission, and sets the CL signal to Low level, as well as to switch the first bit on the Data line. Then eight address bits are transmitted, beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal switches to High, initiating the address comparison in the slave circuits. In the addressed slave, the IM bus interface switches over to Data read or write, because these functions are correlated to the address. Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two bytes of data are written into the addressed IC or read out from it, beginning with the LSB.

The completion of the bus transaction is signalled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data.

For future software compatibility, the CCU must write a zero into all bits not used at present. Reading undefined or unused bits, the CCU must adopt "don't" care behavior.

4.2.2. IM Bus Addresses and Instructions

By means of the IM bus, the DMA 2271, DMA 2280, and DMA 2281 communicate with the CCU 3000 Central Control Unit. The DMA 2271, DMA 2280, and DMA 2281 receive the instructions for the user–actuated settings such as color saturation, contrast, sound channel select, packet 0 control, etc., and transmits the measured or received values such as bit error rate, signal level, sound coding mode,packet 0 data, etc. The address numbers and the associated data for this interaction via the IM bus are shown in Tables 4–1 to 4–4. In these tables "W" means data written by the CCU into the DMA, and "R" means data read by the CCU from the DMA.

4.3. The Burst Bus

The Burst bus serves for transfer of the digitized D2–MAC baseband signal, after code conversion, low-pass filtering and slicing as described in sections 3.1.1. and 3.1.4., to e.g., the TPU 2735 Teletext Processor or the DMA 2275/DMA 2285/DMA 2286 MAC Descrambler. Timing of the B bus is shown in Fig. 2–15 and under Recommended Operating Conditions.

4.3.1. Control and Status Registers

Note: Not–used bits must be set to zero for control (receive) registers and are don't care for status (transmit) registers.

Table 4–1: 16–bit DMA control registers, instructions from CCU to DMA

Address	Label	Bit No.	Default Setting	Typical Value	Function
14	VCOA	0–7	0	0	VCO adjustment (range –128...+127) alignment of the 20.25 MHz VCO
14	VCOS	8–10	4	4	VCO select 1 = VCO3 selected 2 = VCO2 selected 4 = VCO1 selected
14	DI1 DI2 DI3	11 14 15	0	0	disable PLL output (pin 25, 26) if (DI1 . or . DI2 . or DI3) then PLL output = high impedance
23	SAV	2–7	32	25	saturation V adjust 0: gain = 0 63: gain = 2
23	SAU	10–15	32	18	saturation U adjust 0: gain = 0 63: gain = 2
200	LD	3–7	4	6	luma delay adjust (range 0...30) resolution: 20.25 MHz clock
200	CTS	8	0	1	luma contrast switch
200	CT	10–15	32	16	luma contrast adjust 0: gain = 0 63: gain = 1 if CTS = 1 63: gain = 2 if CTS = 0
201	DSY	0	1	0	disable sync outputs (pins 50–53, 58–60) 0 = enabled 1 = high impedance
201	DCL	1	0	0	disable clamping output (pin 48) 0 = enabled 1 = high impedance
201	DLC	2	0	0	disable luma/chroma output (pin 21–24, 27–38) 0 = enabled 1 = high impedance
201	NIN	3	0	0	non interlace 0 = interlace on 1 = interlace off
201	PLLO	4	0	0	PLL open 0 = PLL closed 1 = PLL opened
201	STA	5	0	0	stand alone operation 0 = digital insertion 1 = stand alone
201	CMP	6	0	0	chroma output multiplex 0 = 4 x 4 multiplex 1 = 2 x 8 multiplex

Table 4–1, continued

Address	Label	Bit No.	Default Setting	Typical Value	Function
201	DGC	7	0	0	disable gray code converter input signal (pin 39–45) 0 = gray coded 1 = binary coded
201	L525	8	0	0	525 lines standard select 0 = 625 lines standard selected 1 = 252 lines standard selected
201	LF	10–11	0	0	luma filter selection
201	CF	13–15	0	0	chroma filter selection
202	BD	1–7	64	64	horizontal blank delay adjust (pin 50–52) resolution: 10.125 MHz clock
202	SD	9–15	64	64	comp. sync delay adjust (pin 53) resolution: 10.125 MHz clock
203	C1A	0–9	0	128	channel 1 packet address
203	C1E	10	0	1	channel 1 enable
203	C1U	11	0	0	channel 1 mode update
203	C1M	12–15	0	12	channel 1 mode × × × × └ linear/nicam └ hamming/parity protection └ high/medium quality └ stereo/mono
194	see register 203				channel 2
195	see register 203				channel 3
196	see register 203				channel 4
197	SFS	0–10	7	7	subframe select SFS = sample number of the first bit in the selected subframe examples: DRS = 1, first subframe SFS = 7 DRS = 1, second subframe SFS = 106 DRS = 0, first subframe SFS = 14
197	CD	13	0	0	chip definition 0 = DMA 2280 1 = DMA 2285
197	AUM	14	0	0	auto mode 0 = auto mode off 1 = sound coding in packet header
197	DRS	15	0	1	data rate select 0 = 10.125 Mbits/s D2–MAC 1 = 20.25 Mbits/s C/D–MAC
198	EDC	0–3	0	0	energy dispersal compensation (–8...+7)
198	CLG	4–5	0	2	clamping loop gain
198	CS	14–15	0	0	chip select 0 = IM bus of DMA 2280 active 1 = IM bus of DMA 2285 active

Table 4–1, continued

Address	Label	Bit No.	Default Setting	Typical Value	Function
199	PLLS	0	0	0	PLL select 0 = D/D2 MAC PLL 1 = CMAC PLL
199	ENF2	1	0	0	enable filter 2 0 for C/D MAC 1 for D2 MAC
199	SLS	2–3	0	1	slicer select 0 for D2–MAC 1 for D–MAC 2 for C–MAC
199	PLLG	4–5	0	2	PLL gain 0 = maximal gain 3 = minimal gain
199	FCD	6	0	0	full channel data 0: DBW is gated (pin 52) 1: DBW is active all the time
199	BPH	7	0	0	burst phase 0 = with DMA 2285 1 = only DMA 2280
199	SLL	8–15	0	 40 0	slice level (range –128...+127) for D/D2–MAC for C–MAC
204	SBE	0–3	0	15	S bus enable × × × × └ channel 1 enable └ channel 2 enable └ channel 3 enable └ channel 4 enable
204	DGT	4–7	0	0	data group type selection
204	POR	8	0	0	packet 0 reset 1: select first byte in packet 0 buffer (first byte = data group type DGT)
204	POC	9	0	0	packet 0 clear 1: enable packet 0 buffer to store next packet 0
204	DSB	10	1	0	disable S bus outputs (pins 64, 66, 67) 0 = enabled 1 = high impedance
204	ACS	11	0	1	audio clock switch (pin 65) 0: audio clock = main clock 1: audio clock = 18.432 MHz
204	ACF	12	1	0	audio clock free running 0 = audio clock locked to main clock 1 = audio clock free running

Table 4–1, continued

Address	Label	Bit No.	Default Setting	Typical Value	Function
205	T0	0	0	0	for test only
205	T1	1	0	0	for test only
205	T2	2	0	0	for test only
205	T3	3	0	0	for test only
205	T4	4	0	0	for test only
205	T5	5	0	0	for test only
205	T6	6	0	0	enable PDAT input
205	T7	7	0	0	for test only
205	T8	8	0	0	disable error concealment
205	T9	9	0	0	for test only
205	T10	10	0	0	enable BDAT input
205	T11	11	0	0	for test only
205	T12	12	0	0	for test only
205	T13	13	0	0	disable luma/chroma interpolation filters
205	T14	14	0	0	for test only
205	T15	15	0	0	for test only

Table 4–2: 16–bit DMA status registers, information from DMA to CCU

Address	Label	Bit No.	Function
206	BER	0–7	bit error rate number of erroneous bits detected by the golay decoder within the 82 packet headers of one frame
206	VER	8–9	version 0: C/D/D2–MAC Decoder 1: D2–MAC Decoder 2: D–MAC Decoder 3: C/D2–MAC Decoder
206	C1S	10	status of sound signal selected by C1A 0: sound signal is inactive or interrupted 1: sound signal is present
206	C2S	11	status of sound signal selected by C2A 0: sound signal is inactive or interrupted 1: sound signal is present
206	C3S	12	status of sound signal selected by C3A 0: sound signal is inactive or interrupted 1: sound signal is present
206	C4S	13	status of sound signal selected by C4A 0: sound signal is inactive or interrupted 1: sound signal is present
206	P0S	14	status of packet 0 buffer 0: packet 0 selected by DGT not received 1: packet 0 received
206	SYNC	15	status of frame sync word detector 0: frame sync word not detected within 8 frames 1: frame sync word detected
207	WL	0–7	white level measured in line 624 (typical value = 240)
207	BL	8–15	black level measured in line 624 (typical value = 16)
208	C1L	0–3	coding law of sound signal selected by C1A
208	C2L	4–7	coding law of sound signal selected by C2A
208	C3L	8–11	coding law of sound signal selected by C3A
208	C4L	12–15	coding law of sound signal selected by C4A L = 0: companded law 1: linear law H = 0: first level protection 1: second level protection HQ = 0: medium quality sound 1: high quality sound S = 0: monophonic sound 1: stereophonic sound
209	PSL	0–7	packet 0 syndrom low byte
209	PSH	8–15	packet 0 syndrom high byte PSL + PSH = 0: packet 0 received without error PSL + PSH > 0: packet 0 received with error
210	PDL	0–7	packet 0 data low byte
210	PDH	8–15	packet 0 data high byte

Table 4–3: DMA control and status registers, graphical overview

Addr. No.	Bit No. / Direct.	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
14	W	DI3	DI2	⊘	⊘	DI1	VCOS			VCOA VCO Adjustment							
		0	0	0	0	0	1	0	0	0							
23	W	SAU Saturation U						⊠	⊠	SAV Saturation V						⊠	⊠
		28						0	0	40						0	0
200	W	CT Luma Contrast						CSE	CTS	LD Luma Delay					⊠	⊠	⊠
		32						0	0	6					0	0	0
201	W	CFI Chroma Filter			CSP	LFI Luma Filter		CSP	L525 525 lines	DGC Disable Gray	CMP Chroma Mult.	STA Stand alone	PLLO PLL open	NIN Non Interl.	DLC Disable L/C	DCL Clamp. off	DSY Disable Sync.
		0			0	0		0	0	0	0	0	0	0	0	0	0
202	W	SD Composite Sync. Delay							⊠	BD Blank Delay							⊠
		64							0	64							0
203	W	C1M Channel Mode				C1U Mode Update	C1E Channel Enable			C1A Channel Packet Addres							
		S	HQ	H	L	0	1			100							
194	W	C2M Channel Mode				C2U Mode Update	C2E Channel Enable			C2A Channel Packet Address							
		S	HQ	H	L	0	1			100							
195	W	C3M Channel Mode				C3U Mode Update	C3E Channel Enable			C3A Channel Packet Address							
		S	HQ	H	L	0	0			100							
196	W	C4M Channel Mode				C4U Mode Update	C4E Channel Enable			C4A Channel Packet Address							
		S	HQ	H	L	0	0			100							
197	W	DRS Data Rate Select	AUM Auto Mode	CD Chip Defin.	⊠	⊠				SFS Subframe Select							
		1	0	0	0	0				7							
198	W	CS Chip Select		⊠	⊠	⊠	⊠	⊠	⊠	⊠	⊠	CLG Clamping Loop Gain		EDC Energy Dispersal Compensation			
		0		0	0	0	0	0	0	0	0	2		2			
199	W	SLL Slice Level								BPH Burst Phase	FCD Full Chanel Data	PLLG PLL Gain		SLS Slicer Select	ENF2 Enable Filters	PLLT PLL Test	
		0								0	0	2		1	0	0	
204	W	⊠	⊠	⊠	ACF Audio Free	ACS Clock Switch	DSB Disable S_Bus	P0C P0 Clear	P0R P0 Reset	DGT Data Group Type				SBE S_Bus Enable			
		0	0	0	0	0	0	0	0	0				3			
205	W	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
206	R	SYNC	P0S	C49	C39	C29	C19	VER Version		BER Bit Error Rate							
		Status															
207	R	BL Black Level								WL White Level							
208	R	C4L Coding Law CH4				C3L Coding Law CH3				C2L Coding Law CH2				C1L Coding Law CH1			
		S	HQ	H	L	S	HQ	H	L	S	HQ	H	L	S	HQ	H	L
209	R	PSH Packet 0 Syndrom High Byte								PSL Packet 0 Syndrom Low Byte							
210	R	PDH Packet 0 Data High Byte								PDL Packet 0 Data Low Byte							

⊠ Bits must be set to zero for write registers (W) and are don't care for read registers (R)

⊘ Bits not used in DMA 2280 registers, but in other devices

Table 4–4: VCU control and status registers, graphical overview

Addr. No.	Bit No. / Direct.	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
16	W	SCS SECAM Chroma Sync	NIE Noise Invert. Enable	VI2 Video Input 2	COB Code Bits			BCR Beam Current Reduction		BR Brightness							
		1	0	0	7			0		128							
17	W	CR Cutoff Voltage Red								DR White Drive Red							YDA Luma Adder
		127								127							1
18	W	CG Cutoff Voltage Green								DG White Drive Green							BLD Blank Disable
		127								127							1
19	W	CB Cutoff Voltage Blue								DB White Drive Blue							YDAS Luma Adder Shift
		127								127							0
27	W									RGBC Ext. RGB Contrast						DGD Double Gain Disable	BEN Bit Enlarg.
		0								32						1	1

Bits must be set to zero for write registers (W) and are don’t care for read registers (R)

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