SONY®

CXL5504M/P

CMOS-CCD 1H Delay Line for NTSC

Description

The CXL5504M/P are CMOS-CCD delay line ICs that provide 1H delay for NTSC signals including the external low pass filter.

CXL5504M
8 pin SOP (Plastic)

CXL5504P
8 pin DIP (Plastic)

Features

- Single power supply (5V)
- Low power consumption 90mW (Typ.)
- Built-in peripheral circuits
- Clamp level of input signal can be selected

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
	P_D		
	CXL5504M	350	mW
	CXL5504P	480	mW

Functions

- 905-bit CCD register
- Clock driver
- Autobias circuit
- Input clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

Recommended Operating Condition (Ta = 25°C)

Supply voltage	V_{DD}	5 ± 5%	V

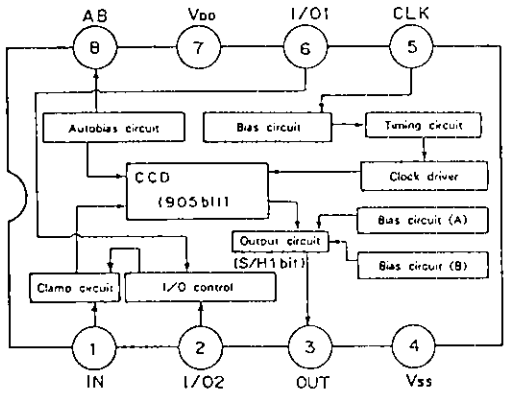
Recommended Clock Conditions (Ta = 25°C)

• Input clock amplitude	V_{CLK}	0.4 to 1.0	Vp-p (0.5Vp-p Typ.)
• Clock frequency	f_{CLK}	14.318182	MHz
• Input clock waveform	Sine wave		

Input Signal Amplitude

V_{SIG} 500mVp-p (Typ.), 572mVp-p (Max.)
(at Internal clamp condition)

Block Diagram and Pin Configuration (Top View)



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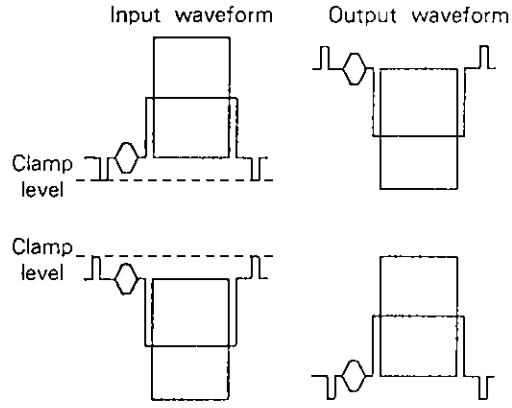
Pin Description

No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	> 10kΩ at no clamp
2	I/O2	I	I/O control 2	
3	OUT	O	Signal output	40 to 500 Ω
4	Vss	—	GND	
5	CLK	I	Clock input	> 100kΩ
6	I/O1	I	I/O control 1	
7	V_{DD}	—	Power supply (5V)	
8	AB	O	Autobias DC output	600 to 200kΩ

Description of Function

In the CXL5504M/P, the condition of I/O control pins (Pins 2 and 6) control the input signal clamp condition and the mode of the output signal with relation to its input signal.

There are 2 modes for the I/O signal.



① PN mode
(Low level clamp/reverse phase output mode)

② NP mode
(High level clamp/positive phase output mode)

I/O Control Pin

① I/O1 (Pin 6)
Control of the I/O signal condition

DC open····Input signal is low level clamped and the output signal is inverted in relation to the input signal. As the pin is biased to 2.5V by means of the resistance inside the IC, a decoupling capacitor of around 1000pF is necessary.

GND·····Input signal is high level clamped and the output signal turns into an inverted signal.

② I/O2 (Pin 2)
Control of the input signal clamp condition

0V·····Internal clamp condition

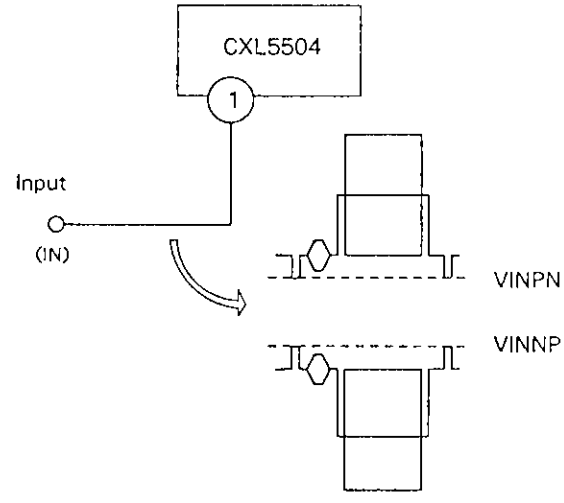
5V·····Non internal clamp condition
Center biased to approx. 2.1V by means of the IC internal resistance (several 10kΩ). Usage in this mode is limited to APL 50% signals and in this mode, the maximum input signal amplitude is 200mVp-p.

Electrical Characteristics ($Ta = 25°C$, $V_{DD} = 5V$, $f_{CLK} = 14.318182MHz$, $V_{CLK} = 500mVp\text{-}p$, Sine wave)
See "Electrical Characteristics Test Circuit"

Item	Symbol	Test condition	SW condition 1	2	3	4	5	6	7	Bias condition Vbias1 (V) (NOTE 1)	Min.	Typ.	Max.	Unit	NOTE
Supply current	IDDPN	——	—	c	b	b	b	a	—	——	10	18	28	mA	2
	IDDNP					a	a								
Low frequency gain	GLPN	200kHz 500mVp-p Sine wave	a	a	b	b	b	a	b	——	−2	0	2	dB	3
	GLNP					a	a								
Frequency response	fPN	200kHz↔3.57MHz 150mVp-p Sine wave	b ↕ c	a	a	b	b	b	b	2.1	−2	−1	0	dB	4
	fNP					a	a								
Differential gain	DGPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	——	0	5	7	%	5
	DGNP			b		a	a								
Differential phase	DPPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	——	0	5	7	degree	5
	DPNP			b		a	a								
S/H pulse coupling	CPPN	No signal input	—	c	a	b	b	b	a	VINPN + 0.5	—	—	350	mVp-p	6
	CPNP					a	a			VINNP					
SN ratio	SNPN	50% white video signal (See Note 7)	e	a	b	b	b	a	d	——	52	56	—	dB	7
	SNNP			b		a	a								

NOTE

① VINPN and VINNP are defined as follows.
VINPN and VINNP are the input signal clamp levels of PN and NP modes clamping the video signal sync chip level.



Testing of VINPN and VINNP is executed with a voltmeter under the following SW conditions.

Item	SW condition 1	2	3	4	5	6	7	Test point
VINPN	——	c	b	b	b	a	——	V1
VINNP	——	c	b	a	a	a	——	

② This is the IC supply current value during clock and signal input.

③ GLPN, GLNP are output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

(Example of calculation)

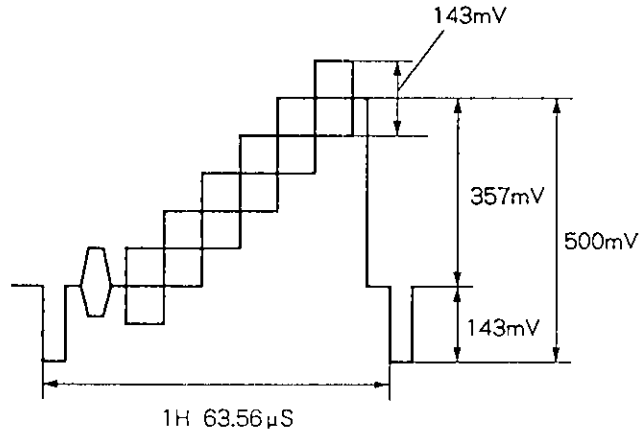
$$GLPN = 20\log \frac{\text{pin OUT output voltage (PN mode) [mVp-p]}}{500\ \text{[mVp-p]}}\ \text{[dB]}$$

④ Indicates the dissipation at 3.57MHz in relation to 200kHz.
From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 3.57MHz sine wave is fed to same, calculation is made according to the following formula. Input bias is tested at 2.1V.

(Example of calculation)

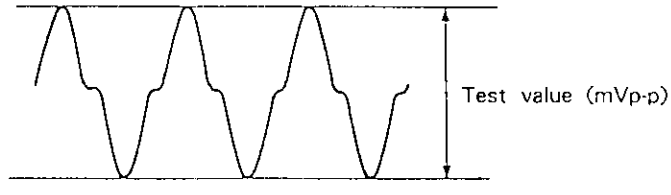
$$fPN = 20\log \frac{\text{pin OUT output voltage (PN mode, 3.57MHz) [mVp-p]}}{\text{pin OUT output voltage (PN mode, 200kHz) [mVp-p]}}\ \text{[dB]}$$

⑤ In Fig. below, differential gain (DG) and differential phase (DP) are tested with a vectorscope when the 5-staircase staircase wave is fed.

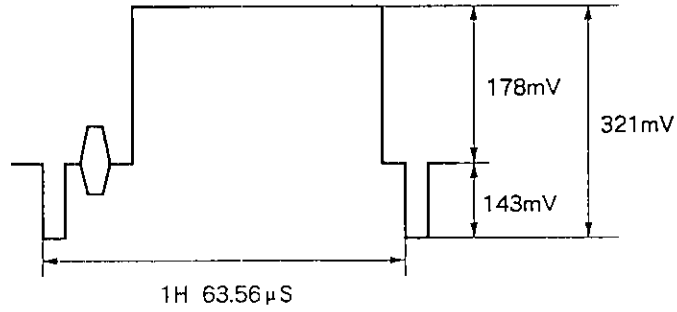


Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

⑥ Leakage of internal clock components and related high frequency components to the output signal, during no signal input. Input bias is tested at VINPN + 0.5V and VINNP for PN and NP modes respectively.



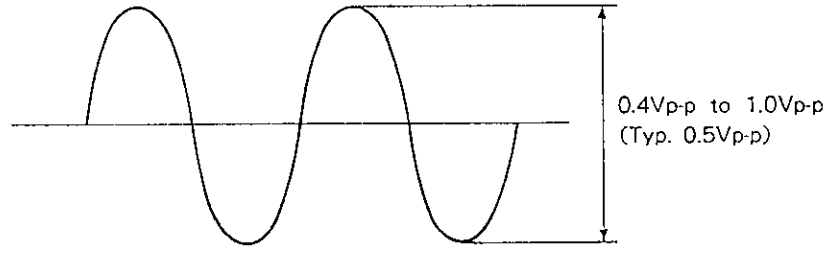
⑦ SN ratio during a 50% white video signal input shown in Fig. below is tested at a video noise meter, in BPF 100kHz to 4MHz, Sub Carrier Trap mode.



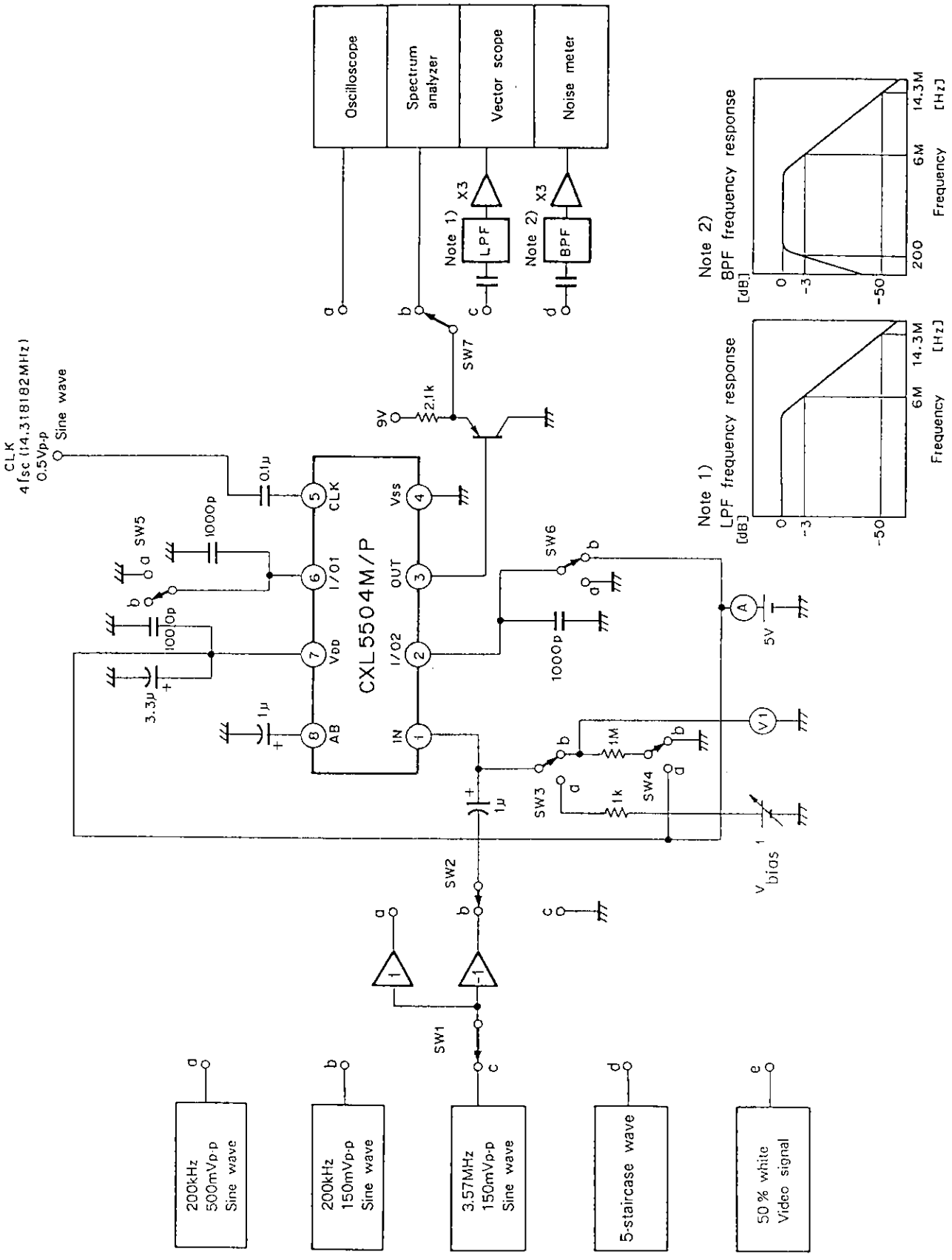
Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

CLOCK

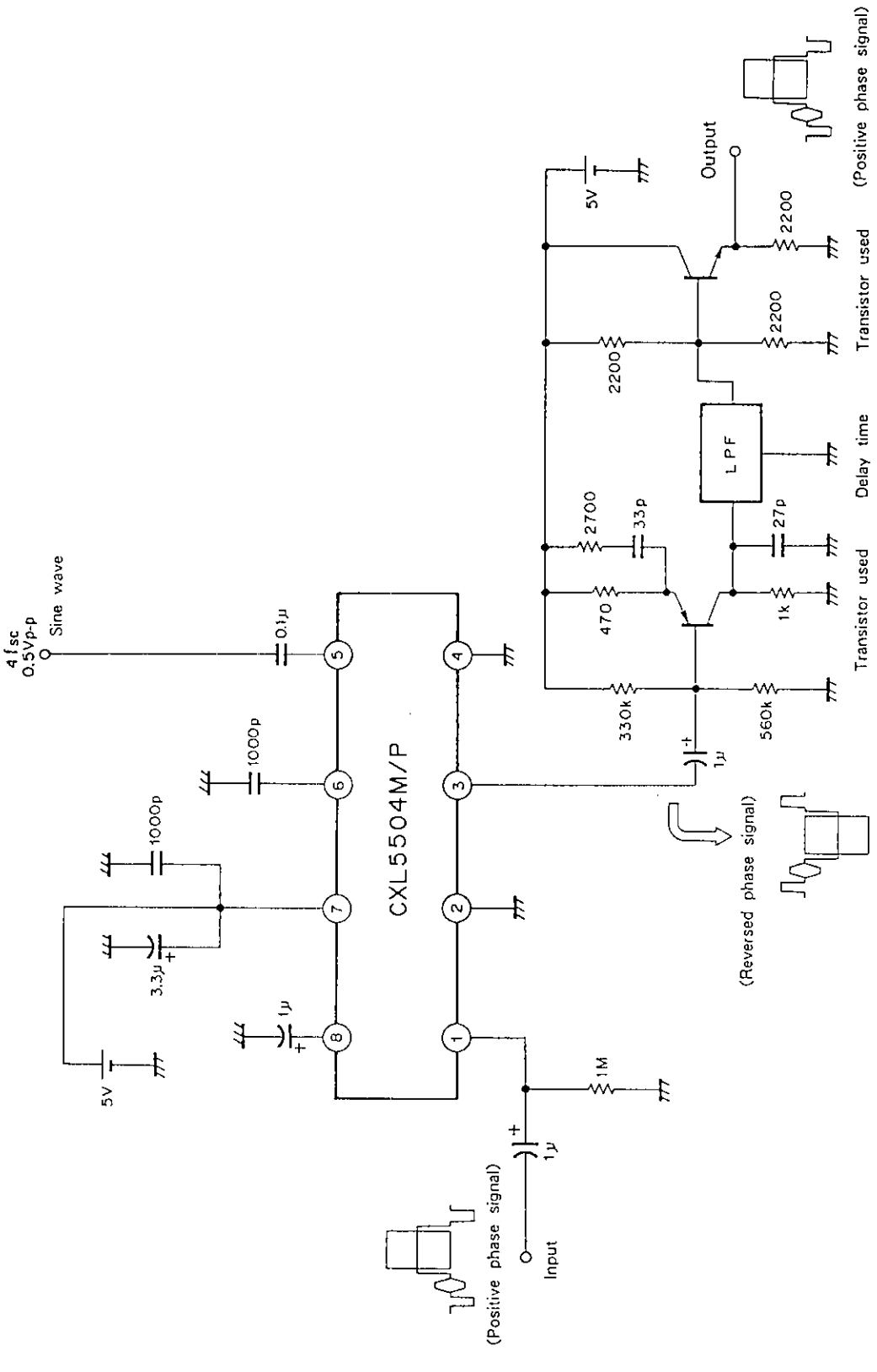
fsc (14.318182MHz) Sine wave



Electrical Characteristics Test Circuit



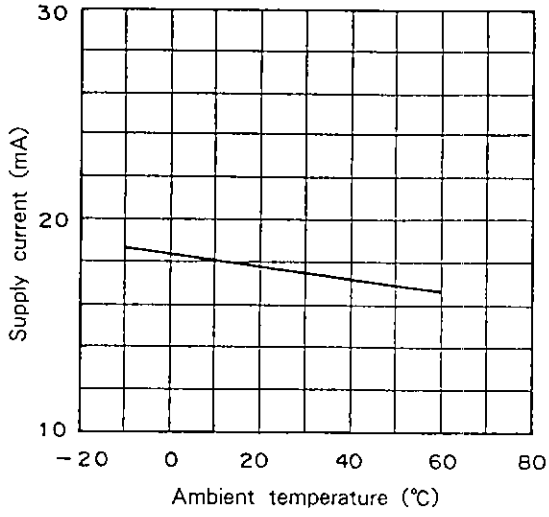
Application Circuit (Using PN mode)



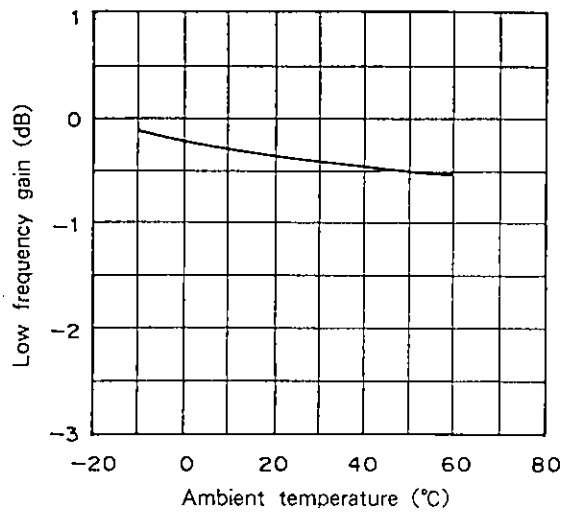
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

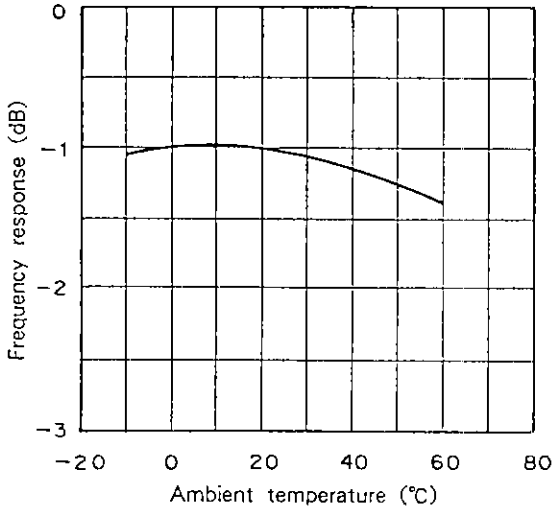
Supply current vs. Ambient temperature



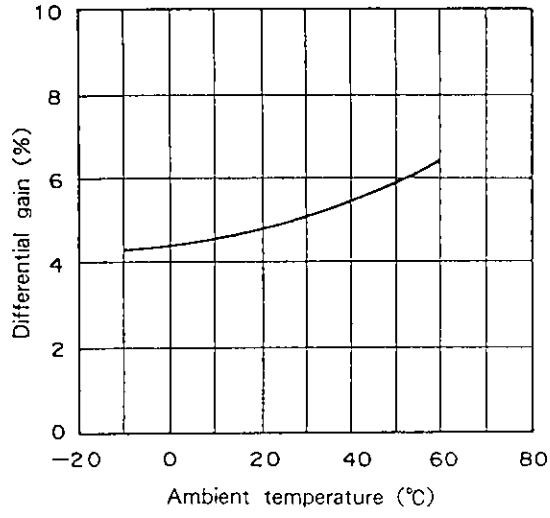
Low frequency gain vs. Ambient temperature



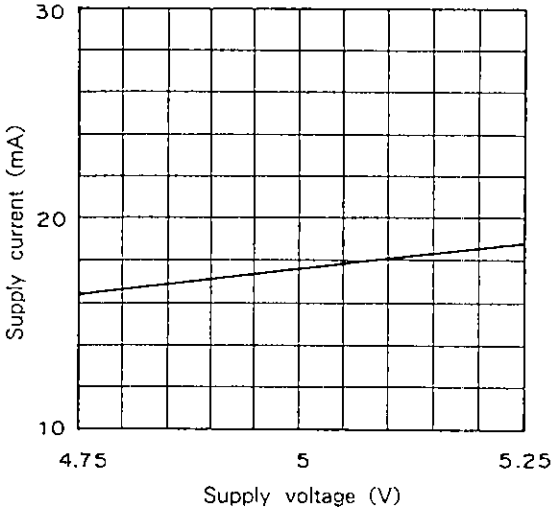
Frequency response vs. Ambient temperature



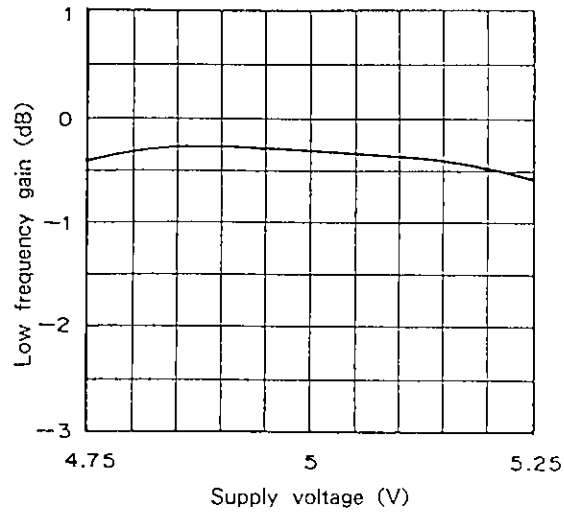
Differential gain vs. Ambient temperature



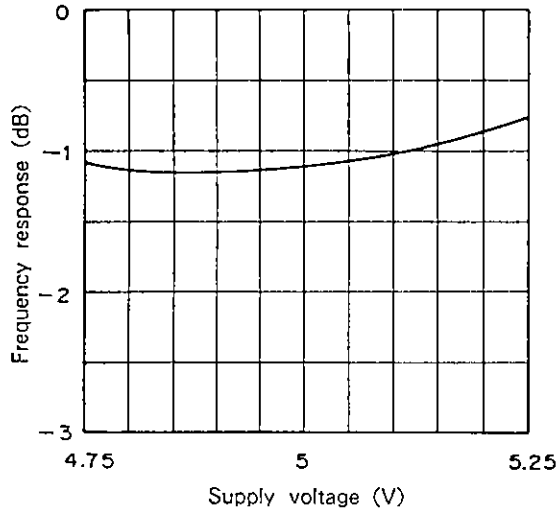
Supply current vs. Supply voltage



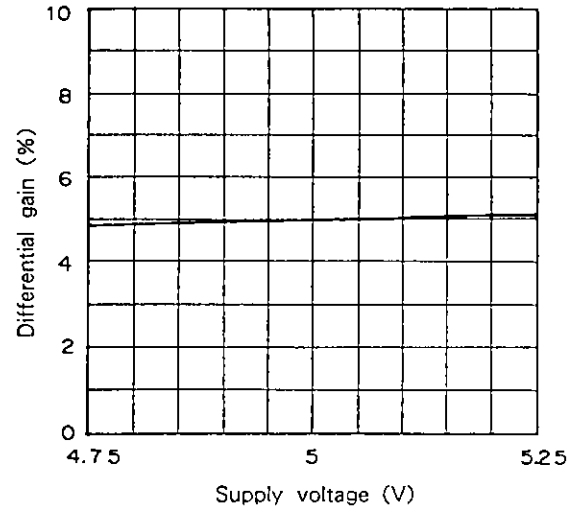
Low frequency gain vs. Supply voltage



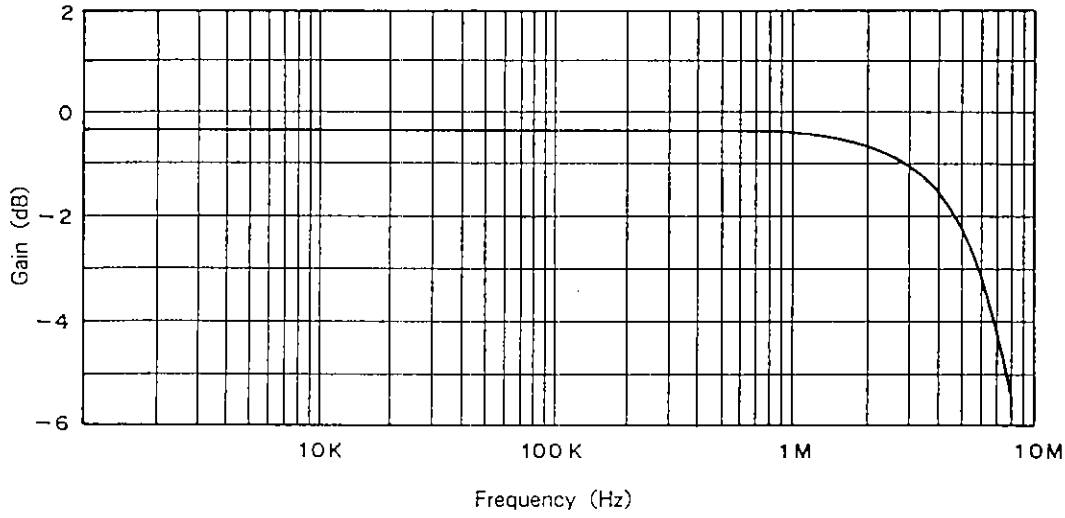
Frequency response vs. Supply voltage



Differential gain vs. Supply voltage



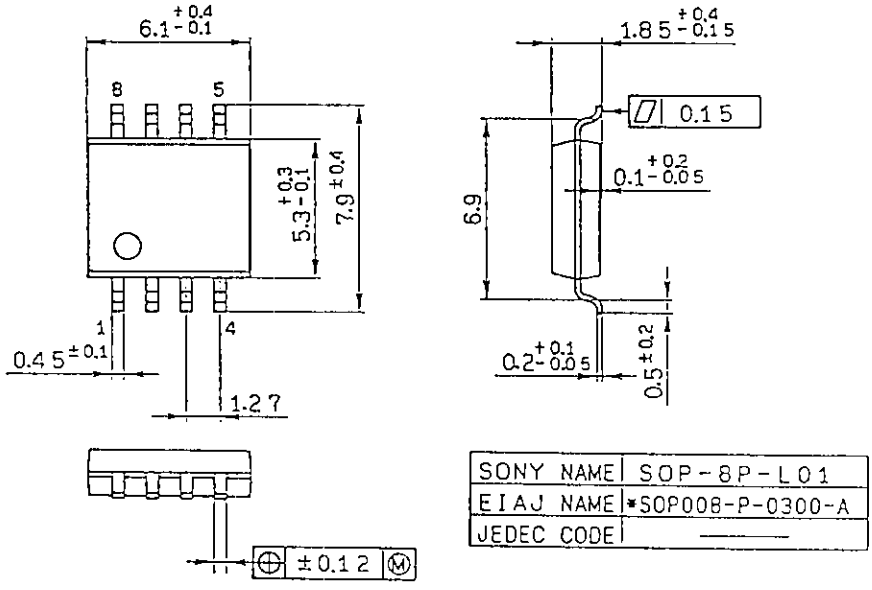
Frequency response



Package Outline

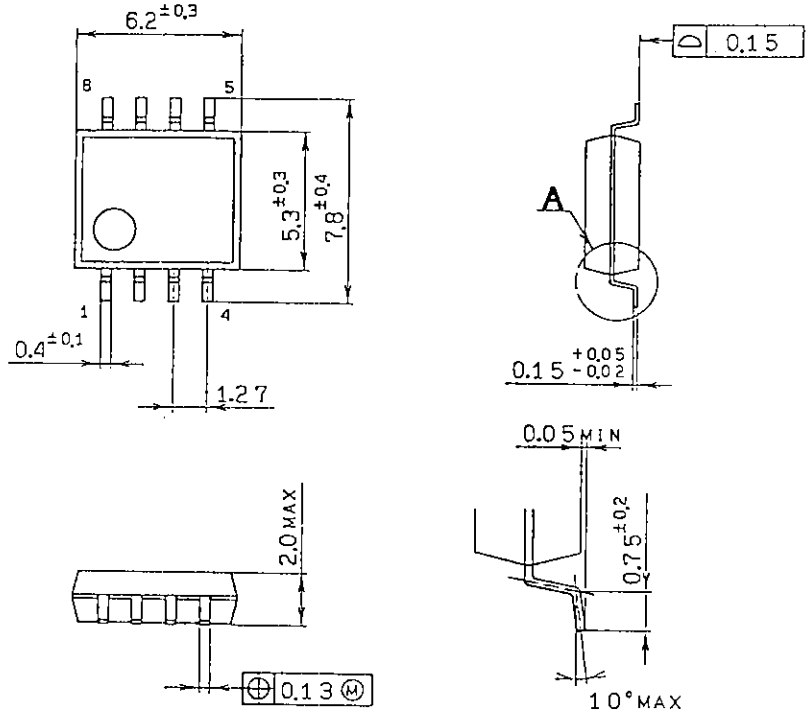
Unit : mm

CXL5504M 8pin SOP (Plastic) 300mil 0.1g



SONY NAME	SOP-8P-L01
EIAJ NAME	*SOP008-P-0300-A
JEDEC CODE	———

8pin SOP (Plastic) 300mil

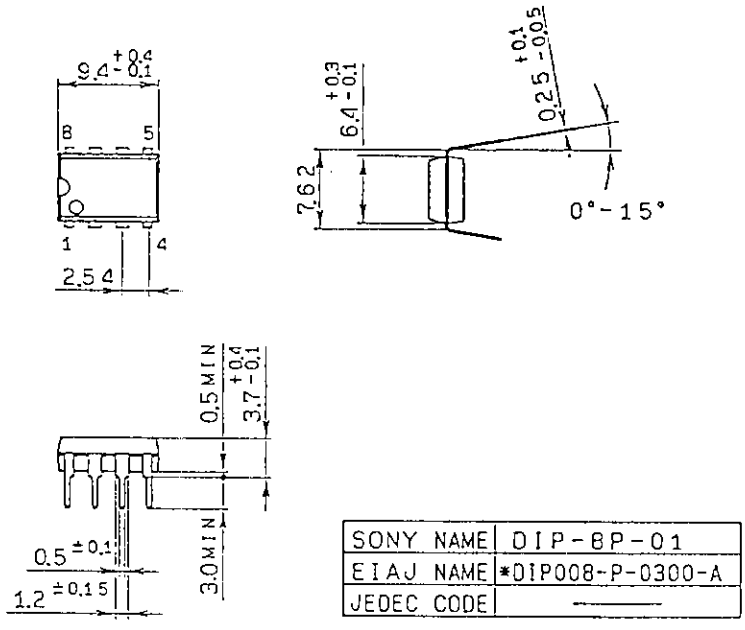


Detailed diagram of A

SONY NAME	SOP-8P-L121
EIAJ NAME	*SOP008-P-0300-AX
JEDEC CODE	———

CXL5504P

8pin DIP (Plastic) 300mil 0.5g



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