

Digital Signal Driver

Description

The CXD2449Q is a RGB driver of digital signal processor type. Arithmetic processing is possible with a system clock up to 100MHz (max.). This IC is suitable for the processing of video signals in bands up to XGA standard.

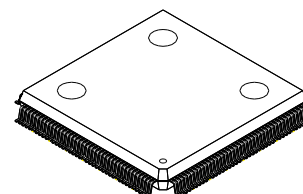
Features

- Gain, bright and limiter adjustment possible by digital arithmetic processing
- Gamma correction can be performed as desired by the look-up table method
- Built-in black frame signal processing circuit that fixes the blanking signal to a certain level
- Built-in serial I/F circuits

Applications

LCD projectors and other video equipment

160 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

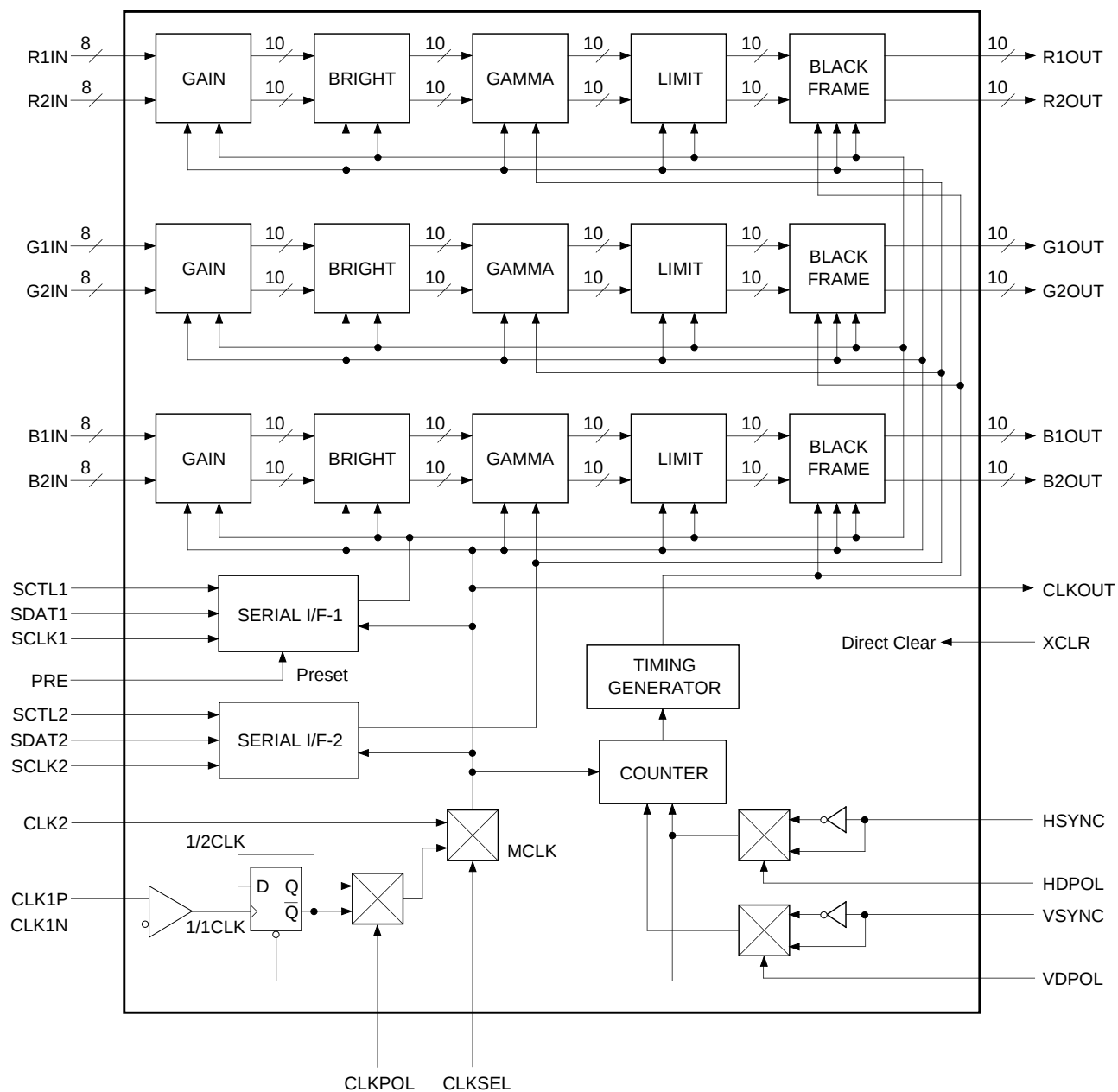
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|-----------------------|-----------|----------------------------------|----|
| • Supply voltage | V_{DD} | $V_{SS} - 0.5$ to $+4.0$ | V |
| • Input voltage | V_I | $V_{SS} - 0.5$ to $V_{DD} + 0.5$ | V |
| • Output voltage | V_O | $V_{SS} - 0.5$ to $V_{DD} + 0.5$ | V |
| • Storage temperature | T_{stg} | -55 to $+125$ | °C |

Recommended Operating Conditions

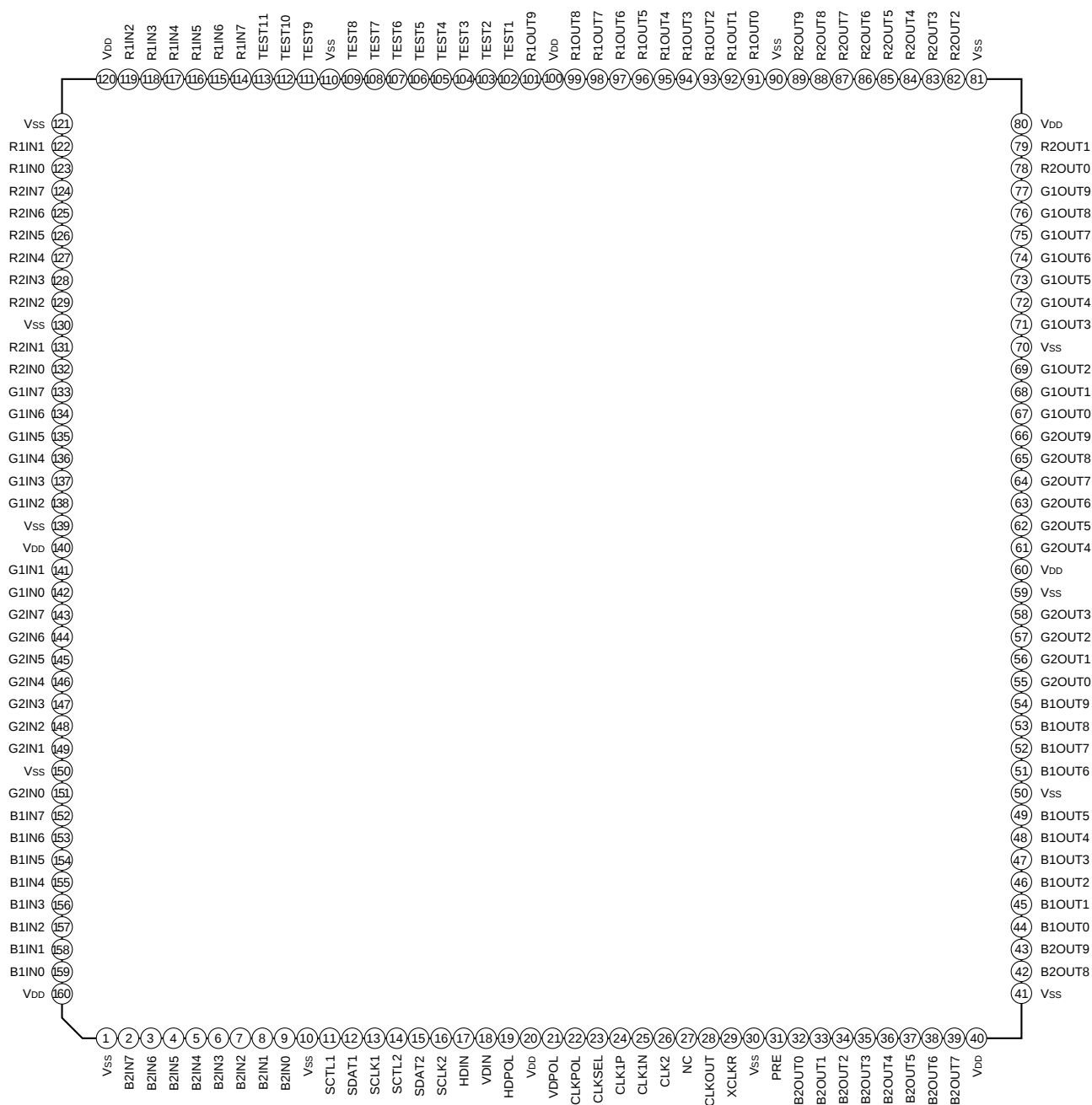
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|-------------------------|-----------|----------------|----|
| • Supply voltage | V_{DD} | 3.0 to 3.6 | V |
| • Operating temperature | T_{opr} | -20 to $+75$ | °C |

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Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description	Input processing
1	V _{SS}	—	GND	—
2	B2IN7	I	Blue-2 data signal input.	—
3	B2IN6	I	Blue-2 data signal input.	—
4	B2IN5	I	Blue-2 data signal input.	—
5	B2IN4	I	Blue-2 data signal input.	—
6	B2IN3	I	Blue-2 data signal input.	—
7	B2IN2	I	Blue-2 data signal input.	—
8	B2IN1	I	Blue-2 data signal input.	—
9	B2IN0	I	Blue-2 data signal input.	—
10	V _{SS}	—	GND	—
11	SCTL1	I	Serial I/F-1 control signal input.	—
12	SDAT1	I	Serial I/F-1 data signal input.	—
13	SCLK1	I	Serial I/F-1 clock input.	—
14	SCTL2	I	Serial I/F-2 control signal input.	—
15	SDAT2	I	Serial I/F-2 data signal input.	—
16	SCLK2	I	Serial I/F-2 clock input.	—
17	HDIN	I	Horizontal sync signal input.	—
18	VDIN	I	Vertical sync signal input.	—
19	HDPOL	I	Input HD polarity selection. (High: positive polarity, Low: negative polarity)	L
20	V _{DD}	—	Power supply.	—
21	VDPOL	I	Input VD polarity selection. (High: positive polarity, Low: negative polarity)	L
22	CLKPOL	I	Output CLK polarity selection. (High: positive polarity, Low: negative polarity)	L
23	CLKSEL	I	Input CLK selection. (High: CLK2, Low: CLK1)	L
24	CLK1P	I	CLK inputs. (differential)	—
25	CLK1N			
26	CLK2	I	1/2 frequency-divided CLK input.	—
27	NC	—	Leave this pin open.	—
28	CLKOUT	I	1/2 frequency-divided CLK output.	—
29	XCLKR	I	External clear. (Low: reset)	H
30	V _{SS}	—	GND	—
31	PRE	I	External preset. (Low: preset)	H
32	B2OUT0	O	Blue-2 data signal output.	—
33	B2OUT1	O	Blue-2 data signal output.	—
34	B2OUT2	O	Blue-2 data signal output.	—
35	B2OUT3	O	Blue-2 data signal output.	—
36	B2OUT4	O	Blue-2 data signal output.	—

Pin No.	Symbol	I/O	Description	Input processing
37	B2OUT5	O	Blue-2 data signal output.	—
38	B2OUT6	O	Blue-2 data signal output.	—
39	B2OUT7	O	Blue-2 data signal output.	—
40	V _{DD}	—	Power supply.	—
41	V _{SS}	—	GND	—
42	B2OUT8	O	Blue-2 data signal output.	—
43	B2OUT9	O	Blue-2 data signal output.	—
44	B1OUT0	O	Blue-1 data signal output.	—
45	B1OUT1	O	Blue-1 data signal output.	—
46	B1OUT2	O	Blue-1 data signal output.	—
47	B1OUT3	O	Blue-1 data signal output.	—
48	B1OUT4	O	Blue-1 data signal output.	—
49	B1OUT5	O	Blue-1 data signal output.	—
50	V _{SS}	—	GND	—
51	B1OUT6	O	Blue-1 data signal output.	—
52	B1OUT7	O	Blue-1 data signal output.	—
53	B1OUT8	O	Blue-1 data signal output.	—
54	B1OUT9	O	Blue-1 data signal output.	—
55	G2OUT0	O	Green-2 data signal output.	—
56	G2OUT1	O	Green-2 data signal output.	—
57	G2OUT2	O	Green-2 data signal output.	—
58	G2OUT3	O	Green-2 data signal output.	—
59	V _{SS}	—	GND	—
60	V _{DD}	—	Power supply.	—
61	G2OUT4	O	Green-2 data signal output.	—
62	G2OUT5	O	Green-2 data signal output.	—
63	G2OUT6	O	Green-2 data signal output.	—
64	G2OUT7	O	Green-2 data signal output.	—
65	G2OUT8	O	Green-2 data signal output.	—
66	G2OUT9	O	Green-2 data signal output.	—
67	G1OUT0	O	Green-1 data signal output.	—
68	G1OUT1	O	Green-1 data signal output.	—
69	G1OUT2	O	Green-1 data signal output.	—
70	V _{SS}	—	GND	—
71	G1OUT3	O	Green-1 data signal output.	—
72	G1OUT4	O	Green-1 data signal output.	—
73	G1OUT5	O	Green-1 data signal output.	—

Pin No.	Symbol	I/O	Description	Input processing
74	G1OUT6	O	Green-1 data signal output.	—
75	G1OUT7	O	Green-1 data signal output.	—
76	G1OUT8	O	Green-1 data signal output.	—
77	G1OUT9	O	Green-1 data signal output.	—
78	R2OUT0	O	Red-2 data signal output.	—
79	R2OUT1	O	Red-2 data signal output.	—
80	V _{DD}	—	Power supply.	—
81	V _{SS}	—	GND	—
82	R2OUT2	O	Red-2 data signal output.	—
83	R2OUT3	O	Red-2 data signal output.	—
84	R2OUT4	O	Red-2 data signal output.	—
85	R2OUT5	O	Red-2 data signal output.	—
86	R2OUT6	O	Red-2 data signal output.	—
87	R2OUT7	O	Red-2 data signal output.	—
88	R2OUT8	O	Red-2 data signal output.	—
89	R2OUT9	O	Red-2 data signal output.	—
90	V _{SS}	—	GND	—
91	R1OUT0	O	Red-1 data signal output.	—
92	R1OUT1	O	Red-1 data signal output.	—
93	R1OUT2	O	Red-1 data signal output.	—
94	R1OUT3	O	Red-1 data signal output.	—
95	R1OUT4	O	Red-1 data signal output.	—
96	R1OUT5	O	Red-1 data signal output.	—
97	R1OUT6	O	Red-1 data signal output.	—
98	R1OUT7	O	Red-1 data signal output.	—
99	R1OUT8	O	Red-1 data signal output.	—
100	V _{DD}	—	Power supply.	—
101	R1OUT9	O	Red-1 data signal output.	—
102	TEST1	—	Test pin. (Connect to GND.)	—
103	TEST2	—	Test pin. (Connect to GND.)	—
104	TEST3	—	Test pin. (Connect to GND.)	—
105	TEST4	—	Test pin. (Connect to V _{DD} .)	—
106	TEST5	—	Test pin. (Connect to V _{DD} .)	—
107	TEST6	—	Test pin. (Connect to V _{DD} .)	—
108	TEST7	—	Test pin. (Connect to V _{DD} .)	—
109	TEST8	—	Test pin. (Connect to V _{DD} .)	—
110	V _{SS}	—	GND	—

Pin No.	Symbol	I/O	Description	Input processing
111	TEST9	—	Test pin. (Connect to V _{DD} .)	—
112	TEST10	—	Test pin. (Connect to GND.)	—
113	TEST11	—	Test pin. (Leave this pin open.)	—
114	R1IN7	I	Red-1 data signal input.	—
115	R1IN6	I	Red-1 data signal input.	—
116	R1IN5	I	Red-1 data signal input.	—
117	R1IN4	I	Red-1 data signal input.	—
118	R1IN3	I	Red-1 data signal input.	—
119	R1IN2	I	Red-1 data signal input.	—
120	V _{DD}	—	Power supply.	—
121	V _{SS}	—	GND	—
122	R1IN1	I	Red-1 data signal input.	—
123	R1IN0	I	Red-1 data signal input.	—
124	R2IN7	I	Red-2 data signal input.	—
125	R2IN6	I	Red-2 data signal input.	—
126	R2IN5	I	Red-2 data signal input.	—
127	R2IN4	I	Red-2 data signal input.	—
128	R2IN3	I	Red-2 data signal input.	—
129	R2IN2	I	Red-2 data signal input.	—
130	V _{SS}	—	GND	—
131	R2IN1	I	Red-2 data signal input.	—
132	R2IN0	I	Red-2 data signal input.	—
133	G1IN7	I	Green-1 data signal input.	—
134	G1IN6	I	Green-1 data signal input.	—
135	G1IN5	I	Green-1 data signal input.	—
136	G1IN4	I	Green-1 data signal input.	—
137	G1IN3	I	Green-1 data signal input.	—
138	G1IN2	I	Green-1 data signal input.	—
139	V _{SS}	—	Power supply.	—
140	V _{DD}	—	GND	—
141	G1IN1	I	Green-1 data signal input.	—
142	G1IN0	I	Green-1 data signal input.	—
143	G2IN7	I	Green-2 data signal input.	—
144	G2IN6	I	Green-2 data signal input.	—
145	G2IN5	I	Green-2 data signal input.	—
146	G2IN4	I	Green-2 data signal input.	—
147	G2IN3	I	Green-2 data signal input.	—

Pin No.	Symbol	I/O	Description	Input processing
148	G2IN2	I	Green-2 data signal input.	—
149	G2IN1	I	Green-2 data signal input.	—
150	V _{SS}	—	GND	—
151	G2IN0	I	Green-2 data signal input.	—
152	B1IN7	I	Blue-1 data signal input.	—
153	B1IN6	I	Blue-1 data signal input.	—
154	B1IN5	I	Blue-1 data signal input.	—
155	B1IN4	I	Blue-1 data signal input.	—
156	B1IN3	I	Blue-1 data signal input.	—
157	B1IN2	I	Blue-1 data signal input.	—
158	B1IN1	I	Blue-1 data signal input.	—
159	B1IN0	I	Blue-1 data signal input.	—
160	V _{DD}	—	Power supply.	—

Electrical Characteristics

DC Characteristics

(T_{opr} = –20 to +75°C, V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	V _{DD}	—	3.0	3.3	3.6	V	—
Input voltage 1	V _{IH1}	CMOS input cell	0.65V _{DD}	—	V _{DD}	V	CLK2
	V _{IL1}		V _{SS}	—	0.25V _{DD}		
Input voltage 2	V _{IH2}	CMOS Schmitt trigger input cell	0.8V _{DD}	—	V _{DD}	V	*1
	V _{IL2}		V _{SS}	—	0.2V _{DD}		
Input voltage 3	VC (center level)	Low-amplitude differential input	(V _{DD} × 0.606) – 0.1	V _{DD} × 0.606	(V _{DD} × 0.606) + 0.1	V	CLK1P, CLK1N
	V _{IH3} *2		V _{IL3} + 0.3	—	V _{DD}		
	V _{IL3} *2		V _{SS}	—	V _{IH3} – 0.3		
Output voltage	V _{OH}	I _{OH} = –4mA	V _{DD} – 0.5	—	V _{DD}	V	All output pins
	V _{OL}	I _{OL} = 4mA	V _{SS}	—	0.4		
Current consumption	I _{DD}	CLK1 = 100MHz V _{DD} = 3.3V Output load = 30pF	—	—	150	mA	

*1 Input pins other than those indicated in items of Input voltage 1 and Input voltage 3.

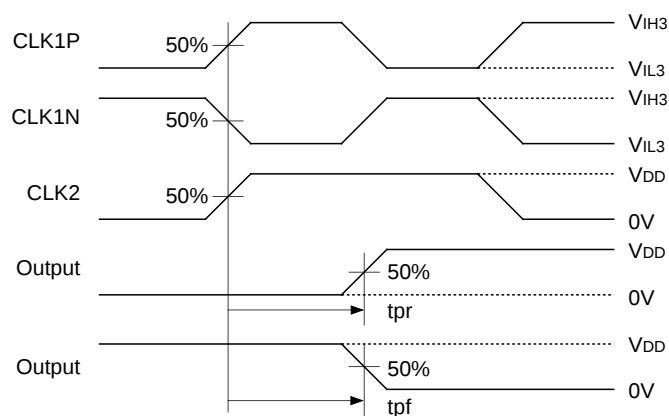
*2 V_{IH3} > (Maximum VC value) and V_{IL3} < (Minimum VC value).

AC Characteristics

(T_{opr} = –20 to +75°C, V_{DD} = 3.3 ± 0.3V, V_{SS} = 0V)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Clock input cycle	—	CLK1P, CLK1N	—	10	—	—	ns
		CLK2	—	20	—	—	ns
Output rise/fall delay time	t _{pr} /t _{pf}	All output pins	CL = 30pF	—	—	20	ns

Timing Definition



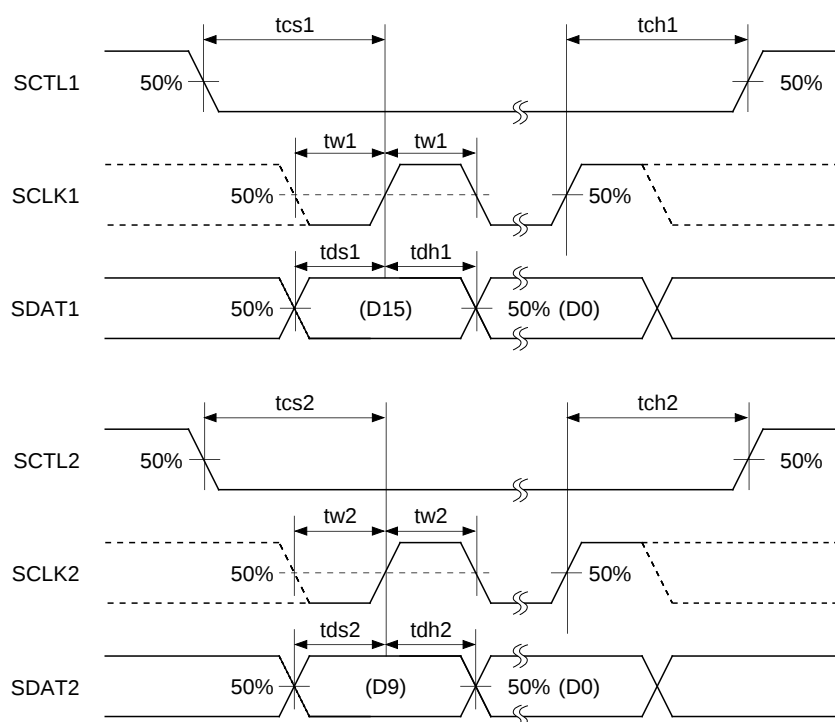
Serial I/F Block AC Characteristics

(Topr = -20 to +75°C, V_{DD} = 3.3 ± 0.3V, V_{SS} = 0V)

Item	Symbol	Min.	Typ.	Max.
SCTL1 setup time, activated by the rising edge of SCLK1	tcs1	8T ^{*3}	—	—
SCTL1 hold time, activated by the rising edge of SCLK1	tch1	8T	—	—
SDAT1 setup time, activated by the rising edge of SCLK1	tds1	4T	—	—
SDAT1 hold time, activated by the rising edge of SCLK1	tdh1	4T	—	—
SCLK1 pulse width	tw1	4T	—	—
SCTL2 setup time, activated by the rising edge of SCLK2	tcs2	8T	—	—
SCTL2 hold time, activated by the rising edge of SCLK2	tch2	8T	—	—
SDAT2 setup time, activated by the rising edge of SCLK2	tds2	4T	—	—
SDAT2 hold time, activated by the rising edge of SCLK2	tdh2	4T	—	—
SCLK2 pulse width	tw2	4T	—	—

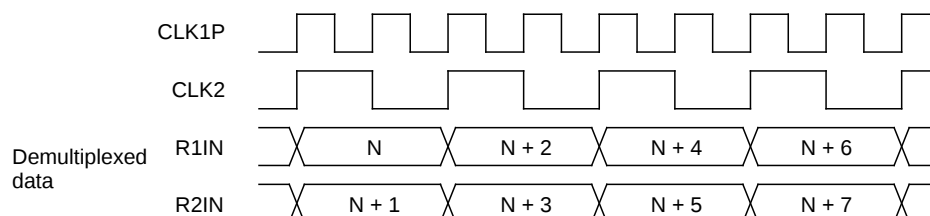
*3 T: master clock (CLK1P, CLK1N) cycle [ns]

Timing Definition



Description of Operation

The internal operation of this IC is performed at 1/2 the speed of the system master clock. Therefore, the input digital data must be demultiplexed to 1:2 as shown in the figure below. Also, the input clock can be either the master clock or the 1/2 frequency-divided master clock. All internal arithmetic processing is performed in parallel, and the digital data is also output in the 1:2 demultiplexed state. The operation of this IC is described below.

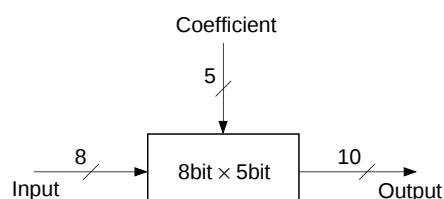


Description of Signal Processing Functions

The various signal processing functions are described below. Note that the coefficients used for each arithmetic operation are set through the serial I/F-1 and serial I/F-2 blocks. See the individual descriptions of the serial I/F-1 and serial I/F-2 blocks for a detailed description of these serial I/F blocks.

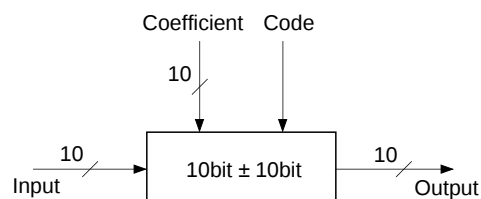
1) Gain block

This block performs multiplication. Multiplication is performed using the 8-bit data input to this IC and a 5-bit coefficient, and the upper 10 bits of the arithmetic results are output to the rear-end arithmetic block. The coefficient used during this arithmetic operation is set from outside the IC through the serial I/F-1 block.



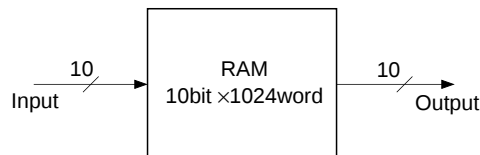
2) Bright block

This block performs addition and subtraction. The 10-bit arithmetic results from the gain block, a 10-bit coefficient, and a 1-bit code are used as the inputs. Addition is performed when the code = 0, and subtraction when the code = 1. However, when performing subtraction, set an arithmetic coefficient that is the two's complement of the number to be subtracted. Also, when the arithmetic results exceed 3FF_H or fall below 000_H, these results are fixed to 3FF_H or 000_H, respectively, and then output as 10 bits. The coefficient used during these arithmetic operations is set from outside the IC through the serial I/F-1 block.



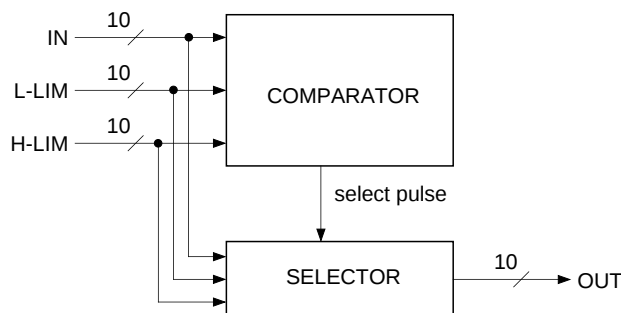
3) Gamma block

This block performs gamma correction for the gain- and bright-adjusted signal. This block comprises a 10-bit $\times$ 1024 word RAM, and the gamma correction curve can be set as desired. The results of this correction are output as 10 bits. The RAM data is set through the serial I/F-2 block during power-on. Note that RAM output is undetermined while data is set in this RAM. Therefore, the RAM data cannot be changed during arithmetic processing.



4) Limiter block

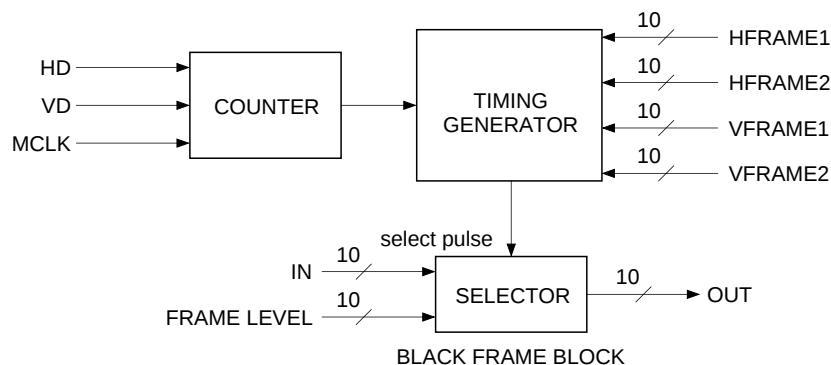
This block limits the output signal so that it does not exceed a certain range. The input signal is compared with the low-side limiter level L-LIM and high-side limiter level H-LIM coefficients by the comparator as shown in the figure below. The selector receives the comparator's arithmetic results and fixes the output to the L-LIM level when $IN \leq L-LIM$ or to the H-LIM level when $H-LIM < IN$. When $L-LIM < IN \leq H-LIM$, the input is output as is. Note that the two coefficients should constantly maintain the relationship $L-LIM < H-LIM$. Also, when $L-LIM = H-LIM = 000H$, limiter processing is not performed. The arithmetic coefficients are set through the serial I/F-1 block.



5) Black frame block

This block can perform processing to fix the blanking period of the video signal to the desired level regardless of the front-end signal processing results. This is effective when attempting to display a video signal which has been pixel-converted using a scan converter, etc., on a LCD panel or other display with a fixed number of pixels. If the number of pixels calculated from the effective period of the video signal to be displayed is less than the number of pixels of the display on which the signal is to be displayed, the blanking period of the video signal is displayed in the excess pixels. At this time, the displayed blanking period can be fixed to the desired level regardless of the gain, bright, gamma or other picture quality adjustment results by processing with this block.

This black frame processing is performed by switching the input data and the black frame black level data with the selector according to the select pulse generated by the counter and the timing generator. The black frame display range is set through the serial I/F-1 block. The horizontal direction can be set in 1-dot units, and the vertical direction, in 1-line units. Note that the 1-dot unit for the horizontal direction is the 1-dot units when viewed with the video signal displayed. Also, the black frame black level data can be set by 10 bits.



Sync Signal Input Pins (HD and VD) and Sync Signal Polarity Selection Pins (HDPOL and VDPOL)

Horizontal and vertical separate sync signals are input to the HD (Pin 17) and VD (Pin 18). The polarity of the input sync signals is set by the HDPOL (Pin 19) and VDPOL (Pin 21) as shown in the table below.

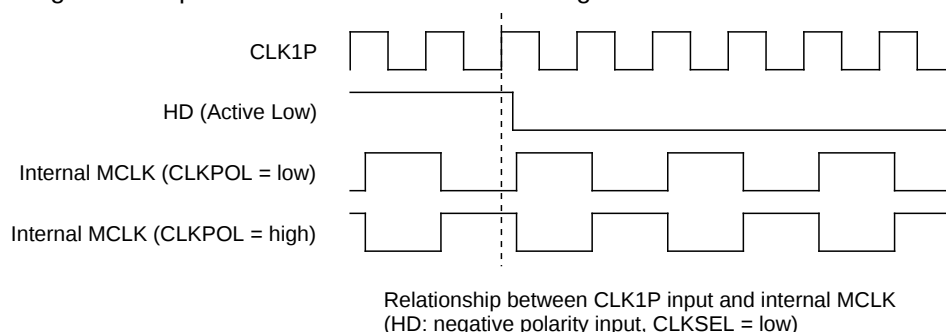
Setting Symbol	H	L
HDPOL	Positive polarity input	Negative polarity input
VDPOL	Positive polarity input	Negative polarity input

Master Clock Input Pins (CLK1P, CLK1N and CLK2), Clock Selection Pin (CLKSEL) and Clock Polarity Selection Pin (CLKPOL)

This IC does not have a built-in phase comparator, so phase comparison is performed externally and a phase-adjusted clock input. There are two sets of clock input pins, and either set may be used. CLK1P and CLK1N (Pins 24 and 25) input a small-amplitude differential input (center level 2.0V, amplitude $\pm 0.4V$) master clock. These pins can input a clock of up to 100MHz (max.), and can interface with ECL and PECL. The CLK2 (Pin 26) inputs the 1/2 frequency-divided master clock at CMOS level. This pin can input a clock of up to 50MHz (max.). The various input functions are described below.

1) CLK input (CLKSEL = low)

CLK1P and CLK1N (Pins 24 and 25) input a small-amplitude differential clock. At this time, the clock input from CLK1P and CLK1N is selected by setting CLKSEL = low. The input clock is 1/2 frequency divided inside the IC. This frequency-division circuit is reset at the edge of the HD pulse input from Pin 17. When HD is a negative polarity input, the circuit is reset at the falling edge, and when a positive polarity input, at the rising edge. Also, the phase of this 1/2 frequency-divided clock with respect to the input clock can be selected by the CLKPOL setting. This simplified waveform is shown in the figure below.



2) 1/2 frequency-divided CLK input (CLKSEL = high)

CLK2 (Pin 26) inputs the 1/2 frequency-divided CLK. At this time, the 1/2 frequency-divided CLK input is selected by setting CLKSEL = high.

Digital Data Input Pins (R1IN, R2IN, G1IN, G2IN, B1IN and B2IN)

These pins input digital data that has been demultiplexed to 1:2. The Red signal is input to R1IN (Pins 114 to 119, 122 and 123) and R2IN (Pins 124 to 129, 131 and 132), the Green signal to G1IN (Pins 133 to 138, 141 and 142) and G2IN (Pins 143 to 149 and 151), and the Blue signal to B1IN (Pins 152 to 159) and B2IN (Pins 2 to 9).

Clock Output Pin (CLKOUT)

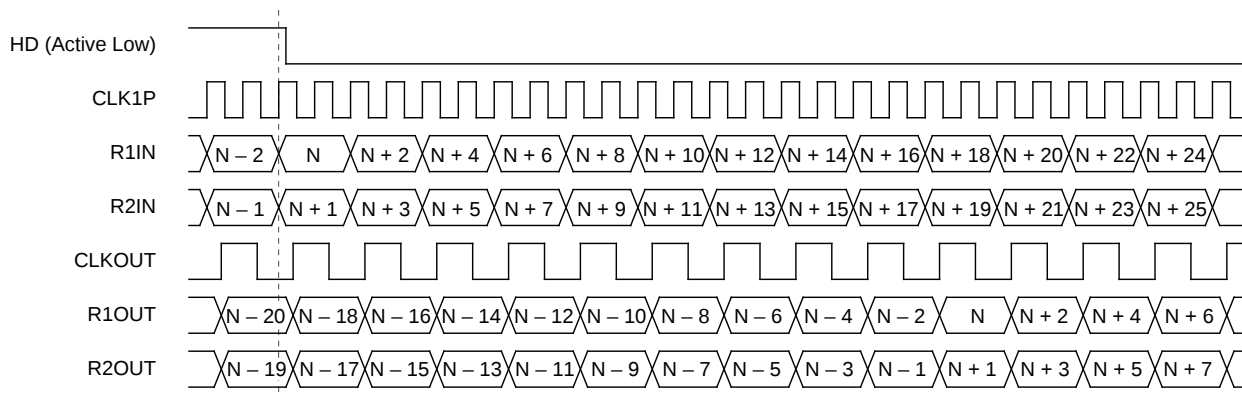
The internal master clock is output from the CLKOUT pin (Pin 28).

Digital Data Output Pins (R1OUT, R2OUT, G1OUT, G2OUT, B1OUT and B2OUT)

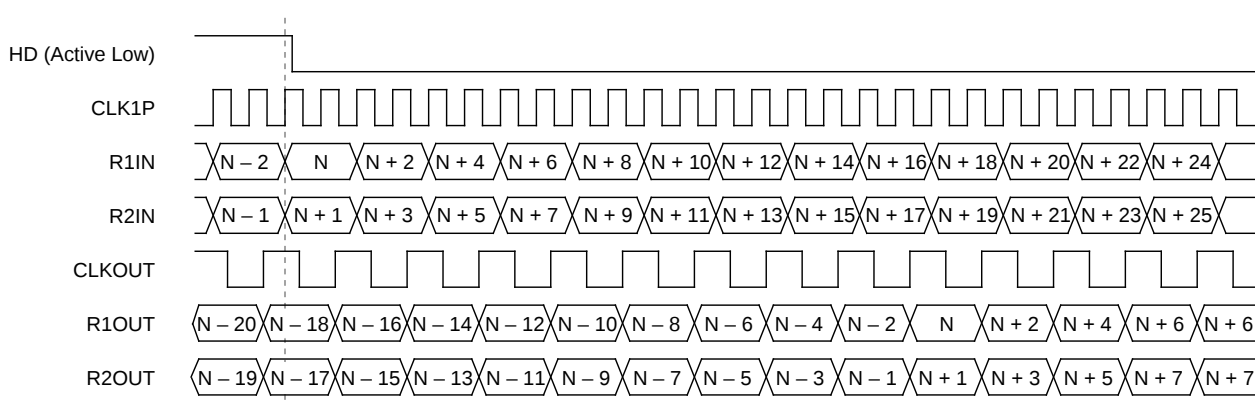
These pins output the arithmetic results data in the 1:2 demultiplexed state. The Red signal is output from R1OUT (Pins 91 to 99 and 101) and R2OUT (Pins 78, 79 and 82 to 89), the Green signal from G1OUT (Pins 67 to 69 and 71 to 77) and G2OUT (Pins 55 to 58 and 61 to 66), and the Blue signal from B1OUT (Pins 44 to 49 and 51 to 54) and B2OUT (Pins 32 to 39, 42 and 43).

Relationship Between Clock and Data I/O

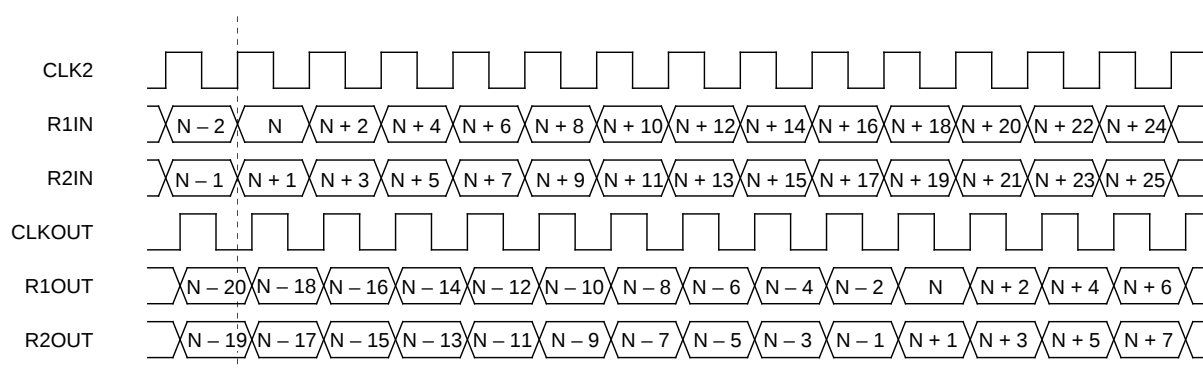
(1) CLK input (CLKPOL = low)



(2) CLK input (CLKPOL = high)



(3) 1/2 frequency-divided CLK input



System Clear Pin (XCLR)

All internal circuits are initialized by setting the XCLR (Pin 29) low. Initialization should be performed during power-on.

Serial Data Initial Setting Pin (PRE)

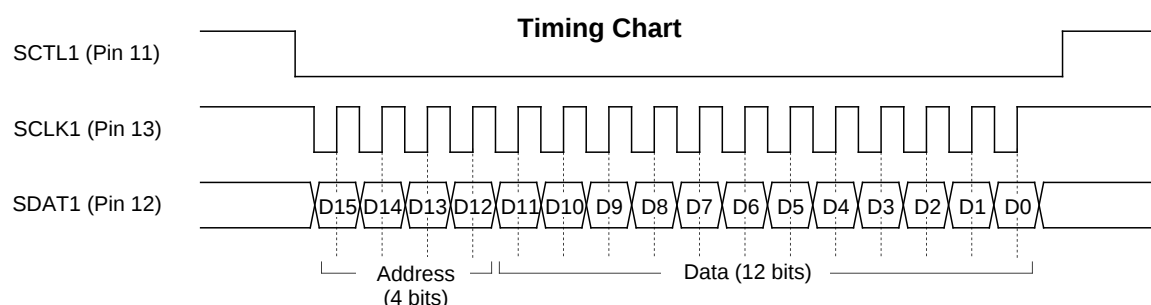
The coefficients set to each arithmetic block from the serial I/F blocks are initialized by setting the PRE (Pin 31) low. See the description of serial data for the initialized data.

Serial I/F-1 Block

This block sets the coefficients for the arithmetic processing other than gamma correction. Data is input in 16-bit units consisting of 4 address bits and 12 data bits as shown in the timing chart below, and the SDAT value is loaded at the rising edge of SCLK. Also, when initialization is performed using the PRE (Pin 31), this block sets each data to the default value.

The timing chart and data format when sending serial data are as follows.

When attempting to set data twice or more consecutively at the same address with the serial I/F-1 block, be sure to set data at a different address one time before setting the next data at the target address again. Addresses D_H and E_H can be used as the dummy address in these cases.



Data Format

Address	Data												Setting contents
D15 to 12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	—	—	—	—	—	—	—	RG4	RG3	RG2	RG1	RG0	Red gain
1	—	—	—	—	—	—	—	GG4	GG3	GG2	GG1	GG0	Green gain
2	—	—	—	—	—	—	—	BG4	BG3	BG2	BG1	BG0	Blue gain
3	—	RBF	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	Red bright
4	—	GBF	GB9	GB8	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	Green bright
5	—	BBF	BB9	BB8	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0	Blue bright
6	—	—	LL9	LL8	LL7	LL6	LL5	LL4	LL3	LL2	LL1	LL0	Low-side limiter level
7	—	—	HL9	HL8	HL7	HL6	HL5	HL4	HL3	HL2	HL1	HL0	High-side limiter level
8	—	H1F10	H1F9	H1F8	H1F7	H1F6	H1F5	H1F4	H1F3	H1F2	H1F1	H1F0	Horizontal black frame range 1
9	—	H2F10	H2F9	H2F8	H2F7	H2F6	H2F5	H2F4	H2F3	H2F2	H2F1	H2F0	Horizontal black frame range 2
A	—	V1F10	V1F9	V1F8	V1F7	V1F6	V1F5	V1F4	V1F3	V1F2	V1F1	V1F0	Vertical black frame range 1
B	—	V2F10	V2F9	V2F8	V2F7	V2F6	V2F5	V2F4	V2F3	V2F2	V2F1	V2F0	Vertical black frame range 2
C	—	—	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0	Black frame level

Note) —: Don't care

The detailed setting contents are described below.

(a) Gain arithmetic coefficient setting

This sets the R, G and B gain arithmetic coefficients. Each coefficient can be set by 5 bits.
The default values are all 08H.

(b) Bright arithmetic coefficient setting

This sets the R, G and B bright arithmetic coefficients. Each coefficient can be set by 11 bits. Within the coefficients, the 10 bits from D0 to D9 are the operand data when performing addition and subtraction, and D10 is the code bit. Addition is performed when the code bit = 0, and subtraction when the code bit = 1. At this time, set a twos complement for the operand data.

The default values are all 000H.

(c) Limiter arithmetic coefficient setting

This sets the low-side and high-side limiter arithmetic coefficients. Each coefficient can be set by 10 bits. When performing limiter processing, set the data so that the relationship $LL < HL$ is maintained at all times. Also, when 000H is set for both LL and HL, this processing is not performed.

The default values are 000H.

(d) Black frame display range setting

This sets the black frame display range coefficients. Both the horizontal and vertical directions can be set by 11 bits.

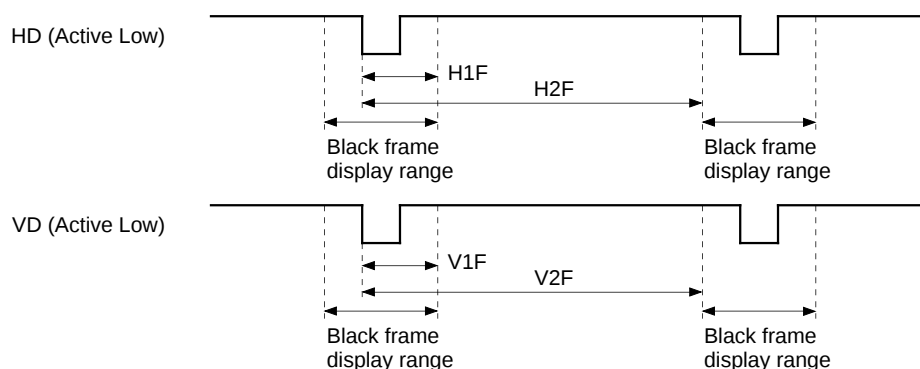
The horizontal direction display range can be set in 1-dot units using the edge of the HD input as the reference. The reference is the falling edge when HD is a negative polarity input, and the rising edge when HD is a positive polarity input. When the master clock is CLK input, set the value of "display range - 2" for both H1F and H2F. When the master clock is 1/2 frequency-divided CLK input, set the value of "display range" for both H1F and H2F.

The vertical direction display range can be set in 1-line units using the edge of the VD input as the reference. The reference is the falling edge when VD is a negative polarity input, and the rising edge when VD is a positive polarity input. Set the value of "display range" for both V1F and V2F.

When performing black frame processing, be sure to set a value other than 000H for H1F, H2F, V1F and V2F. Also, it is not possible to set only the horizontal direction or the vertical direction.

And further, the black frame level coefficients can be set by 10bits.

The default values are all 000H.

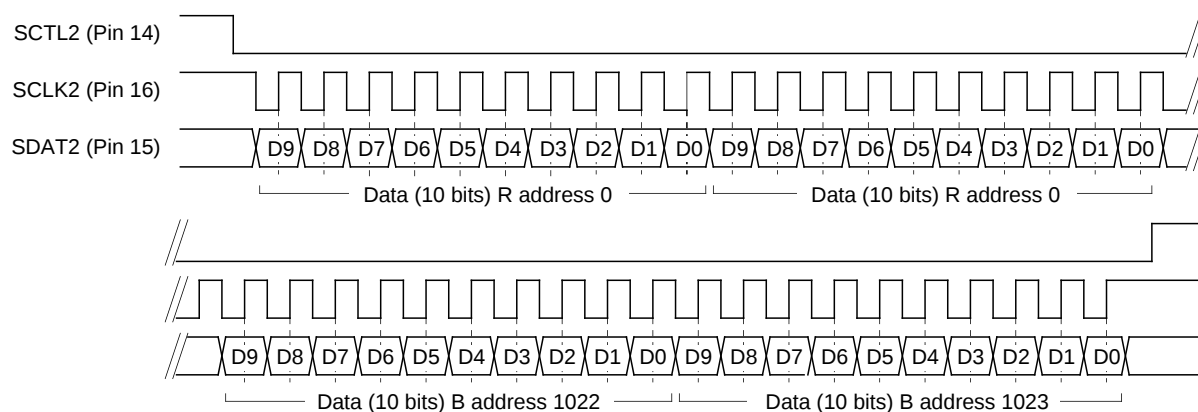


Serial I/F-2 Block

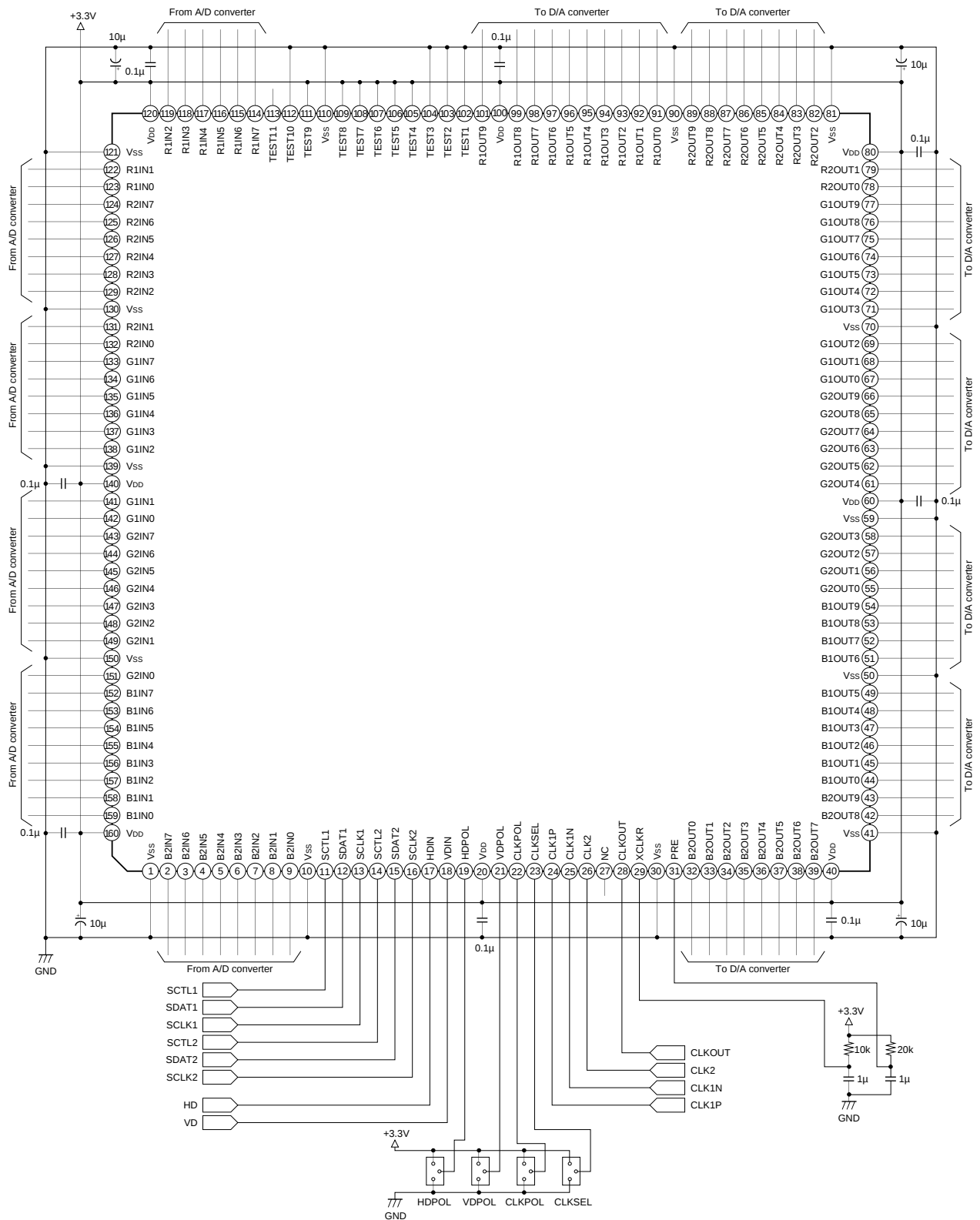
Data is set in the gamma block RAM from this block. The RAM output values of this IC are undetermined during power-on. Therefore, be sure to set this data. The RAM have a 10-bit $\times$ 1024 word configuration. When setting data, set the data continuously from addresses 0 to 1023 of the R, G and B RAM.

The timing chart when sending serial data is as follows.

Timing Chart



Application Circuit

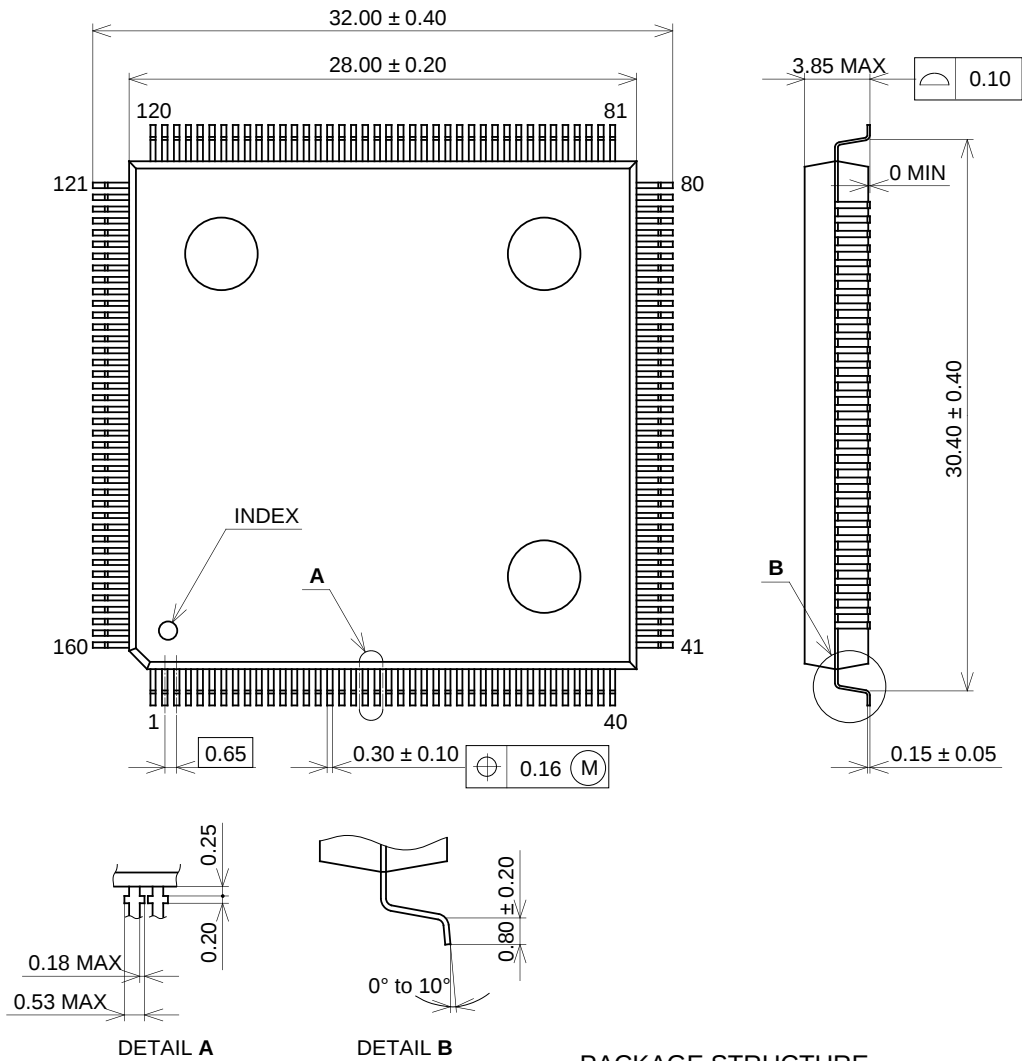


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

Unit: mm

160PIN QFP(PLASTIC)



SONY CODE	QFP-160P-L021
EIAJ CODE	QFP160-P-2828
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.4g