

Sync Signal, Timing Signal Generator for CCD Cameras

Description

The CXD1261AR is an IC which generates the sync signals and timing signals required for a camera system that uses the monochrome CCD image sensor (760H) such as the ICX038/039 and ICX058/059.

Features

- Compatible with monochrome (EIA/CCIR) systems
- Built-in electronic shutter function
- Built-in driver for the horizontal (H) clock
- Built-in SG and TG functions

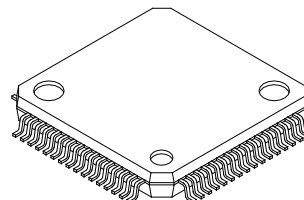
Applications

CCD camera systems

Structure

Silicon gate CMOS

64 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

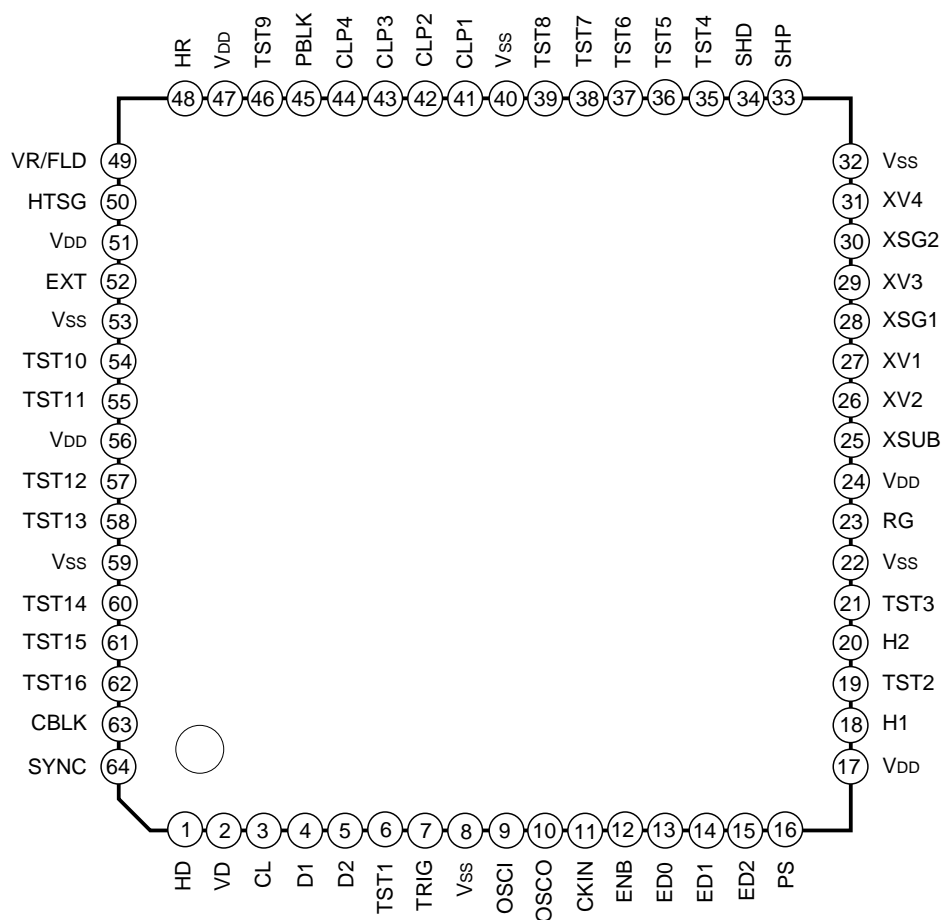
| | | | |
|-------------------------|------------------|--|----|
| • Supply voltage | V _{DD} | V _{SS} – 0.5 to +7.0 | V |
| • Input voltage | V _I | V _{SS} – 0.5 to V _{DD} + 0.5 | V |
| • Output voltage | V _O | V _{SS} – 0.5 to V _{DD} + 0.5 | V |
| • Operating temperature | T _{opr} | –20 to +75 | °C |
| • Storage temperature | T _{stg} | –55 to +150 | °C |

Recommended Operating Conditions

| | | | |
|-------------------------|------------------|------------|----|
| • Supply voltage | V _{DD} | 5.0 ± 0.25 | V |
| • Operating temperature | T _{opr} | –20 to +75 | °C |

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Pin Configuration



| Mode name | Pin No. | PRESET | L | H |
|-----------|---------|--------|---------------|----------------|
| D1 | 4 | L | EIA | CCIR |
| D2 | 5 | L | Field readout | Frame readout |
| ENB | 12 | H | Normal | Shutter |
| ED0 | 13 | H | Shutter speed | |
| ED1 | 14 | H | | |
| ED2 | 15 | H | | |
| PS | 16 | H | Serial input | Parallel input |
| EXT | 52 | L | Internal | External |
| TST1 | 6 | — | Normally High | |
| TST13 | 58 | — | Normally Low | |

Note) Normally open for TST except as shown in the above table.

* During frame accumulation (readout), low-speed shutter does not operate normally.

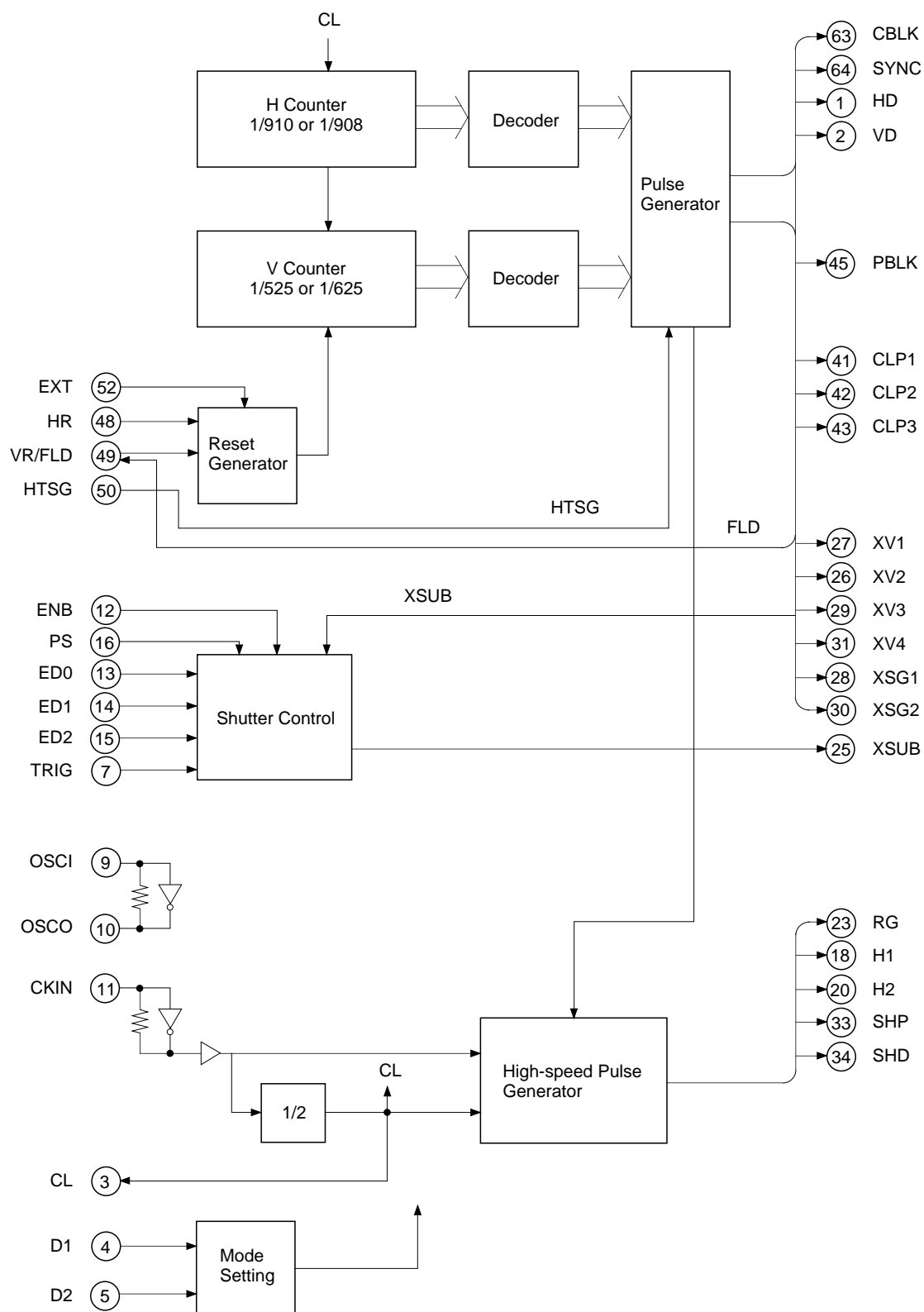
Pin Description

| Pin No. | Symbol | I/O | Description |
|---------|--------|-----|---|
| 1 | HD | O | Horizontal drive pulse |
| 2 | VD | O | Vertical drive pulse |
| 3 | CL | O | CKIN 2 frequency divided output (EIA: 14.318MHz, CCIR: 14.1875MHz) |
| 4 | D1 | I | Mode switching; low: EIA; high: CCIR (with pull-down resistor) |
| 5 | D2 | I | Mode switching; low: field readout; high: frame readout* (with pull-down resistor) |
| 6 | TST1 | I | Test input, fixed to high |
| 7 | TRIG | I | Shutter speed setting pulse (with pull-up resistor) |
| 8 | Vss | — | GND |
| 9 | OSCI | I | Oscillating cell input |
| 10 | OSCO | O | Oscillating cell output |
| 11 | CKIN | I | Clock input (EIA: 28.636MHz, CCIR: 28.375MHz) |
| 12 | ENB | I | Shutter switching; low: normal; high: shutter (with pull-up resistor) |
| 13 | ED0 | I | Shutter speed control (with pull-up resistor) |
| 14 | ED1 | I | Shutter speed control (with pull-up resistor) |
| 15 | ED2 | I | Shutter speed control (with pull-up resistor) |
| 16 | PS | I | Shutter speed setting method switching; low: serial; high: parallel (with pull-up resistor) |
| 17 | VDD | — | Power supply |
| 18 | H1 | O | Horizontal register drive clock |
| 19 | TST2 | I | Test input, normally open (with pull-down resistor) |
| 20 | H2 | O | Horizontal register drive clock |
| 21 | TST3 | I | Test input, normally open (with pull-down resistor) |
| 22 | Vss | — | GND |
| 23 | RG | O | Reset gate pulse |
| 24 | VDD | — | Power supply |
| 25 | XSUB | O | Discharge pulse |
| 26 | XV2 | O | Vertical register drive clock |
| 27 | XV1 | O | Vertical register drive clock |
| 28 | XSG1 | O | Sensor charge readout pulse |
| 29 | XV3 | O | Vertical register drive clock |
| 30 | XSG2 | O | Sensor charge readout pulse |
| 31 | XV4 | O | Vertical register drive clock |
| 32 | Vss | — | GND |

* The CCD image sensor characteristics are guaranteed for field accumulation operation.

| Pin No. | Symbol | I/O | Description |
|---------|-----------------|-----|--|
| 33 | SHP | O | Precharge level sample-and-hold pulse |
| 34 | SHD | O | Data sample-and-hold pulse |
| 35 | TST4 | O | Test output, normally open |
| 36 | TST5 | O | Test output, normally open |
| 37 | TST6 | O | Test output, normally open |
| 38 | TST7 | O | Test output, normally open |
| 39 | TST8 | O | Test output, normally open |
| 40 | V _{SS} | — | GND |
| 41 | CLP1 | O | Clamp pulse |
| 42 | CLP2 | O | Clamp pulse |
| 43 | CLP3 | O | Clamp pulse |
| 44 | CLP4 | O | Clamp pulse |
| 45 | PBLK | O | Blanking cleaning pulse |
| 46 | TST9 | O | Test output, normally open |
| 47 | V _{DD} | — | Power supply |
| 48 | HR | I | H reset pulse |
| 49 | VR/FLD | I | V reset pulse (FLD output when EXT = low) |
| 50 | HTSG | I | HTSG input; low: XSG1, 2 on; high: off (valid only when EXT = low) Fixed to low when EXT = high |
| 51 | V _{DD} | — | Power supply |
| 52 | EXT | I | Sync mode switching; low: internal; high: external sync (with pull-down resistor) |
| 53 | V _{SS} | — | GND |
| 54 | TST10 | I | Test input, normally open (with pull-down resistor) |
| 55 | TST11 | O | Test output, normally open |
| 56 | V _{DD} | — | Power supply |
| 57 | TST12 | O | Test output, normally open |
| 58 | TST13 | I | Test input, fixed to low |
| 59 | V _{SS} | — | GND |
| 60 | TST14 | O | Test output, normally open |
| 61 | TST15 | O | Test output, normally open |
| 62 | TST16 | O | Test output, normally open |
| 63 | CBLK | O | Composite blanking pulse |
| 64 | SYNC | O | Composite sync pulse |

Block Diagram



Electrical Characteristics

1) DC characteristics

(V_{DD} = 5V ± 0.25V, T_{opr} = -20 to +75°C)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---------------------|------------------|--|-----------------------|------|--------------------|------|
| Supply voltage | V _{DD} | | 4.75 | 5.0 | 5.25 | V |
| Input voltage | V _{IH1} | | 0.7V _{DD} | | | V |
| | V _{IL1} | | | | 0.3V _{DD} | V |
| Output voltage 1 *1 | V _{OH1} | I _{OH} = -2mA | V _{DD} - 0.5 | | | V |
| | V _{OL1} | I _{OL} = 4mA | | | 0.4 | V |
| Output voltage 2 *2 | V _{OH2} | I _{OH} = -4mA | V _{DD} - 0.5 | | | V |
| | V _{OL2} | I _{OL} = 8mA | | | 0.4 | V |
| Output voltage 3 *3 | V _{OH3} | I _{OH} = -8mA | V _{DD} - 0.5 | | | V |
| | V _{OL3} | I _{OL} = 8mA | | | 0.4 | V |
| Output voltage 4 *4 | V _{OH4} | I _{OH} = -2mA | V _{DD} /2 | | | V |
| | V _{OL4} | I _{OL} = 2mA | | | V _{DD} /2 | V |
| Feedback resistor | R _{FB} | V _{IN} = V _{SS} or V _{DD} | 500k | 2M | 5M | Ω |
| Pull-up resistor | R _{PU} | V _{IL} = 0V | 40k | 100k | 250k | Ω |
| Pull-down resistor | R _{PD} | V _{IH} = V _{DD} | 40k | 100k | 250k | Ω |

2) I/O pin capacitance

(V_{DD} = V_I = 0V, f_M = 1MHz)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------------------|------------------|------|------|------|------|
| Input pin capacitance | C _{IN} | | | 9 | pF |
| Output pin capacitance | C _{OUT} | | | 11 | pF |
| Input/output pin capacitance | C _{I/O} | | | 11 | pF |

Note) *1 CLP1, CLP2, CLP3, CLP4, PBLK, CBLK, SYNC, VR, HD, VD, XSUB, XSG1, XSG2, XV1, XV2, XV3, XV4

*2 CL, RG, SHP, SHD

*3 H1, H2

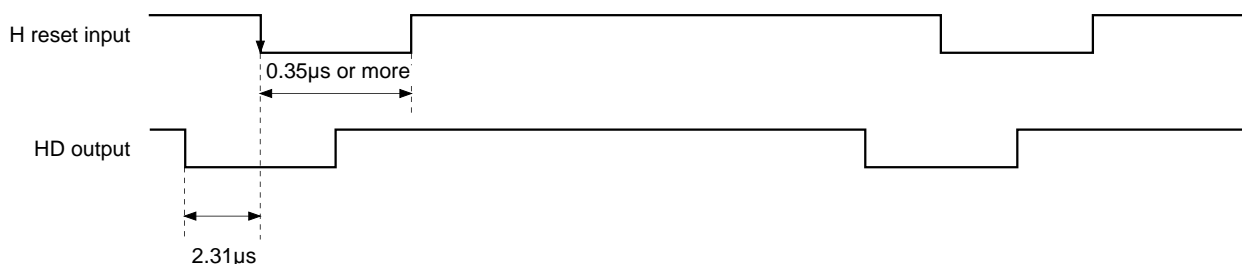
*4 OSCO

External Reset Description

H Reset (HR)

The reset is performed at the first falling edge of the reset pulse that was input; resets are not performed at subsequent edges as long as they do not deviate by two clock pulses ($0.14\mu\text{s}$) or more.

The minimum reset pulse width is $0.35\mu\text{s}$. In addition, HD immediately after a reset can not be guaranteed. The position at which the reset is performed is $2.31\mu\text{s}$ advanced after the H reset input.



V Reset (VR)

The falling edge of V reset pulse that was input is field identified by the phase difference with the internal signal (field judge pulse) defined by the falling edge of HD. And VD is reset in phase with V reset pulse.

When field judge pulse is low and V reset pulse falls,

EIA: VD falling edge after 262.5H is the relation between HD and VD of EVEN field.

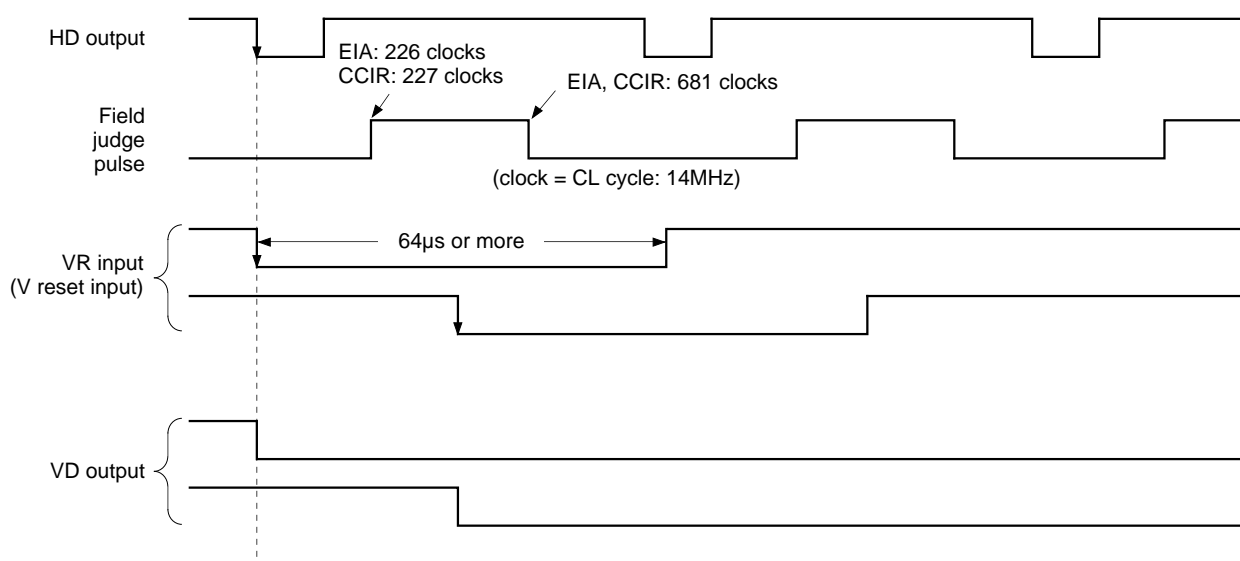
CCIR: VD falling edge after 312.5H is the relation between HD and VD of ODD field.

Also, when field judge pulse is high and V reset pulse falls,

EIA: VD falling edge after 262.5H is the relation between HD and VD of ODD field.

CCIR: VD falling edge after 312.5H is the relation between HD and VD of EVEN field.

The minimum reset pulse width is $64\mu\text{s}$. In addition, VD immediately after reset can not be guaranteed.

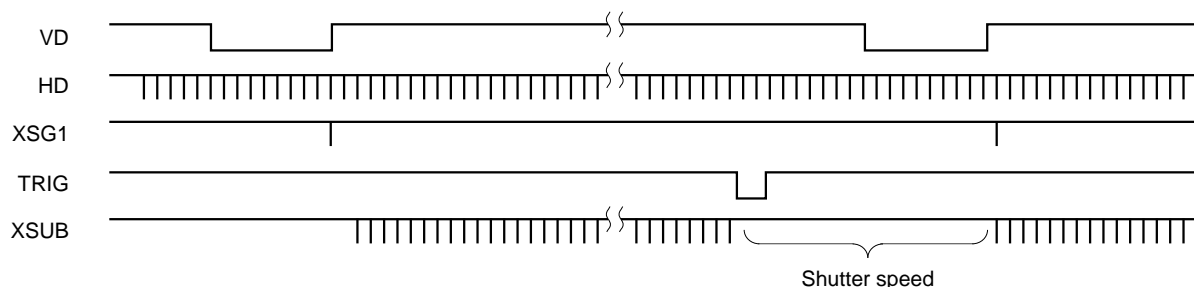


Electronic Shutter Description (During frame accumulation, low-speed shutter does not operate normally.)

The XSUB pulse timing changes according to the electronic shutter control described below. In addition, the ENB pin controls whether the XSUB pulse is output or not; this control has priority.

1. Continuously variable shutter (trigger mode)

- When using the normal shutter, either leave the TRIG pin open or connect it to the power supply.
- When using the continuous variable shutter, input the clock pulse to the TRIG pin.



The shutter speed is determined by sampling the XSUB pulse during the interval between the falling edge of XSG1 and the falling edge of TRIG, and then stopping the XSUB pulse during the interval between the falling edge of TRIG and the next falling edge of XSG1.

When using the TRIG pin to control the shutter speed, in order to broaden the control range it is necessary to use the ED0, 1, and 2 pins (described later) to set the shutter speed to 1/10000.

2. Normal shutter

2-1. Switching between parallel input and serial input

Parallel input or serial input can be selected as the method for inputting the data used to determine the shutter speed.

- Parallel input (PS = High):
Permits selection of eight shutter speeds by using three bits ED0, ED1, and ED2.
- Serial input (PS = Low):
Shutter speed is determined by inputting the strobe to ED0, CLK to ED1, and the data to ED2.

2-2. When using parallel input (PS = High)

Shutter speed table

Only the high-speed shutter is used when using parallel input (During frame accumulation, low-speed shutter does not operate normally.)

| D1 | ENB | ED0 | ED1 | ED2 | Shutter speed |
|----|-----|-----|-----|-----|----------------|
| X | L | X | X | X | Shutter off *1 |
| L | H | H | H | H | 1/60 (s) *2 |
| H | H | H | H | H | 1/50 (s) *3 |
| L | H | L | H | H | 1/100 (s) |
| H | H | L | H | H | 1/120 (s) |
| X | H | H | L | H | 1/250 (s) |
| X | H | L | L | H | 1/500 (s) |
| X | H | H | H | L | 1/1000 (s) |
| X | H | L | H | L | 1/2000 (s) |
| X | H | H | L | L | 1/4000 (s) |
| X | H | L | L | L | 1/10000 (s) |

*1 XSUB (shutter pulse) is not generated.

*2 Accumulation time is as follows regardless of field accumulation/frame accumulation.

D1 = Low (EIA), 1/60 (s)

D2 = High (CCIR), 1/50 (s)

(Pseudo field readout during frame accumulation.)

2-3. When using serial input (PS = Low)

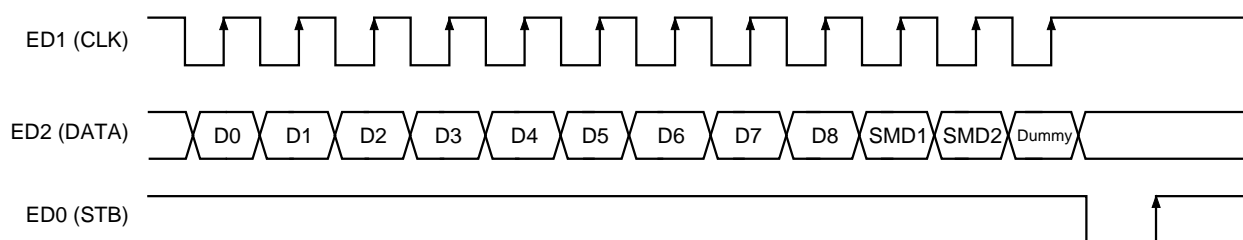
The following four modes can be selected according to the combination of serial data SMD1 and SMD2. (During frame accumulation, low-speed shutter does not operate normally.)

Shutter mode

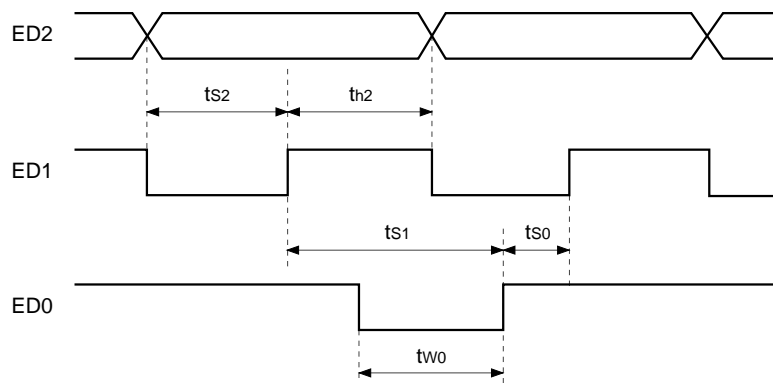
| Mode | Flickerless | High-speed shutter | Low-speed shutter | No shutter |
|------|-------------|--------------------|-------------------|------------|
| SMD1 | L | L | H | H |
| SMD2 | L | H | L | H |

- Flickerless: Eliminates flicker resulting from the frequency of fluorescent light
- High-speed shutter: Higher speed shutter than 1/60 (EIA), 1/50 (CCIR)
- Low-speed shutter: Lower speed shutter than 1/60 (EIA), 1/50 (CCIR)
(Does not operate normally during frame accumulation.)
- No shutter: No shutter operation

<Input timing when using serial input>



The data on ED2 is latched in the register at the rising edge of ED1 and is then taken in internally while ED0 is low.



| Symbol | | Min. | Max. |
|--------|--|------|------|
| ts2 | ED2 setup time against the rising edge of ED1 | 20ns | — |
| th2 | ED2 hold time against the rising edge of ED1 | 20ns | — |
| ts1 | ED1 rising setup time against the rising edge of ED0 | 20ns | — |
| tw0 | ED0 pulse width | 20ns | 50μs |
| ts0 | ED0 rising setup time against the rising edge of ED1 | 20ns | — |

<Shutter speed calculation> (During frame accumulation, low-speed shutter does not operate normally.)

High-speed shutter

- For EIA

$$T = [262_{10} - (1FF_{16} - L_{16})] \times 63.56 + 34.78\mu s \quad * L_{16}: \text{load value}$$

- For CCIR

$$T = [312_{10} - (1FF_{16} - L_{16})] \times 64 + 35.6\mu s$$

| EIA | | | CCIR | | |
|-------------------|---------------|------------------|-------------------|---------------|------------------|
| Load value | Shutter speed | Calculated value | Load value | Shutter speed | Calculated value |
| 0FA ₁₆ | 1/10000 | 1/10169 | 0C8 ₁₆ | 1/1000 | 1/10040 |
| 0FC ₁₆ | 1/4000 | 1/4435 | 0CA ₁₆ | 1/4000 | 1/4394 |
| 100 ₁₆ | 1/2000 | 1/2085 | 0CE ₁₆ | 1/2000 | 1/2068 |
| 108 ₁₆ | 1/1000 | 1/1012 | 0D6 ₁₆ | 1/1000 | 1/1004 |
| 118 ₁₆ | 1/500 | 1/499 | 0E6 ₁₆ | 1/500 | 1/495 |
| 137 ₁₆ | 1/250 | 1/252 | 105 ₁₆ | 1/250 | 1/250 |
| 176 ₁₆ | 1/125 | 1/125 | 143 ₁₆ | 1/125 | 1/125 |
| 196 ₁₆ | 1/100 | 1/100 | 149 ₁₆ | 1/100 | 1/120 |

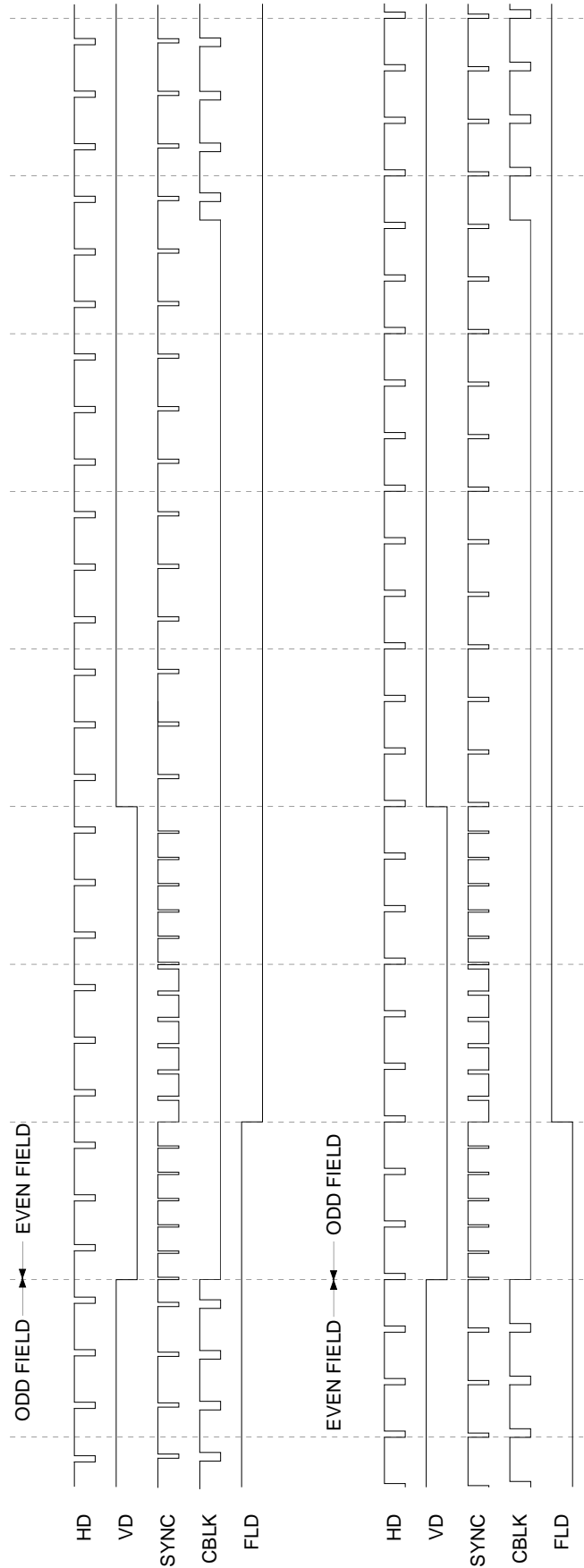
Low-speed shutter (Does not operate normally during frame accumulation.)

$$N = 2 \times (1FF_{16} - L_{16}) \quad \text{FLD}$$

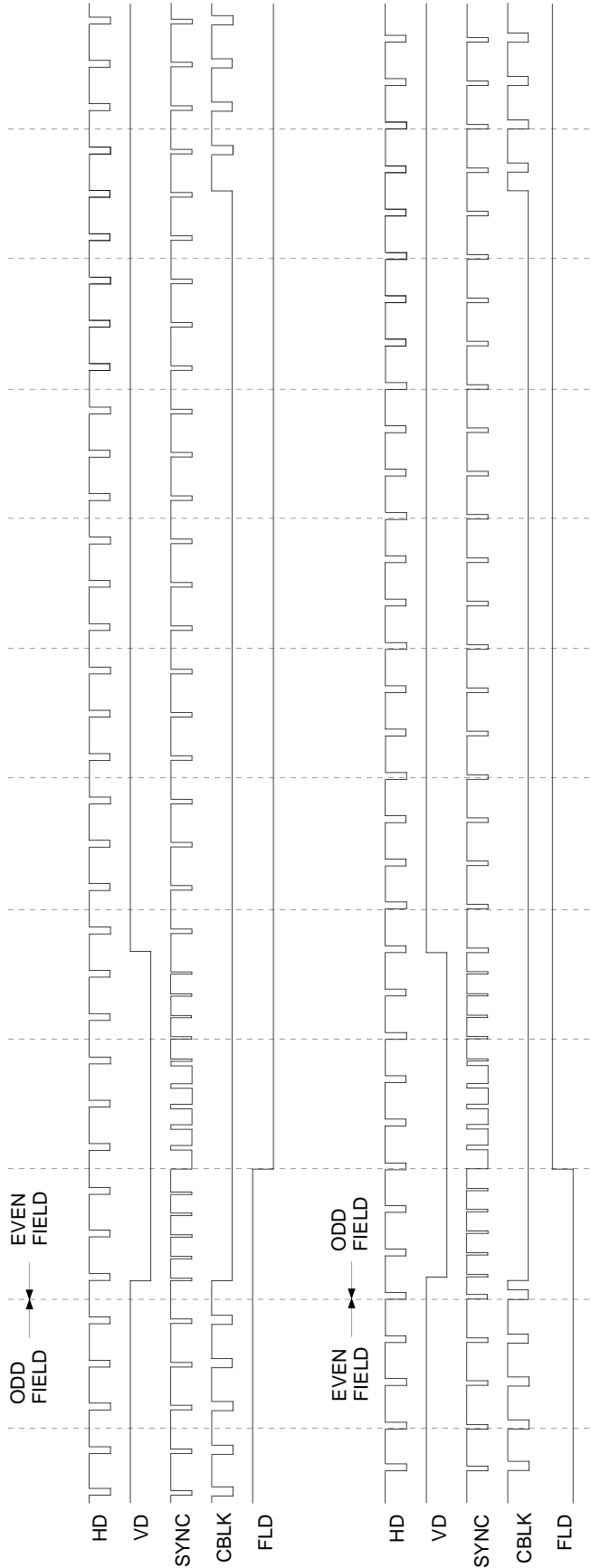
However, 1FF cannot be used as the load value.

| Load value | Shutter speed (FLD) |
|-------------------|---------------------|
| 1FE ₁₆ | 2 |
| 1FD ₁₆ | 4 |
| : | : |
| 101 ₁₆ | 508 |
| 100 ₁₆ | 510 |

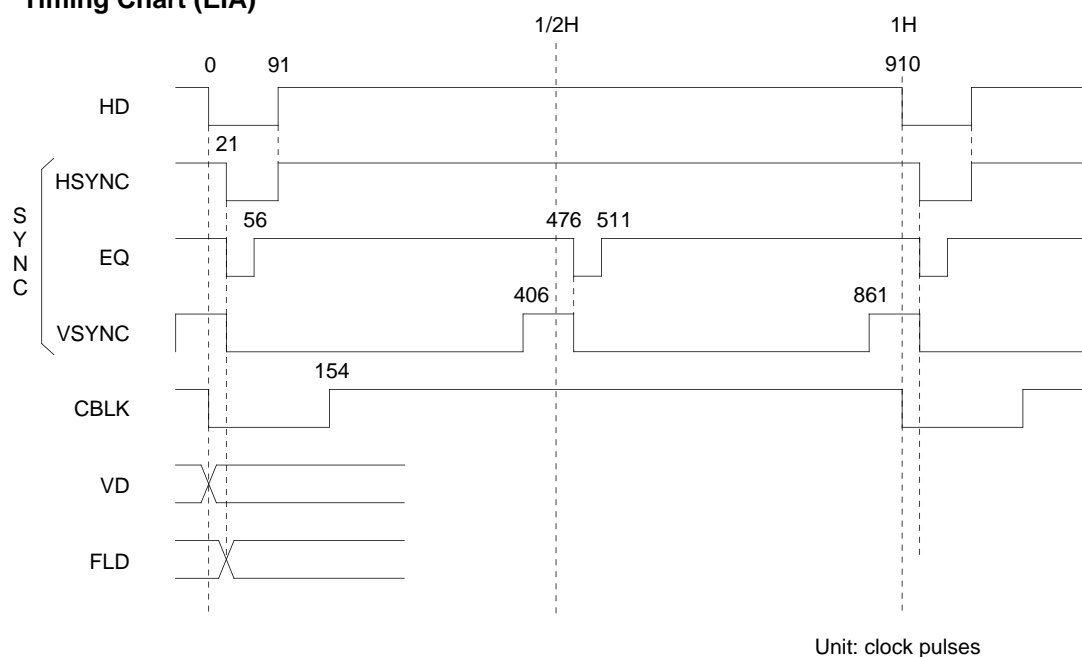
Timing Chart (EIA)



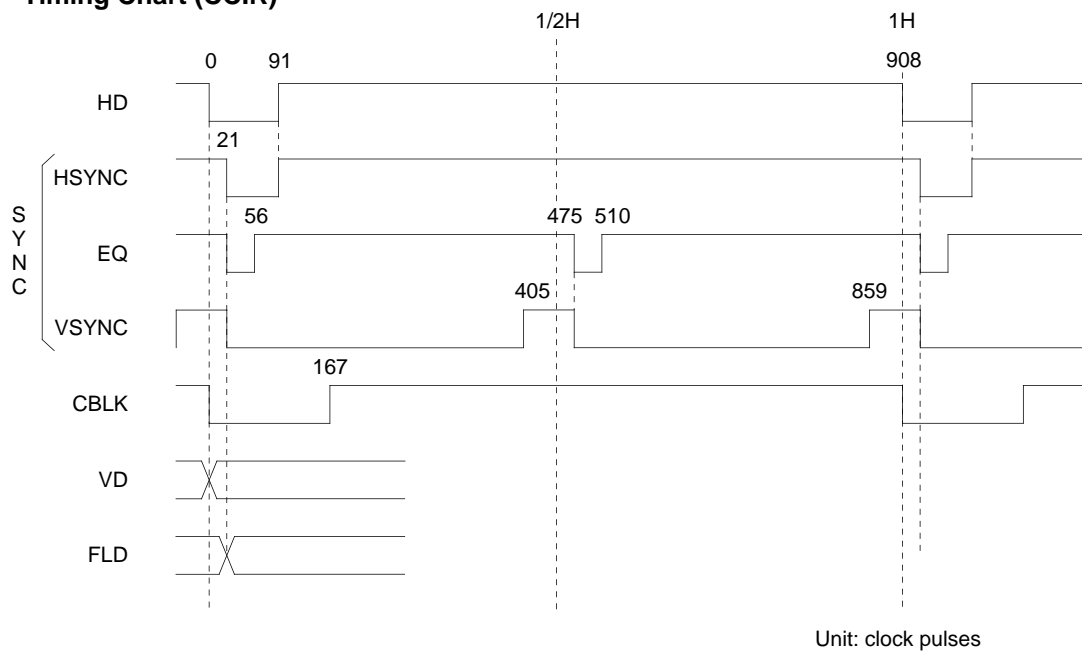
Timing Chart (CCIR)



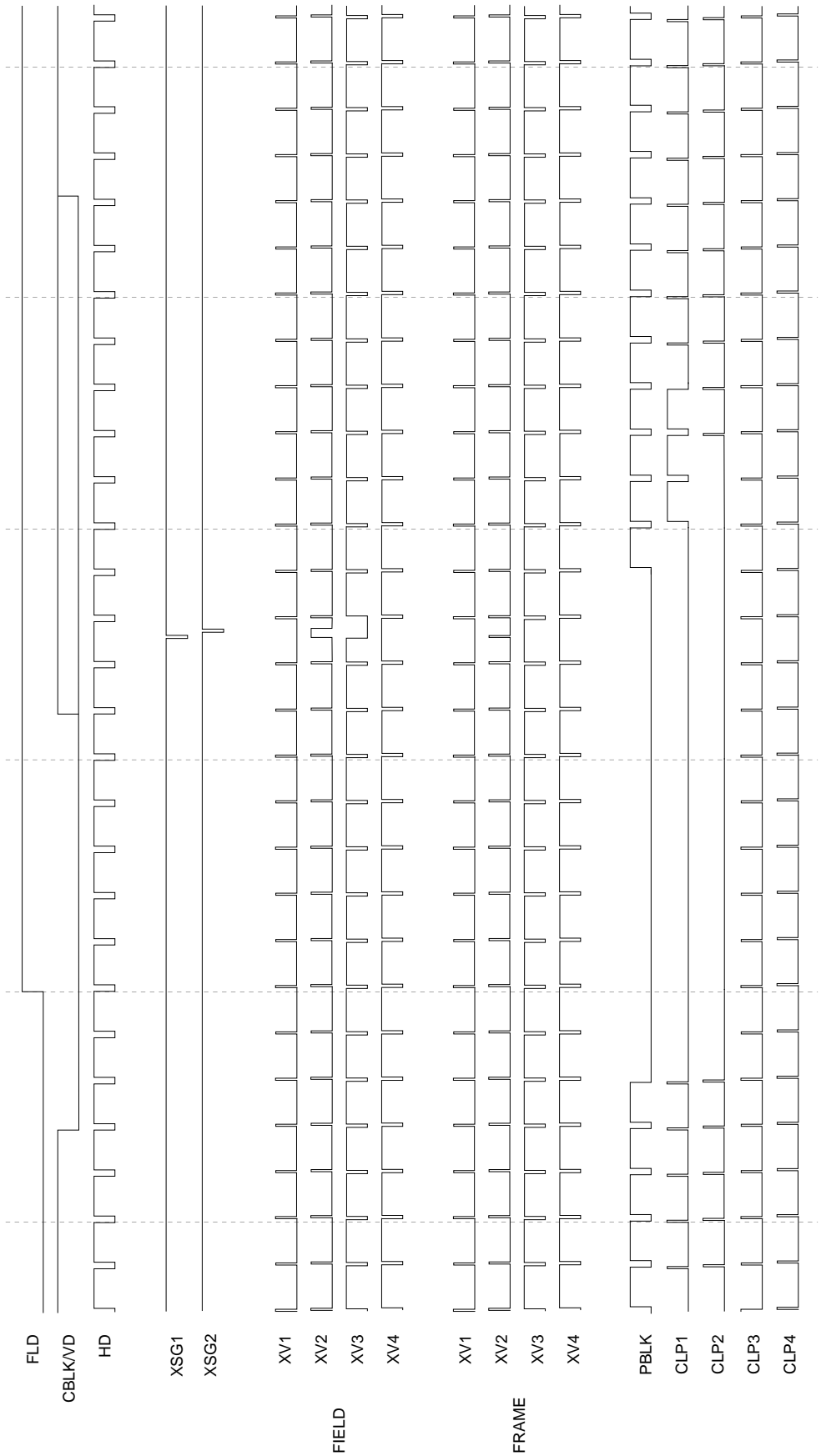
Timing Chart (EIA)



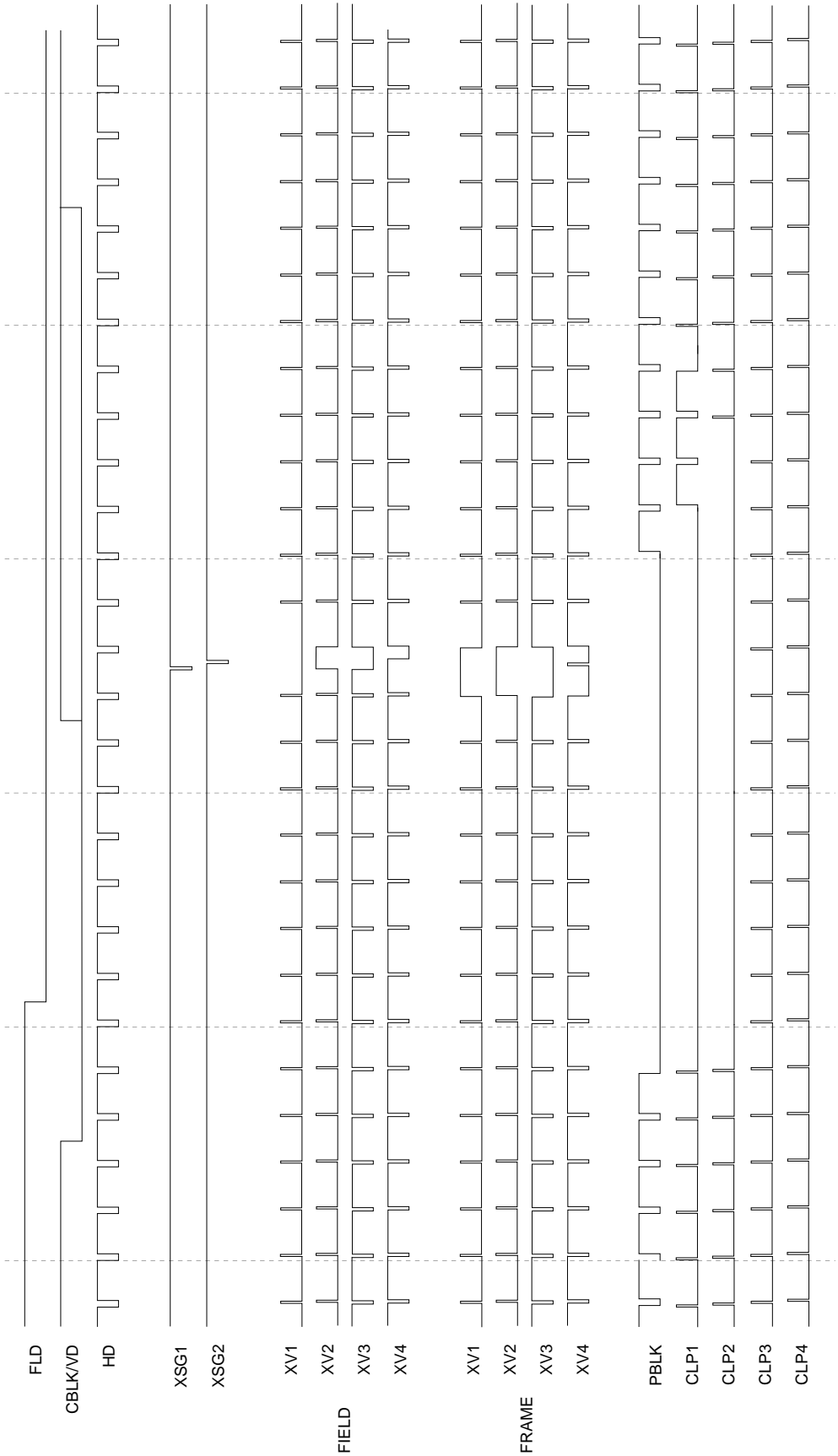
Timing Chart (CCIR)



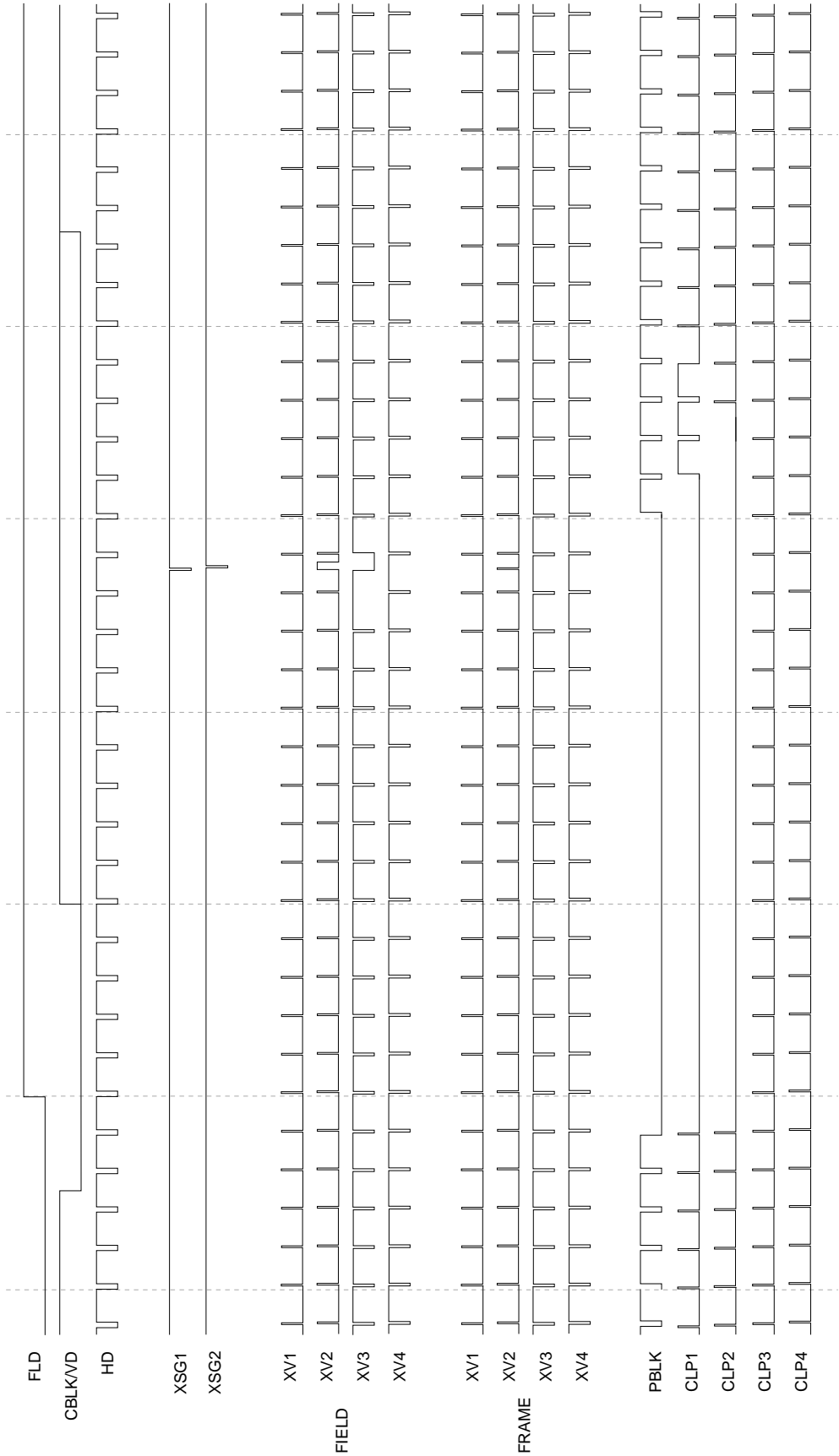
Timing Chart (EIA vertical direction)
ODD Field



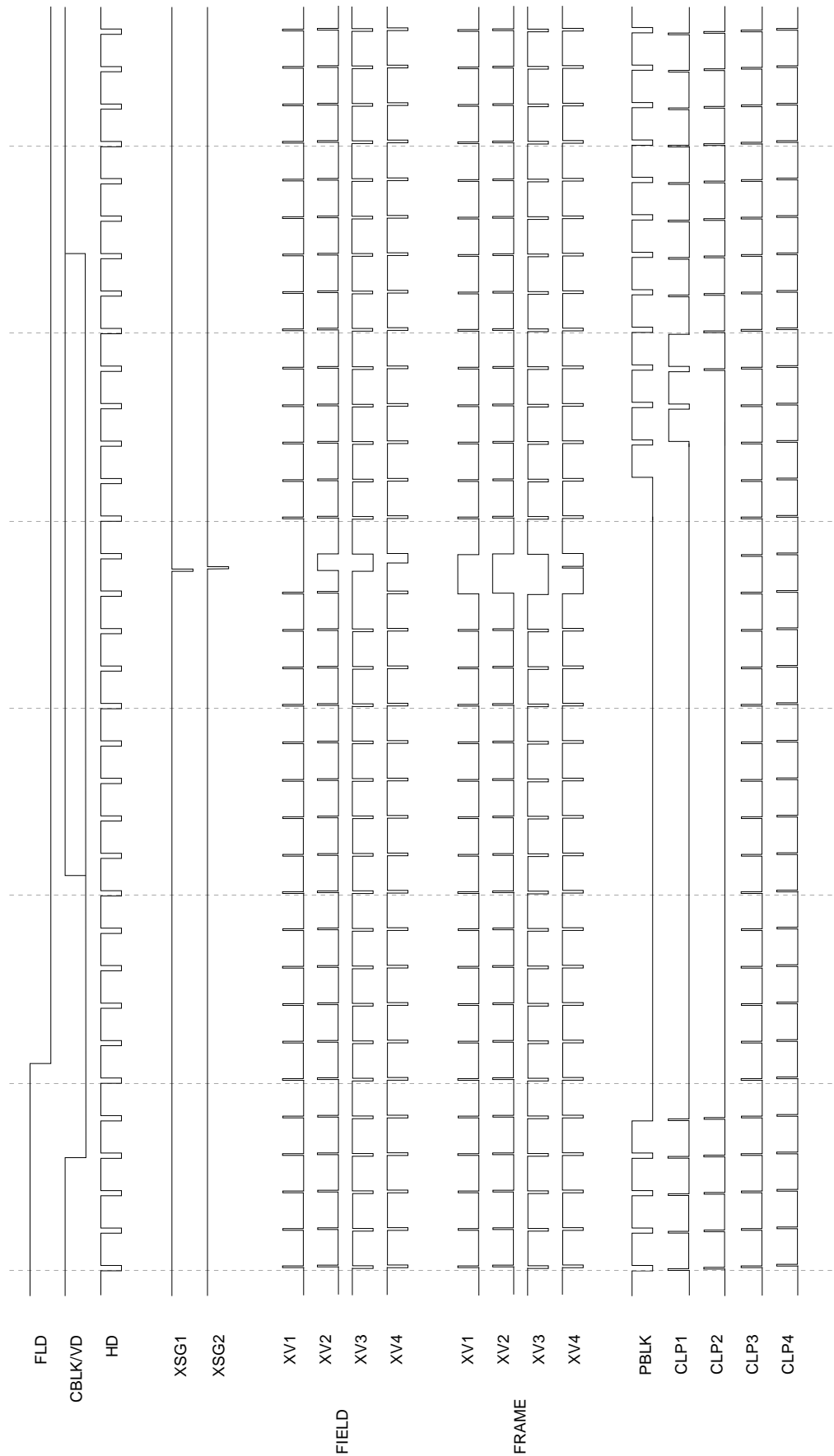
Timing Chart (EIA vertical direction)
EVEN Field



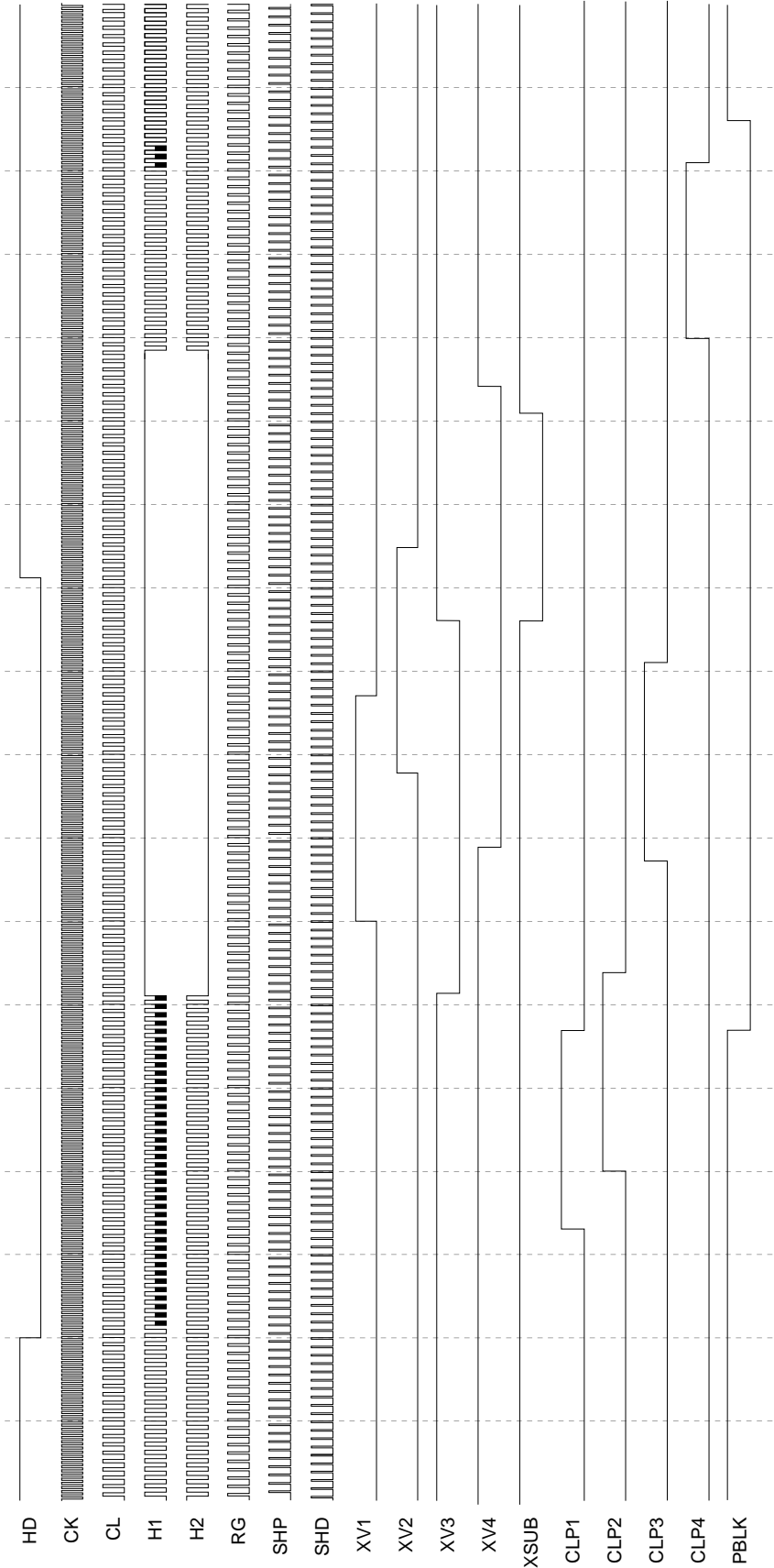
Timing Chart (CCIR vertical direction)
ODD Field



Timing Chart (CCIR vertical direction)
EVEN Field

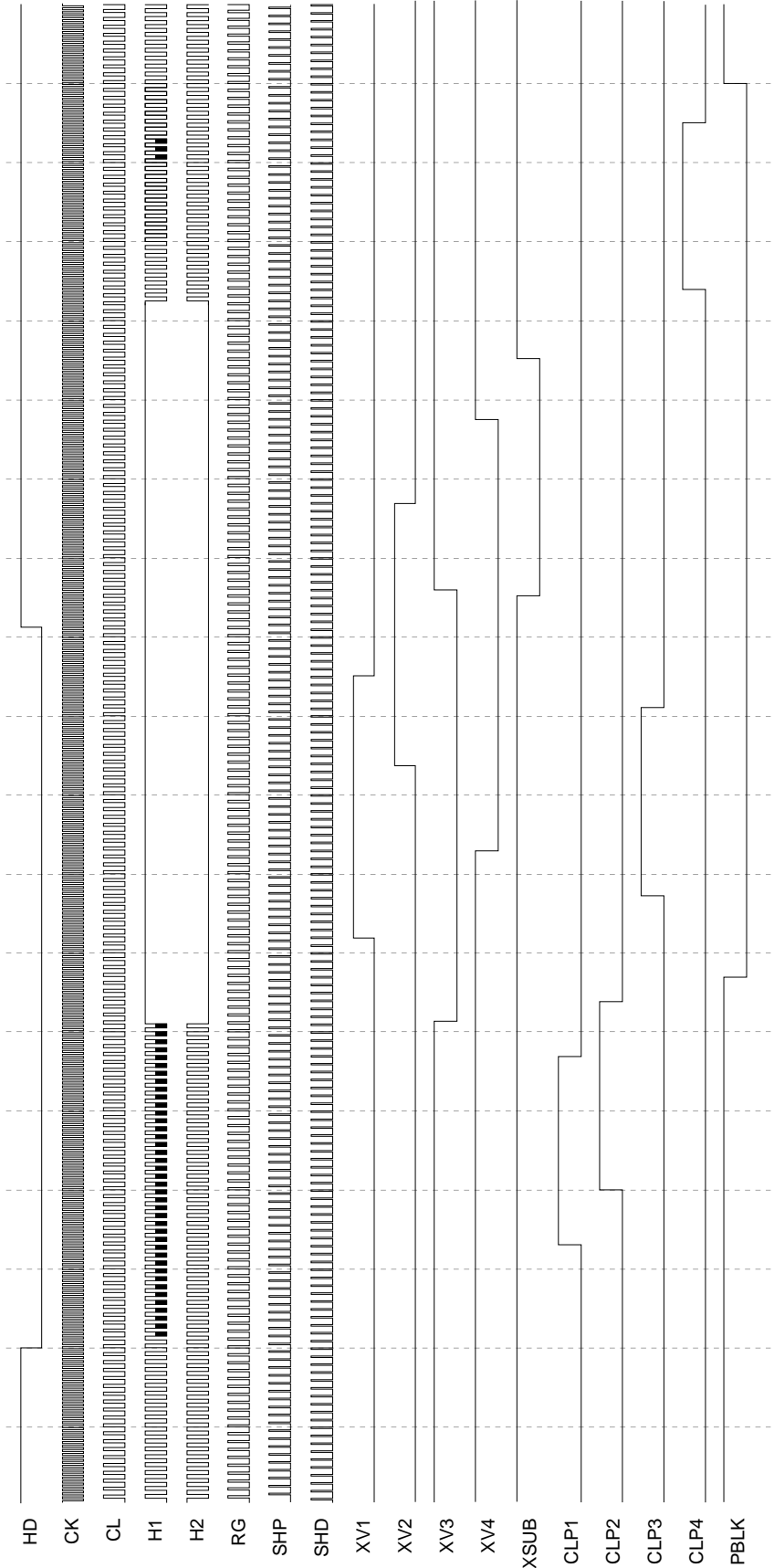


Timing Chart (EIA horizontal direction)



The black-pointed sections of the H1 clock indicate the optical black.

Timing Chart (CCIR horizontal direction)



The black-pointed sections of the H1 clock indicate the optical black.

The diagram illustrates the timing of the 1080p60i signal, divided into two main sections: FIELD READOUT and FRAME READOUT. The signals shown are HD, ODD, EVEN, and XSG (XSG1, XSG2).

FIELD READOUT:

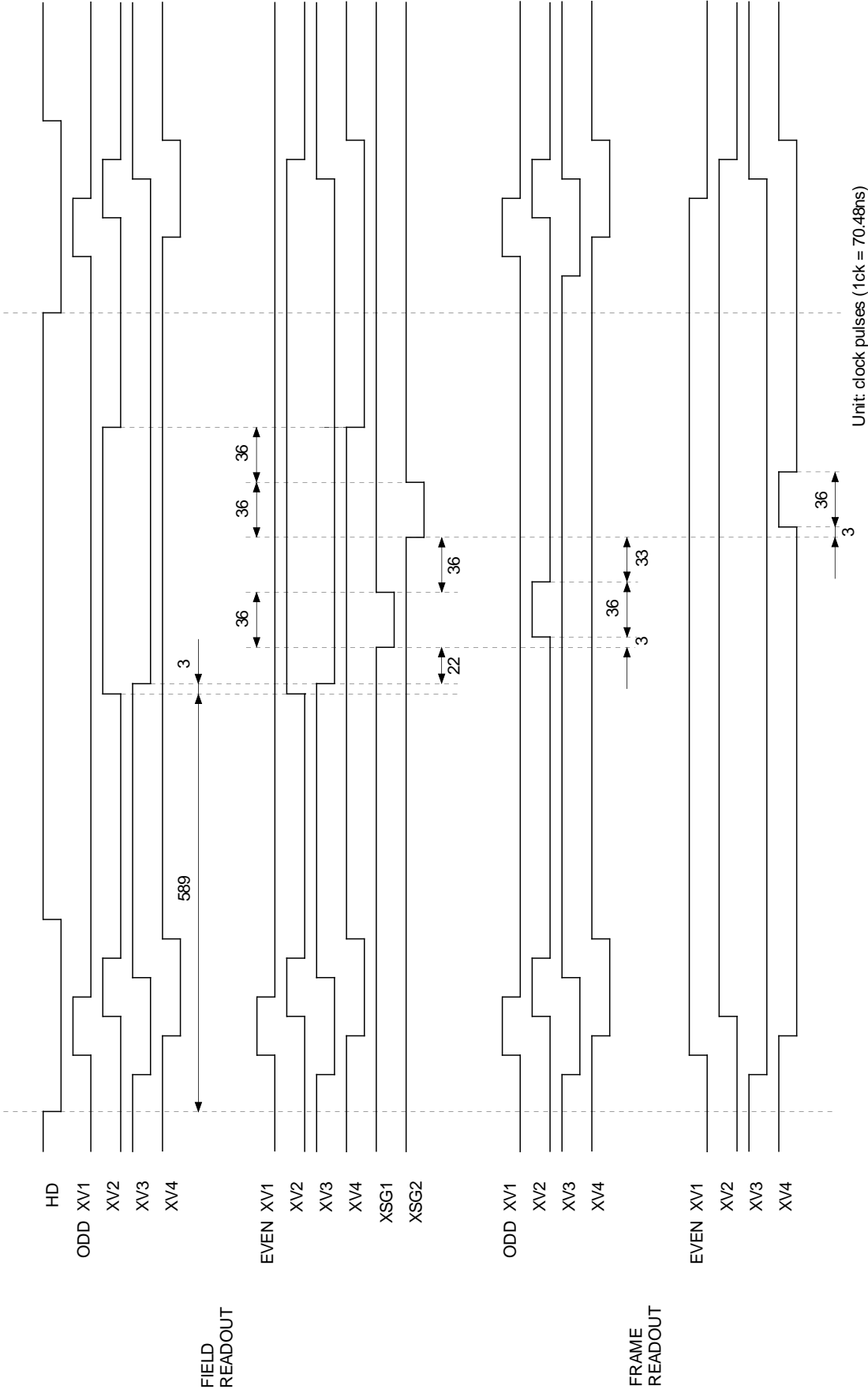
- HD:** Horizontal sync signal. The duration of the active period is 578 clock pulses.
- ODD:** Odd field sync signal. The duration of the active period is 3 clock pulses.
- EVEN:** Even field sync signal. The duration of the active period is 3 clock pulses.
- XSG1 and XSG2:** X-ray sync signals. The duration of the active period is 36 clock pulses.

FRAME READOUT:

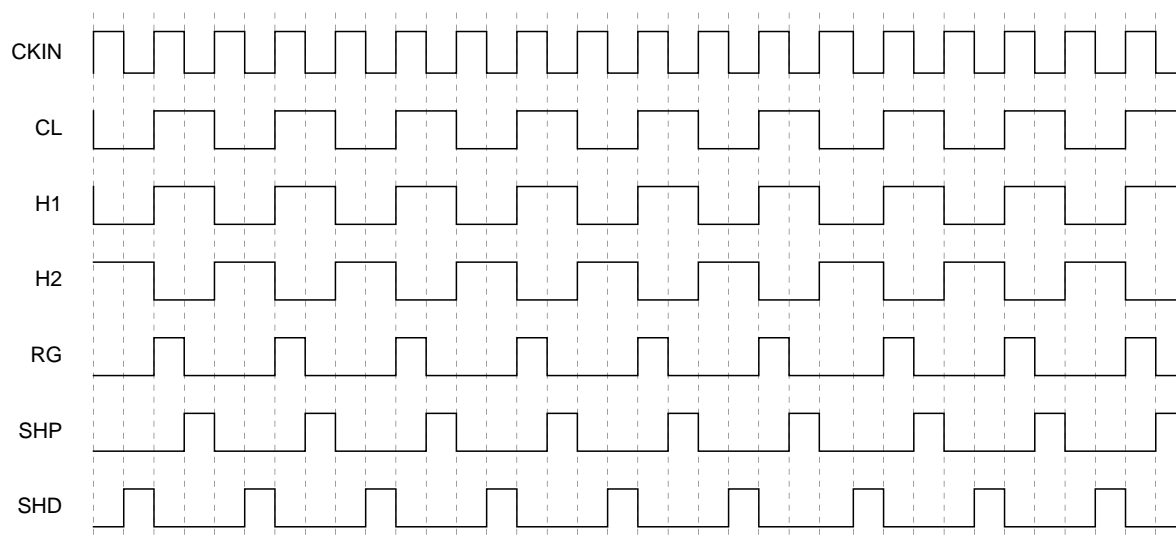
- ODD:** Odd frame sync signal. The duration of the active period is 36 clock pulses.
- EVEN:** Even frame sync signal. The duration of the active period is 36 clock pulses.
- XSG1 and XSG2:** X-ray sync signals. The duration of the active period is 36 clock pulses.

Unit: clock pulses (1clk = 69.84ns)

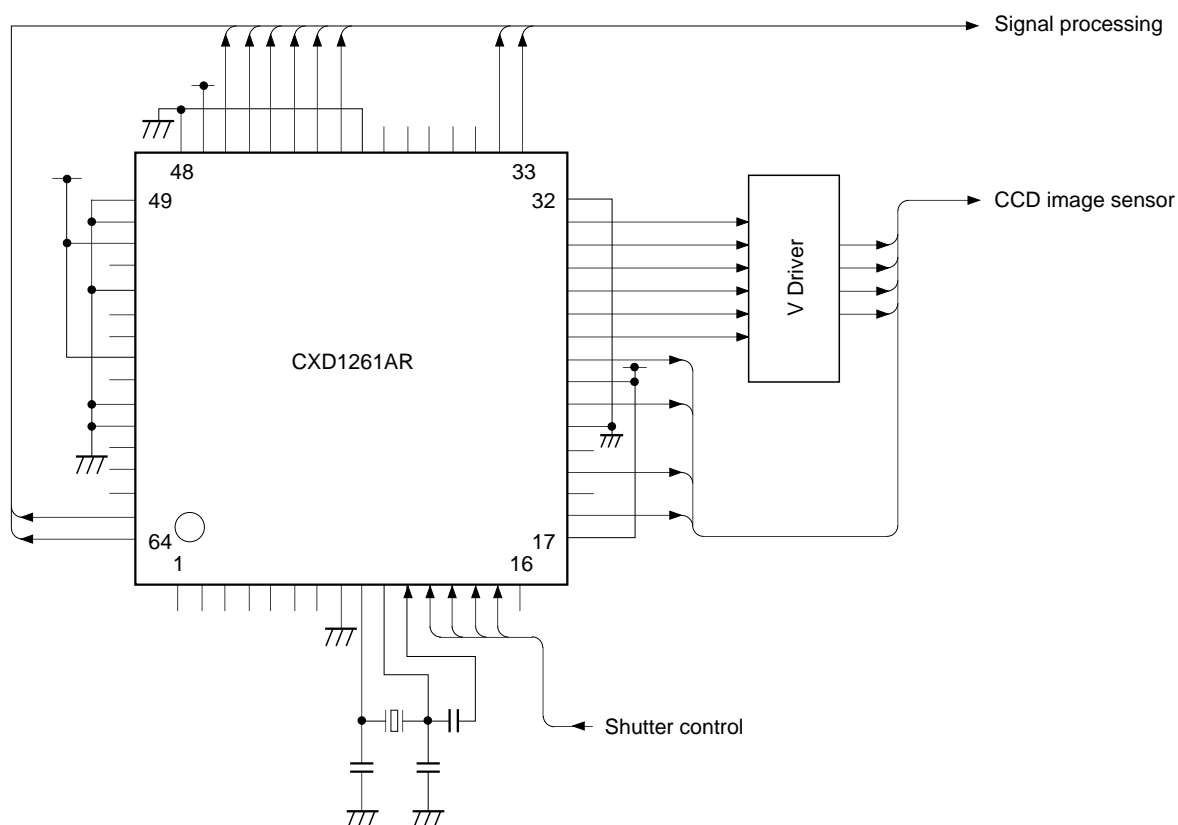
Readout Timing Chart (CCIR)



Timing Chart (High-speed phase)



Application Circuit



OSC EIA : 28.6363MHz

CCIR : 28.375MHz

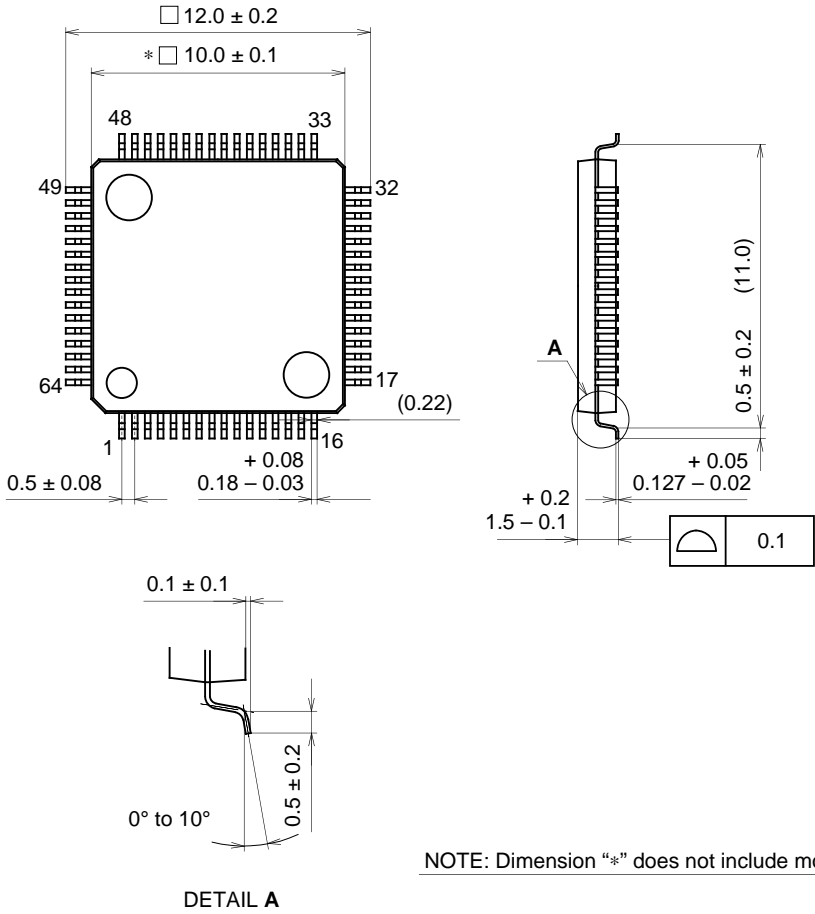
* Use a crystal that operates with a fundamental wave.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

Unit: mm

64PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

| | |
|------------|----------------|
| SONY CODE | LQFP-64P-L01 |
| EIAJ CODE | LQFP064-P-1010 |
| JEDEC CODE | |

| | |
|------------------|--------------------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER/PALLADIUM PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 0.3g |