SONY

CXA1977R

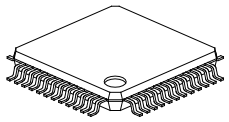
10-bit 20MSPS A/D Converter

Description

The CXA1977R is a 10-bit 20MSPS 2-step parallel type A/D converter for video signal processing.

This A/D converter operates on +5V power supplies. The analog signal can be converted to the digital signal by using this IC in conjunction with the Sample-and-hold IC.

48 pin LQFP (Plastic)



Features

- Maximum operating speed : 20MSPS (Min.)
- Resolution : 10-bit
- Low power dissipation : 160mW (Typ.)
- Wide-band analog input : 10MHz
- Low input capacitance : 50pF (Typ.)
- Built-in digital correction
  (Compensation within ±16LSB)
- TTL input
- TTL output
- Output code : binary/2'S complement/1'S complement

Function

10-bit 20MSPS 2-step parallel type A/D converter

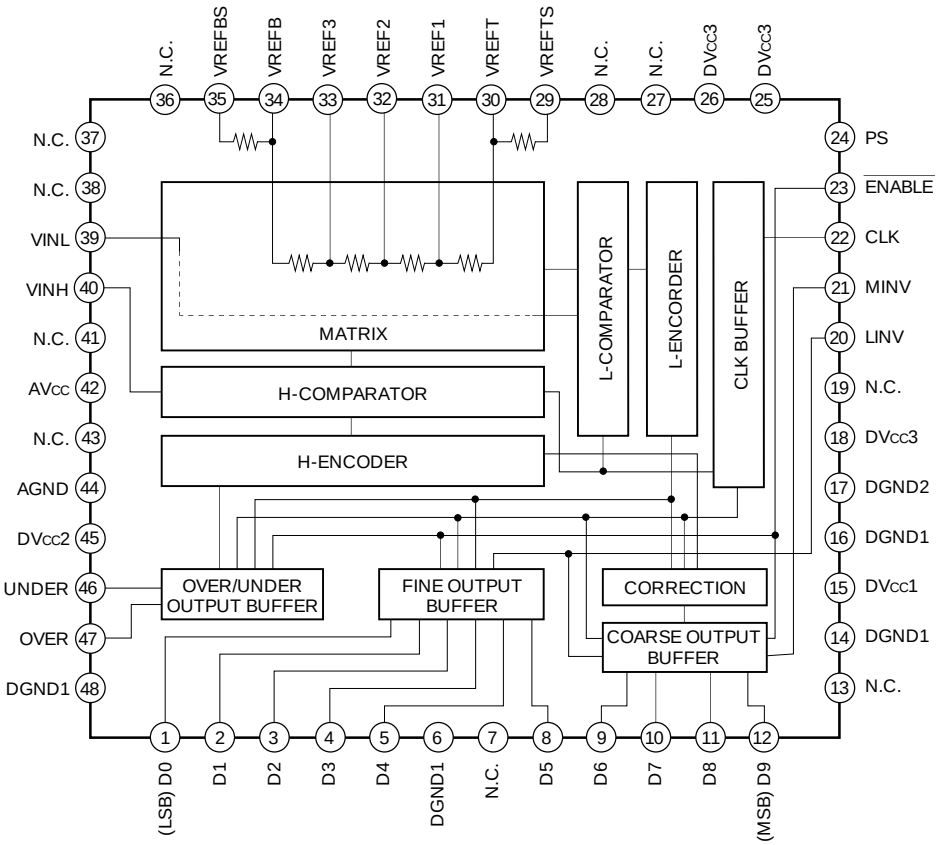
Structure

Bipolar silicon monolithic IC

Applications

High resolution video signal processing

Block Diagram



E94326-PS

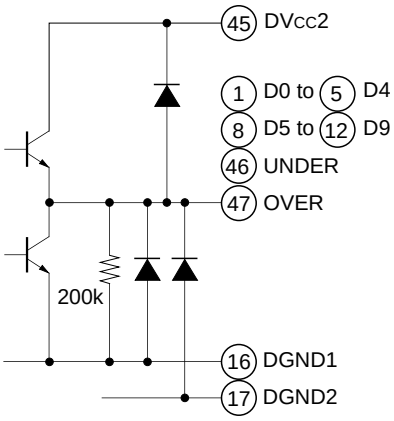
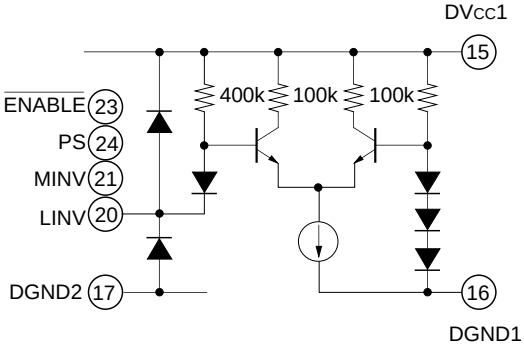
Absolute Maximum Ratings (Ta = 25°C)

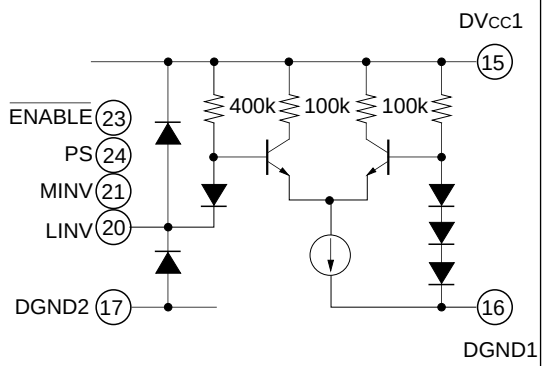
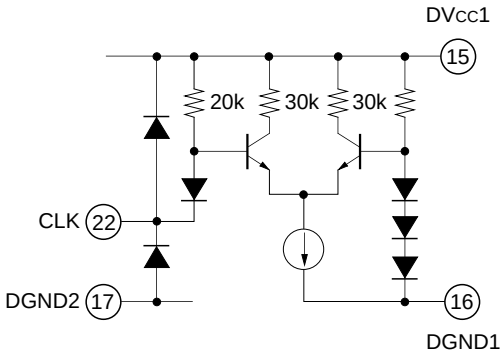
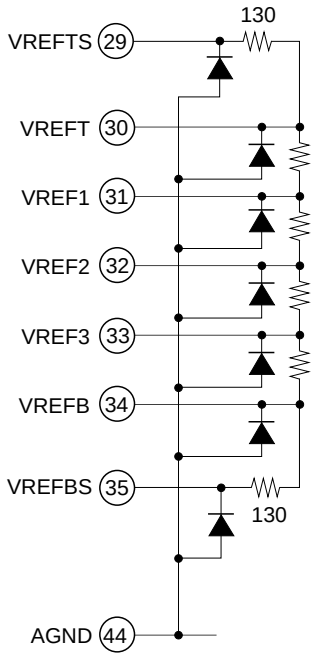
• Supply voltage	DVcc1	0 to +6	V
	DVcc2	0 to +6	V
	DVcc3	0 to +6	V
	AVcc	0 to +6	V
• Analog input voltage	VINH	AGND to AVcc + 0.3	V
	VINL	AGND to AVcc + 0.3	V
• Reference voltage	VREFT	AGND to AVcc + 0.3	V
	VREFB	AGND to AVcc + 0.3	V
• Digital input voltage	CLK	DGND1 – 0.5 to DVcc1	V
	MINV	DGND1 – 0.5 to DVcc1	V
	LINV	DGND1 – 0.5 to DVcc1	V
	PS	DGND1 – 0.5 to DVcc1	V
	$\overline{\text{ENABLE}}$	DGND1 – 0.5 to DVcc1	V
• Digital output voltage	Vo	DGND1 – 0.5 to +3.6	V
	(Vo: The voltage is applied to the output pin for high impedance output.)		
• Storage temperature	Tstg	–65 to 150	°C
• Allowable power dissipation	P_D	950	mW
	(On a fiber-glass epoxy board: 40mm × 40mm, t = 0.8mm)		

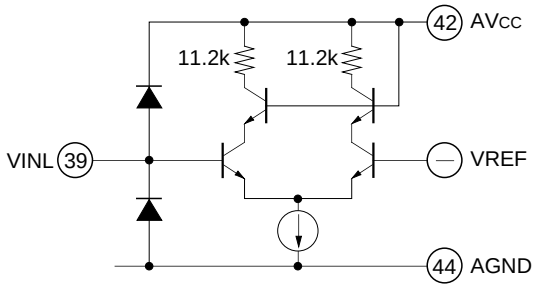
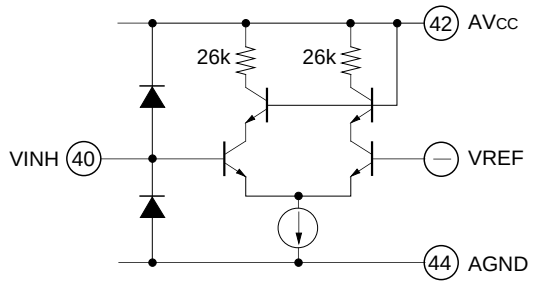
Recommended Operating Conditions

		Min.	Typ.	Max.	Unit
• Supply voltage	DVcc1	+4.6	+5	+5.25	V
	DVcc2	+4.6	+5	+5.25	V
	DVcc3	+4.6	+5	+5.25	V
	AVcc	+4.6	+5	+5.25	V
	AGND		0		V
	DGND1		0		V
	DGND2		0		V
• Analog input voltage	VINH	+2		+4	V
	VINL	+2		+4	V
• Reference voltage	VREFT	+3.9	+4	+4.1	V
	VREFB	+1.9	+2	+2.1	V
• Digital input voltage	V_{IH}	+2			V
	V_{IL}			+0.8	V
• Clock width	t_{PWH}	25			ns
	t_{PWL}	24			ns
• Operating temperature	Topr	–20		+85	°C

Pin Description

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
1 to 5 8 to 12	D0 to D9	O	TTL		Digital output D0 (LSB) to D9 (MSB)
46	UNDER	O			Underflow output
47	OVER	O			Overflow output
15	DVcc1	—	+5V (typ.)		Digital power supply
45	DVcc2				
6, 14, 16, 48	DGND1	—	GND		Digital ground
18	DVcc3	—	+5V (typ.)		Digital power supply
25					
26					
17	DGND2	—	GND		Digital negative power supply
44	AGND	—			Analog negative power supply
20	LINV	I	TTL		This input can invert output form of D0 to D8. In open condition, this pin turns to high level input. (For details, refer to the Output Formula Chart.)
21	MINV	I			This input can invert output form of D9 (MSB). In open condition, this pin turns to high level input. (For details, refer to the Output Formula Chart.)
23	$\overline{\text{ENABLE}}$	I			3-state control. Turns to enable when low is input. In open condition, this pin turns to high level input.

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
24	PS	I	TTL		Power save input. Power save condition is entered when high level is input. In open condition, this pin turns to high level input.
22	CLK	I	TTL		Clock input
29	VREFTS	—	+4V		Reference voltage sense (Top)
30	VREFT	I			Reference voltage force (Top)
31	VREF1	—	+3.5V		
32	VREF2	—	+3.0V		
33	VREF3	—	+2.5V		
34	VREFB	I	+2V		Reference voltage force (Bottom)
35	VREFBS	—			Reference voltage sense (Bottom)

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
39	VINL	I	+2V to +4V		Analog input (Lower comparator input)
40	VINH	I	+2V to +4V		Analog input (Upper comparator input)
42	AVCC	—	+5V (Typ.)		Analog power supply
7, 13, 19, 27	N.C.	—	—		Open. Not connected to internal circuit, but connection to DGND (digital ground) is recommended.
28, 36, 37, 38, 41, 43	N.C.	—	—		Open. Not connected to internal circuit, but connection to AGND (analog ground) is recommended.

Electrical Characteristics

(Ta = 25°C, $DV_{CC}1, 2, 3$, AV_{CC} = +5V, AGND, DGND1, 2 = 0V, V_{REFB} = +2V, V_{REFT} = +4V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n		10	10	10	bit
DC characteristics						
Integral linearity error	E_{IL}	V_{IN} = +2 to +4V	–2.0		+2.0	LSB
Differential linearity error	E_{DL1}	V_{IN} = +2 to +2.5V	–0.8		+0.8	LSB
	E_{DL2}	V_{IN} = +2.5 to +4V	–1		+2 *1	LSB
Analog input						
Analog input current	I_{IN}	V_{IN} = +4V	0		60	µA
Analog input capacitance	C_{IN}	V_{IN} = +3V + 0.07Vrms		50		pF
Analog input band width	BW	–1dB		10		MHz
Reference voltage input						
Reference current	I_{REF}		–16	–10	–7	mA
Reference resistance	R_{REF}		120	200	280	Ω
Offset voltage	E_{OT}		1	10	25	mV
	E_{OB}		1	10	25	mV
Reference voltage	V_{REF1}			3.5		V
	V_{REF2}			3.0		V
	V_{REF3}			2.5		V
Digital input						
Digital input voltage	V_{IH}		2			V
	V_{IL}				0.8	V
Digital input current	I_{IH1}	*2, $DV_{CC}1$ = 5.25V, V_{IH} = 2.7V	–10		+10	µA
	I_{IL1}	*2, $DV_{CC}1$ = 5.25V, V_{IL} = 0.5V	–200		0	µA
	I_{IH2}	*3, $DV_{CC}1$ = 5.25V, V_{IH} = 2.7V	–10		+10	µA
	I_{IL2}	*3, $DV_{CC}1$ = 5.25V, V_{IL} = 0.5V	–20		0	µA
Digital input characteristics				2		pF
Switching characteristics						
Maximum operating speed	Fc		20			MSPS
Clock pulse width	t_{PWH}		25			ns
	t_{PWL}	*4	24			ns
Sampling delay	t_{SH}		–2	1	5	ns
	t_{SL}		–15	–1	2	ns
Output delay time	t_{DLH}	*4, CL = 20pF	10		30	ns
	t_{DHL}	*6, CL = 20pF	10		30	ns
3-state output disable time	t_{PHZ}				250	ns
	t_{PLZ}	*5			400	ns
3-state output enable time	t_{PZH}	*7			500	ns
	t_{PZL}				500	ns

Item	Symbol	Measurement conditions		Min.	Typ.	Max.	Unit
Digital output							
Digital output voltage	V_{OH}	I_{OH} = –300µA	$DV_{CC}1, 2$ = 4.6V	2.7	3.4		V
	V_{OL}	I_{OL} = +500µA				0.5	V
Leak current during output off	I_{OZ}	$DV_{CC}1, 2$ = 5.25V, V_O = 3.6V		–20		75	µA
Dynamic characteristics							
Differential gain error	DG	NTSC 40IRE mod. ramp, Fc = 14.3MSPS			0.5		%
Differential phase error	DP				0.3		deg
SNR	SNR	Fc = 20MSPS FIN = 1kHz			55		dB
		Fc = 20MSPS FIN = 1MHz			53		dB
		Fc = 20MSPS FIN = 2MHz			52		dB
		Fc = 20MSPS FIN = 7.5MHz			49		dB
Power supply							
$DV_{CC}1$ current	$I_{DVCC}1$	$DV_{CC}1$ = +5V		6.0	9.9	14.0	mA
		*8 During power save		4.3	7.3	12.0	mA
$DV_{CC}2$ current	$I_{DVCC}2$	$DV_{CC}2$ = +5V		0.05	0.16	0.30	mA
		*8 During power save		0	0	27	mA
$DV_{CC}3$ current	$I_{DVCC}3$	$DV_{CC}3$ = +5V		8.1	14.7	21.1	mA
		*8 During power save		0.34	0.55	1.13	mA
AV_{CC} current	I_{AVCC}	AV_{CC} = +5V		0.5	3.2	6.0	mA
		*8 During power save		0	20	50	µA
Power dissipation Pd = A + B A = ($I_{DVCC}1$ + $I_{DVCC}2$ + $I_{DVCC}3$ + I_{AVCC}) × 5V B = | I_{REF} | × 2V	Pd			87	160	239	mW
		*8 During power save		37	59	98	mW

*1 +1 < $E_{DL}2$ ≤ +2 (LSB) is two and under.

*2 CLK input

*3 MINV, LINV, $\overline{\text{ENABLE}}$, and PS inputs

*4 Refer to Timing Diagram (1)

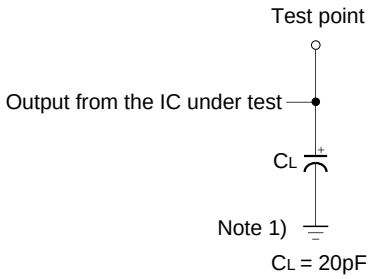
*5 Refer to Timing Diagram (2)

*6 The load is a bi-state totem-pole output delay time test load circuit.

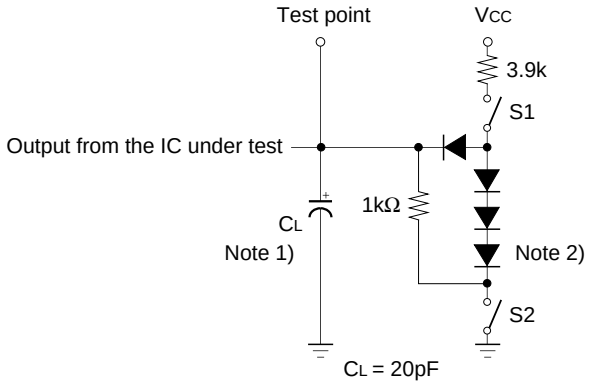
*7 The load is a 3-state output test load circuit.

*8 When PS and $\overline{\text{ENABLE}}$ inputs are in high level.

Bi-state Totem-pole Output Delay Time Test Load Circuit



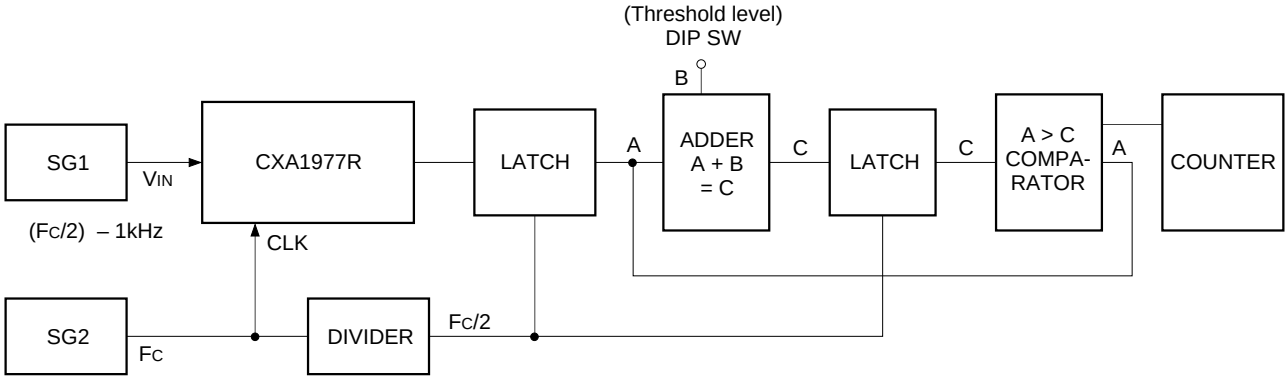
3-state Output Test Load Circuit



Test condition	S1	S2
t_{PZL}	Close	Open
t_{PZH}	Open	Close
t_{PLZ} t_{PHZ}	Close	Close

Note 1) C_L includes probe capacitance and parasitic capacitance in Test Board.
Note 2) All diodes are IS2076.

Error Rate Test Circuit



Notes on Operation

1. Analog ground (AGND)
   Keep analog ground surface on PCB as wide as possible with impedance and resistance as low as possible.

2. Digital ground (DGND1, DGND2)
   Upon mounting to PCB keep ground surface as wide as possible with impedance and resistance as low as possible.
   Moreover, a common analog and digital ground immediately near ADC will help obtain characteristics smoothly.

3. Digital positive power supply (DVcc1, DVcc2, DVcc3)
   Connect to the digital ground with a ceramic capacitor over 0.1µF and as close to the pins as possible.
   Insert a ceramic capacitor between DVcc2 and DGND1 of TTL output power supply as shortly as possible because noise tends to occur.

4. Analog positive power supply (AVcc)
   Connect to the analog ground on PCB with a ceramic capacitor over 0.1µF as close to the pin as possible.

5. Reference voltage (VREFTS, VREFT, VREF1, VREF2, VREF3, VREFB, VREFBS)
   These pins provide reference voltage to upper and lower comparators. Voltage between VREFT and VREFB corresponds to input dynamic range.
   There is a 200Ω resistance between VREFT and VREFB. By applying 2V to both pins a current of about 10mA flows. When the reference voltage is made unstable by the clock, ADC characteristics are adversely affected. Connect VREFT and VREFB to the analog ground on PCB by means of a tantalum capacitor over 10µF and a ceramic capacitor over 0.1µF respectively. Also, connect each of VREF1, VREF2 and VREF3 to the analog ground on PCB using a ceramic capacitor over 0.1µF. This will provide stability to the characteristics of high frequency. Strictly speaking on reference voltage VREFT side and VREFB side there is a respective about 10mV offset.
   When there is no problem with the usage of those offset voltages, voltage is applied directly to VREFT, VREFB. In case the reference voltage is to be strictly applied, adjust to obtain an offset voltage of 0V, keeping VREFTS and VREFBS as sense pins and VREFT and VREFB as force pins to form a feedback loop circuit.
   For details, see the Standard Circuit.

6. Analog input (VINH, VINL)
   VINH is the input pin for the upper comparator while VINL is the input pin for the lower comparator.
   Keep the input signal level within the level between VREFT and VREFB.
   As this IC's analog input capacitance stands at about 50pF, it is necessary to drive with an buffer amplifier having sufficient driving capability. Also, when driving is done with the buffer amplifier of a low output impedance, as A/D converter input capacitance is large, ringing is generated and settling time grows longer. Here a small resistance of about 5 to 30Ω is connected in series between the buffer amplifier and each of A/D converter's VINH and VINL, as a dumping resistance. This eliminates ringing and shortens settling time. Also keep wiring between buffer amplifier and A/D converter as short as possible.

7. Clock input (CLK)

   TTL input. Clock line wiring should be the shortest possible while distanced from other signal lines to avoid affecting them.

   This IC is 2-step parallel type A/D converter. Accordingly an external sample-and-hold circuit (SH) is necessary. However the timing between this SH circuit output waveform (A/D converter analog input waveform) and the A/D converter clock timing requires attention. In the relation between A/D converter clock and the A/D converter analog input signal, with the timing T_H of the rising edge of A/D converter clock, the upper comparator compares the input signal and the reference voltage to latch the results. After that, with the timing T_L of the falling edge of A/D converter clock, the lower comparator compares the input signal and reference signal to latch the results. (Strictly speaking, the sampling delay t_{SH} is in T_H and the sampling delay t_{SL} is in T_L.)

   In this A/D converter, the lower comparator features a length of ±32mV (±16LSB) redundance in relation to the upper comparator. At the timing when the lower comparator compares input signal and reference signal to latch at the timing T_L, it is necessary to have the SH output settling performed. But at the timing when the upper comparator compares input signal and reference voltage to latch at the timing T_H, as long as the SH output is within the ±32mV range to the final settling value, digital correction applies, A/D conversion precisely occurs. As seen from the above, A/D converter clock rise and fall timing versus SH output waveform should be duly considered. For the clock high level time t_{PWH} and low level time t_{PWL}, set to a value in excess of the time indicated for the respective operating conditions.

   Output data is synchronously with the clock rising edge.

   For details on timing, refer to the Timing Chart.

8. MINV input (MINV)

   Digital output polarity inversion control pin of D9 (MSB).

   TTL input. At open, turns to high level input.

   For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

9. LINV input (LINV)

   Digital output polarity inversion control pin of D8 to D0 (LSB).

   TTL input. At open, turns to high level input.

   For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

10. Output enable ($\overline{\text{ENABLE}}$)

    3-state control pin of digital output (D0 to D9, UNDER, OVER)

    TTL input. At open, turns to high level input. At that time digital output turns all to high impedance.

11. Power save input (PS)

    Power save control pin of internal circuit.

    TTL input. At open, turns to high level input.

    To set to power save mode, turn both PS and $\overline{\text{ENABLE}}$ to high level input.

12. Digital output (D0 to D9)

Output pin of D9 (MSB) to D0 (LSB).

TTL output.

Output data polarity inversion is executed by means of MINV and LINV signals, and they can output in binary, 1'S complement and 2'S complement.

Also, by turning $\overline{\text{ENABLE}}$ signal to high level, the output can be turned into high impedance output.

However, when the output level is for high impedance output or is in power save mode, the voltage of 3.6V or more must not be applied to prevent the distruction of IC.

For correspondence with analog input voltage and output data code, refer to the Output Formula Chart. For the timing, refer to the Timing Chart.

13. Overflow output (OVER)

When the input signal exceeds VREFT, overflow signal is output.

MINV and LINV have no effect on this pin.

Also by turning $\overline{\text{ENABLE}}$ signal to high level, the output can be turned into high impedance output.

However, when the output level is for high impedance output or is in power save mode, the voltage of 3.6V or more must not be applied to prevent the distruction of IC.

For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

For the timing, refer to the Timing Chart.

14. Underflow output (UNDER)

When the input signal turns below VREFB, underflow signal is output.

MINV and LINV have no effect on this pin.

Also by turning $\overline{\text{ENABLE}}$ signal to high level, the output can be turned into high impedance output.

However, when the output level is for high impedance output or is in power save mode, the voltage of 3.6V or more must not be applied to prevent the distruction of IC.

For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

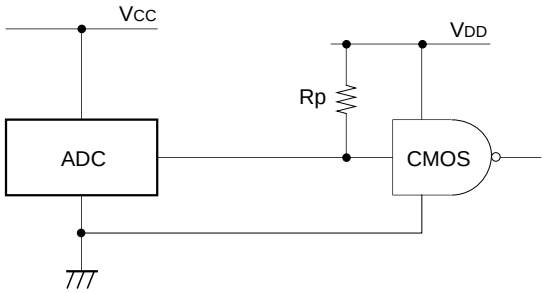
For the timing, refer to the Timing Chart.

15. TTL to CMOS interface

In general, V_{OH} of TTL is approximately 3.7V without load, and it is guaranteed to be 2.7V (Min.). However, it is not enough for V_{OH} of TTL to drive V_{IH} of CMOS,because V_{IH} of CMOS is 3.5V (Min.)

TTL	CMOS
V_{OH} (Min.) = 2.7V	V_{IH} (Min.) = 3.5V (= 0.7V_{DD})
V_{OL} (Max.) = 0.5V	V_{IL} (Max.) = 1.5V (= 0.3V_{DD})

When TTL output of ADC is made a connection with CMOS logic circuit, pull-up resistance (Rp) is used. (See chart below). The value of Rp is usually from a few thousand ohm to scores of thousand ohm. The Rp (min.) is decided by Supply voltage of CMOS (V_{DD}) and I_{OL} of ADC (= +500µA), while the Rp (max.) is decided by required propagation delay (positive edge) and load capacitance. When Vcc is larger than V_{DD}, it is necessary to pay attention to input equivalent circuit of CMOS, because it may happen that V_{IH} goes over the absolute maximum ratings of CMOS and it brings about LATCH-UP to CMOS circuit.



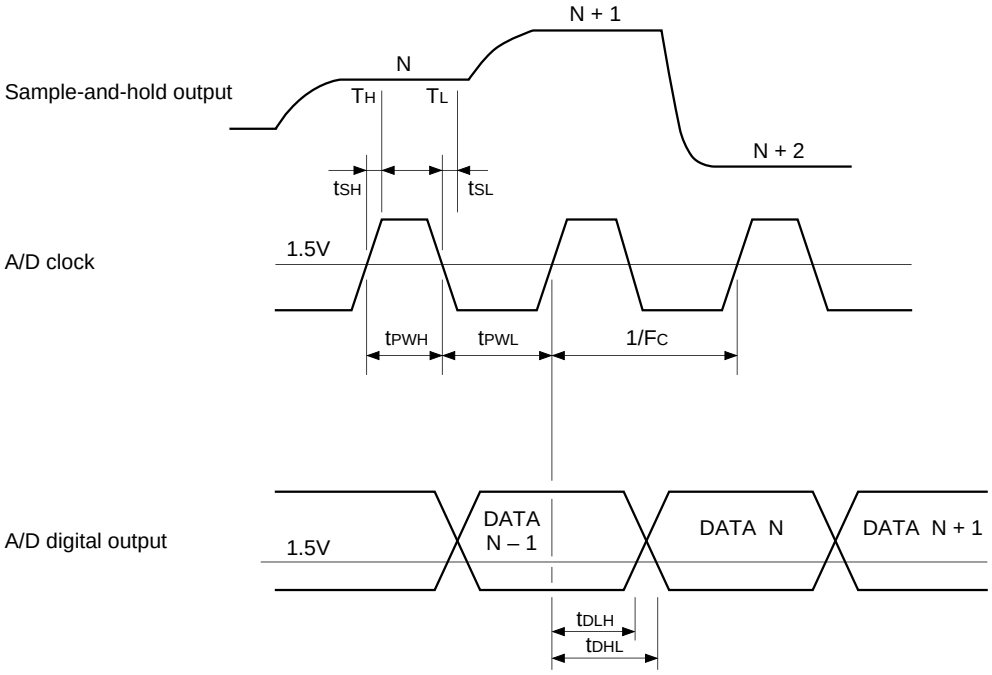
Output Formula Chart

$\overline{\text{ENABLE}}$		0	0	0	0	1 (OPEN)
MINV		1 (OPEN)	1 (OPEN)	0	0	—
LINV		1 (OPEN)	0	1 (OPEN)	0	—
OUTPUT		OF 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	OF 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	OF 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	OF 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	
4V	0	1 0 0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1 1 0	1 1 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 0	Z
:	1	0 0 0 0 0 0 0 0 0 0 1 0	0 0 1 1 1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 1 0	0 1 1 1 1 1 1 1 1 1 0 0	Z
:	2	0 0 0 0 0 0 0 0 0 1 0 0	0 0 1 1 1 1 1 1 1 0 1 0	0 1 0 0 0 0 0 0 0 1 0 0	0 1 1 1 1 1 1 1 1 0 1 0	Z
:	3	0 0 0 0 0 0 0 0 0 1 1 0	0 0 1 1 1 1 1 1 1 0 0 0	0 1 0 0 0 0 0 0 0 1 1 0	0 1 1 1 1 1 1 1 1 0 0 0	Z
:	:	:	:	:	:	:
:	512	0 1 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 0	Z
:	:	:	:	:	:	:
:	1019	0 1 1 1 1 1 1 1 0 1 1 0	0 1 0 0 0 0 0 0 1 0 0 0	0 0 1 1 1 1 1 1 0 1 1 0	0 0 0 0 0 0 0 0 1 0 0 0	Z
:	1020	0 1 1 1 1 1 1 1 1 0 0 0	0 1 0 0 0 0 0 0 0 1 1 0	0 0 1 1 1 1 1 1 1 0 0 0	0 0 0 0 0 0 0 0 0 1 1 0	Z
:	1021	0 1 1 1 1 1 1 1 1 0 1 0	0 1 0 0 0 0 0 0 0 1 0 0	0 0 1 1 1 1 1 1 1 0 1 0	0 0 0 0 0 0 0 0 0 1 0 0	Z
:	1022	0 1 1 1 1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 1 0	0 0 1 1 1 1 1 1 1 1 0 0	0 0 0 0 0 0 0 0 0 0 1 0	Z
2V	1023	0 1 1 1 1 1 1 1 1 1 1 1	0 1 0 0 0 0 0 0 0 0 0 1	0 0 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 1	Z

0: VOLTAGE LEVEL-LOW
1: VOLTAGE LEVEL-HIGH
Z: HIGH IMPEDANCE

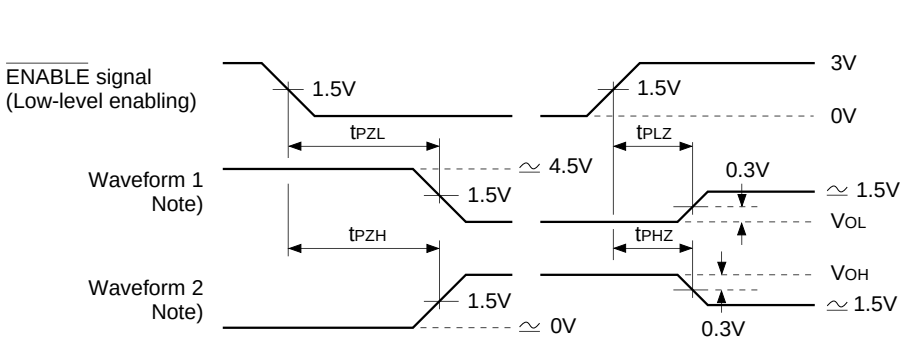
OF: OVER FLOW
UF: UNDER FLOW

Timing Chart (1)



T_H is the timing of latching result for the comparator of V_{IN} and V_{REF} in the upper comparators.
T_L is the timing of latching result for the comparator of V_{IN} and V_{REF} in the lower comparators.

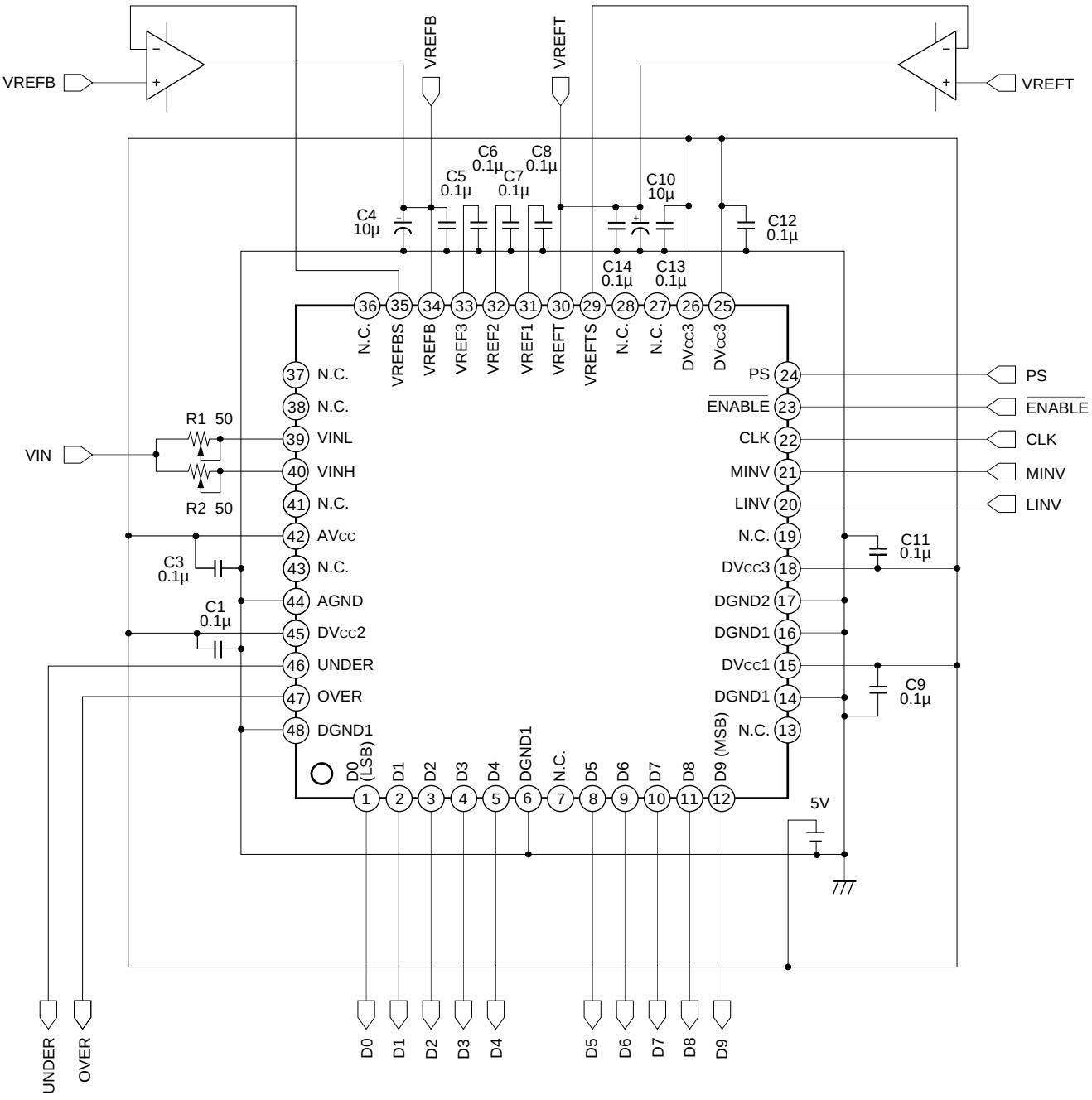
Timing Chart (2)



Output waveform of 3-state enable and disable time*.
(* Enable time = t_{PZL}/t_{PZH}, disable time = t_{PLZ}/t_{PHZ})

Notes) Waveform 1 indicates the output waveform when internal conditions are set to obtain a low level output, with the exception of when output is disabled by means of the $\overline{\text{ENABLE}}$ signal.
Waveform 2 indicates the output waveform when internal conditions are set to obtain a high level output, with the exception of when output is disabled by means of the $\overline{\text{ENABLE}}$ signal.

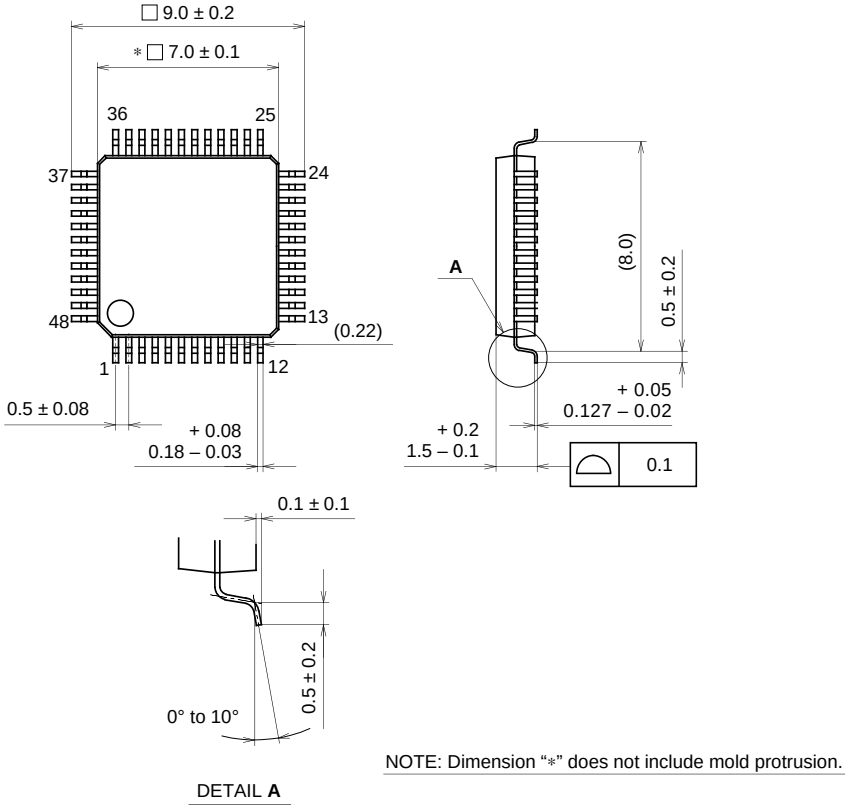
Standard Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g