AUTOMOTIVE GRADE

CS8183

Dual Micropower 200mA Low Dropout Tracking Regulator/Line Driver

Description

The CS8183 is a dual low dropout tracking regulator designed to provide adjustable buffered output voltages that closely track (±10mV) the reference inputs. The outputs deliver up to 200mA while being able to be configured higher, lower or equal to the reference voltages.

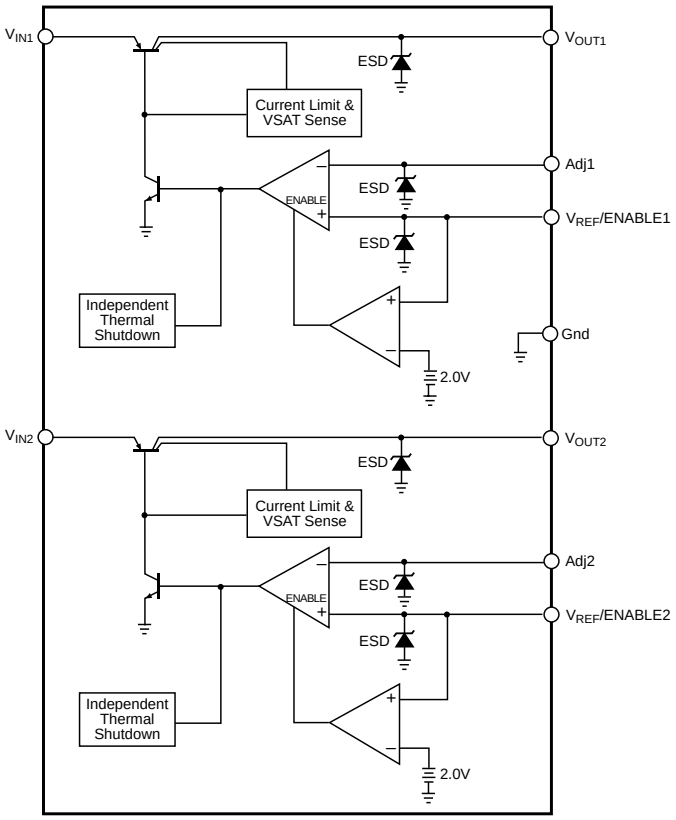
The outputs have been designed to operate over a wide range (2.8V to 40V) while still maintaining excellent DC characteristics. The CS8183 is protected from reverse battery, short circuit and thermal runaway conditions. The device also can withstand 45V load dump transients and -50V reverse polarity input voltage transients. This makes it suitable for use in automotive environments.

The V_{REF} / ENABLE leads serve two purposes. They are used to provide the input voltage as a reference for the output and they also can be pulled low to place the device in sleep mode where it nominally draws less than 30µA from the supply.

Features

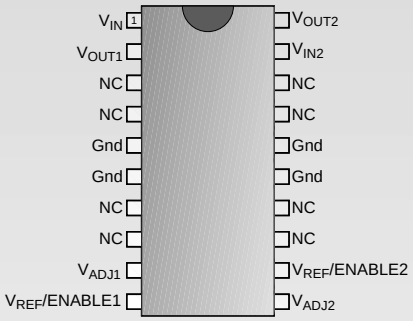
- **Two Regulated Outputs 200mA, ±10mV Track Worst Case**
- **Low Dropout (0.35V typ. @ 200mA)**
- **Low Quiescent Current**
- **Independent Thermal Shutdown**
- **Short Circuit Protection**
- **Wide Operating Range**

Block Diagram



Package Options

20 Lead SO Wide
(internally fused leads)



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Absolute Maximum Ratings

Storage Temperature ..... –65°C to 150°C
Supply Voltage Range (continuous) ..... –15V to 40V
Supply Voltage Range (normal, continuous) ..... 3.4V to 40V
Peak Transient Voltage (V_{IN} = 14V, Load Dump Transient = 31V) 45V
Voltage Range (Adj, V_{REF} / ENABLE, V_{OUT}) ..... –10V to 45V
Maximum Junction Temperature ..... 150°C
ESD Capability (Human Body Model) 2kV
Lead Temperature Soldering
Wave Solder(through hole styles only) ..... 10 sec. max, 260°C peak
Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: V_{IN} = 14V; V_{REF}/ENABLE > 2.75V; -40°C ≤ T_J ≤ +125°C; unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ **Regulator Output 1, 2**					
$V_{REF} - V_{OUT}$	4.5V ≤ V_{IN} ≤ 26V,	-10		10	mV
V_{OUT} Tracking Error	100µA ≤ I_{OUT} ≤ 200mA (Note 1)				
Dropout Voltage	I_{OUT} = 100µA		100	150	mV
($V_{IN} - V_{OUT}$)	I_{OUT} = 200mA		350	600	mV
Line Regulation	4.5V ≤ V_{IN} ≤ 26V (Note 1)			10	mV
Load Regulation	100µA ≤ I_{OUT} ≤ 200mA (Note 1)			10	mV
Adj Lead Current	Loop in Regulation		0.2	1.0	µA
Current Limit	V_{IN} = 14V, V_{REF} = 5V, V_{OUT} = 90% of V_{REF}, (Note 1)	225		700	mA
Quiescent Current	V_{IN} = 12V, I_{OUT} = 200mA		15	25	mA
($I_{IN} - I_{OUT}$)	V_{IN} = 12V, I_{OUT} = 100µA, T_J ≤ 85°C		50	100	µA
	V_{IN} = 12V, V_{REF} / ENABLE = 0V, T_J ≤ 85°C		20	30	µA
Reverse Current	V_{OUT} = 5V, V_{IN} = 0V		0.2	1.5	mA
Ripple Rejection	*f* = 120Hz, I_{OUT} = 200mA, 4.5V ≤ V_{IN} ≤ 26V	60			dB
Thermal Shutdown	GBD	150	180	210	°C
■ **V_{REF}/ENABLE 1, 2**					
Enable Voltage		0.80	2.00	2.75	V
Input Bias Current	V_{REF} / ENABLE 1, 2 > 2V	0		1	µA

Note 1: V_{OUT} connected to Adj lead.

Package Lead Description

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
20 Lead SOIC (Fused)		
1	V_{IN1}	Input voltage for V_{OUT1}.
2	V_{OUT1}	Regulated output voltage 1.
3, 4, 7, 8, 13, 14, 17, 18	NC	No connection.
5, 6, 15, 16	Gnd	Ground.
9	V_{ADJ1}	Adjust lead for V_{OUT1}.
10	V_{REF} / ENABLE1	Reference voltage and ENABLE input for V_{OUT1}.
11	V_{ADJ2}	Adjust lead for V_{OUT2}.
12	V_{REF} / ENABLE2	Reference voltage and ENABLE input for V_{OUT2}.
19	V_{IN2}	Input voltage for V_{OUT2}.
20	V_{OUT2}	Regulated output voltage2 .

Circuit Description

ENABLE Function

By pulling the V_{REF} / ENABLE 1, 2 lead below 2.0V typically, (see Figure 4 or Figure 5), the IC is disabled and enters a sleep state where the device draws less than 30µA from supply. When the V_{REF} / ENABLE lead is greater than 2.75V, V_{OUT} tracks the V_{REF} / ENABLE lead normally.

Output Voltage

Figures 1 through 6 only display one channel of the device for simplicity. The configurations shown apply for both channels.

The outputs are capable of supplying 200mA to the load while configured as a similar (Figure 1), lower (Figure 3), or higher (Figure 2) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the V_{REF} lead as the non-inverting.

The device can also be configured as a high-side driver as displayed in Figure 6.

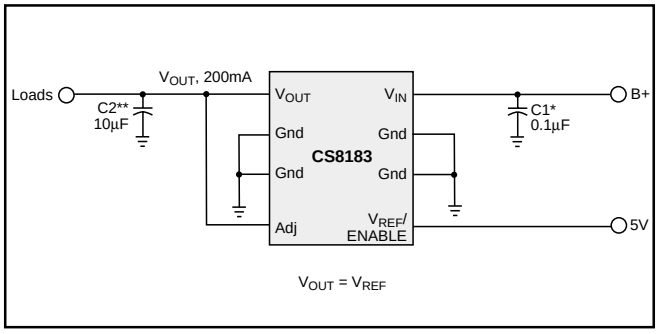


Figure 1: Tracking regulator at the same voltage.

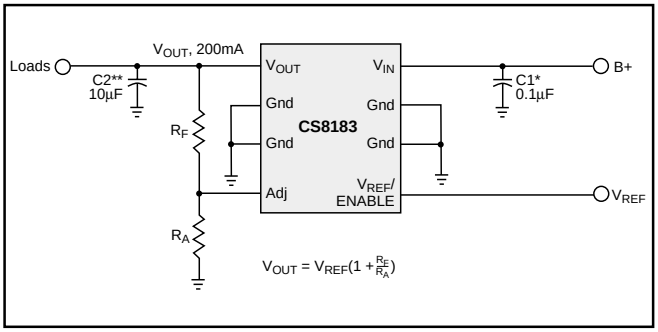


Figure 2: Tracking regulator at higher voltages.

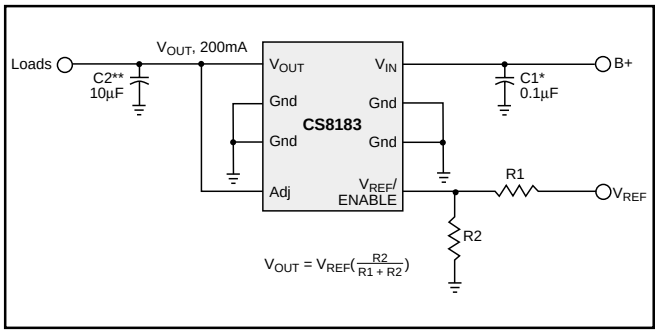


Figure 3: Tracking regulator at lower voltages.

* C_1 is required if the regulator is far from the power source filter.
** C_2 is required for stability.

Circuit Description: continued

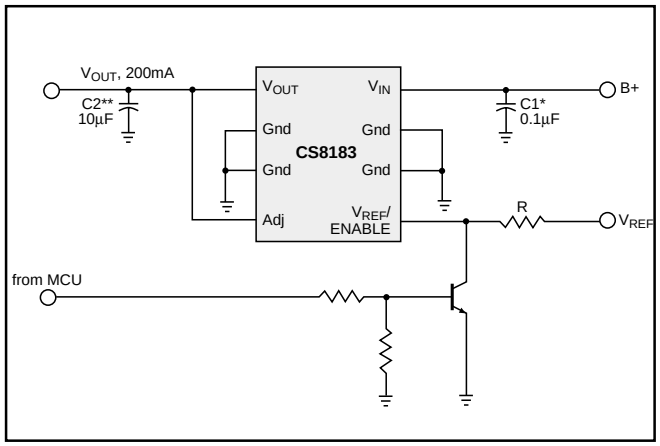


Figure 4: Tracking regulator with ENABLE circuit.

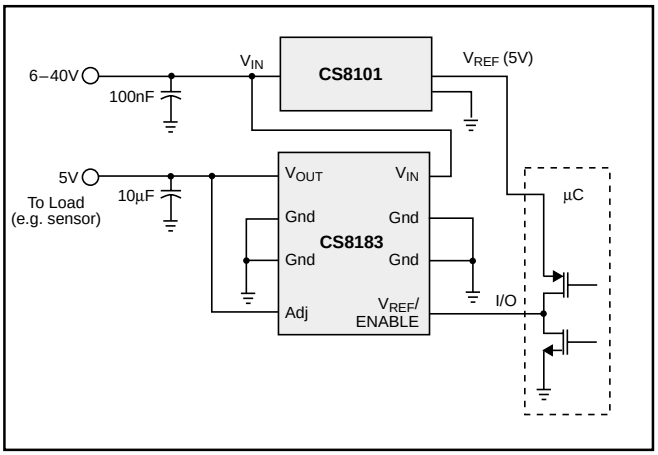


Figure 5: Alternative ENABLE circuit.

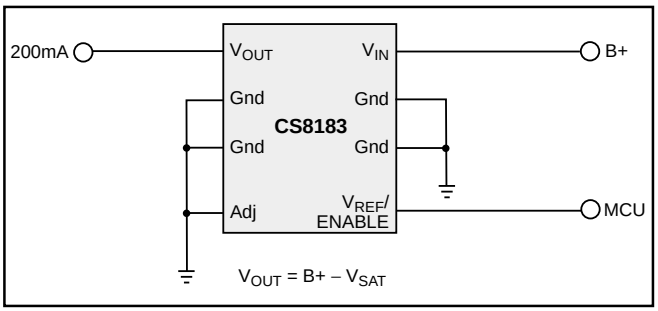


Figure 6: High-Side Driver.

Application Notes

External Capacitors

Output capacitors for the CS8183 are required for stability. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is determined at the minimum ambient temperature and maximum load expected.

The output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to -40˚C, a capacitor rated at that temperature must be used.

More information on capacitor selection for Smart Regulators™ is available in the Smart Regulator application note, “Compensation for Linear Regulators.”

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 5) is:

$$PD(max) = \{V_{IN}(max) - V_{OUT1}(min)\}I_{OUT1}(max) + \{V_{IN}(max) - V_{OUT2}(min)\}I_{OUT2}(max) + V_{IN}(max)I_Q \quad (1)$$

Where

$V_{IN}(max)$ is the maximum input voltage,
$V_{OUT1}(min)$ is the minimum output voltage from V_{OUT1},
$V_{OUT2}(min)$ is the minimum output voltage from V_{OUT2},
$I_{OUT1}(max)$ is the maximum output current, for the application
$I_{OUT2}(max)$ is the maximum output current, for the application
I_Q is the quiescent current the regulator consumes at $I_{OUT}(max)$.

Once the value of PD(max) is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.

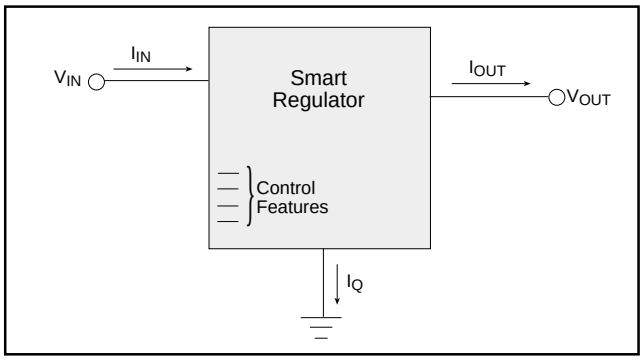


Figure 5: Dual output regulator with key performance parameters labeled.

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heatsink manufacturers.

Package Specification

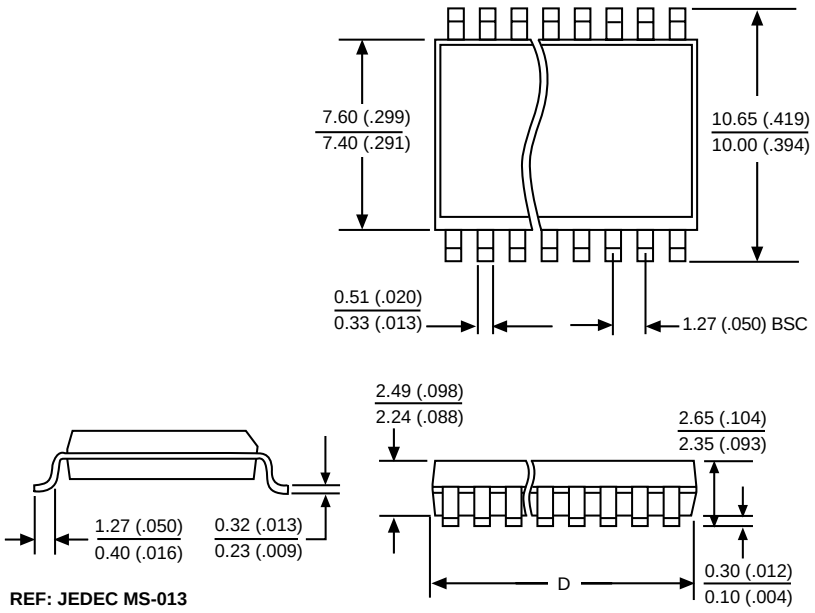
PACKAGE DIMENSIONS IN mm (INCHES)

	D			
Lead Count	**Metric**		**English**	
	Max	Min	Max	Min
20 Lead SOIC Wide*	13.00	12.60	.512	.496

PACKAGE THERMAL DATA

Thermal Data		**20 Lead SO Wide***	
$R_{\Theta JC}$	typ	18	˚C/W
$R_{\Theta JA}$	typ	73	˚C/W

Surface Mount Wide Body (DW); 300 mil wide



REF: JEDEC MS-013

Ordering Information

Part Number	**Description**
CS8183YDWF20	20 Lead SO Wide*
CS8183YDWFR20	20 Lead SO Wide* *(tape & reel)*

*Internally Fused Leads (4L fused)

Notes

Notes