AUTOMOTIVE GRADE

CS8182

Micropower 200mA Low Dropout Tracking Regulator/Line Driver

Description

The CS8182 is a monolithic integrated low dropout tracking regulator designed to provide an adjustable buffered output voltage that closely tracks (±10mV) the reference input. The output delivers up to 200mA while being able to be configured higher, lower or equal to the reference voltage.

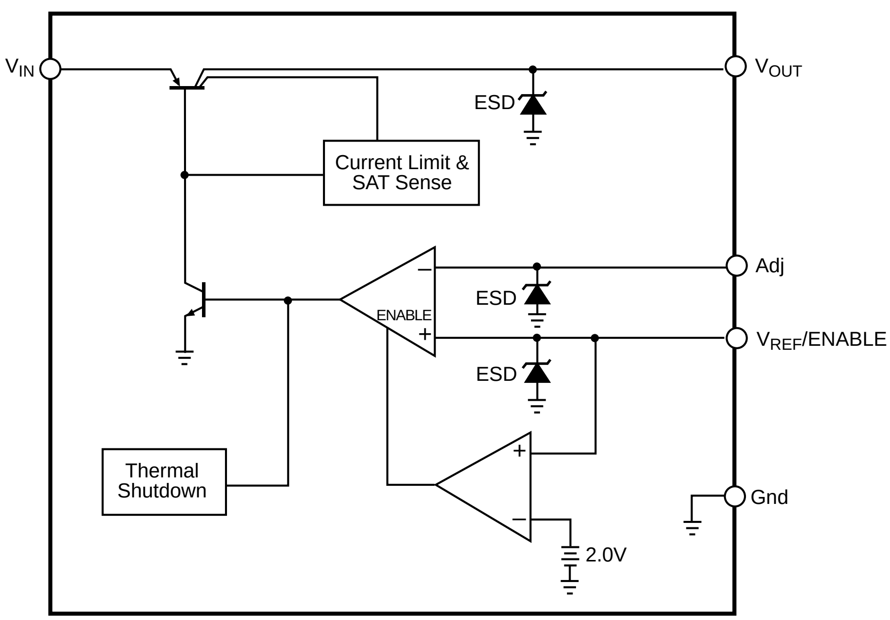
The output has been designed to operate over a wide range (2.8V to 40V) while still maintaining excellent DC characteristics. The CS8182 is protected from reverse battery, short circuit and thermal runaway conditions. The device also can withstand 45V load dump transients and –50V reverse polarity input voltage transients. This makes it suitable for use in automotive environments.

The V_{REF} / ENABLE lead serves two purposes. It is used to provide the input voltage as a reference for the output and it also can be pulled low to place the device in sleep mode where it nominally draws less than 10µA from the supply.

Features

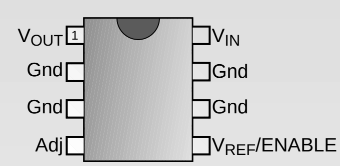
- **200mA Source Capability**
- **Output Tracks within ±10mV Worst Case**
- **Low Dropout (0.35V typ. @ 200mA)**
- **Low Quiescent Current**
- **Thermal Shutdown**
- **Short Circuit Protection**
- **Wide Operating Range**

Block Diagram



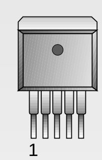
Package Options

8 Lead SO Narrow



5 Lead D^{2}PAK

Tab (Gnd)



1 V_{IN}
2 V_{OUT}
3 Gnd
4 Adj
5 V_{REF}

Consult Factory for 8 Lead SOIC with exposed pad.

ON Semiconductor

ON Semiconductor
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885–3600 Fax: (401)885–5786
N. American Technical Support: 800-282-9855
Web Site: www.onsemi.com

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Absolute Maximum Ratings

Storage Temperature .... –65°C to 150°C
Supply Voltage Range (continuous) .... –15V to 40V
Supply Voltage Range (normal, continuous) .... 3.4V to 40V
Peak Transient Voltage (V_{IN} = 14V, Load Dump Transient = 31V) 45V
Voltage Range (Adj, V_{OUT}, V_{REF}/ENABLE) .... –10V to 45V
Maximum Junction Temperature .... 150°C
ESD Capability (Human Body Model) 2kV
Lead Temperature Soldering
  Wave Solder(through hole styles only) .... 10 sec. max, 260°C peak
  Reflow (SMD styles only) .... 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: V_{IN} = 14V; V_{REF}/ENABLE > 2.75V; –40°C < T_J < 125°C; C_{OUT} ≥ 10µF; 0.1Ω ≤ $C_{OUT-ESR}$ ≤ 10Ω @ 10kHz, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Regulator Output					
$V_{REF} - V_{OUT}$ V_{OUT} Tracking Error	4.5V ≤ V_{IN} ≤ 26V, 100µA ≤ I_{OUT} ≤ 200mA (Note 1)	–10		10	mV
Dropout Voltage ($V_{IN} - V_{OUT}$)	I_{OUT} = 100µA I_{OUT} = 200mA		100 350	150 600	mV mV
Line Regulation	4.5V ≤ V_{IN} ≤ 26V (Note 1)			10	mV
Load Regulation	100µA ≤ I_{OUT} ≤ 200mA (Note 1)			10	mV
Adj Lead Current	Loop in Regulation		0.2	1.0	µA
Current Limit	V_{IN} = 14V, V_{REF} = 5V, V_{OUT} = 90% V_{REF} (Note 1)	225		700	mA
Quiescent Current ($I_{IN} - I_{OUT}$)	V_{IN} = 12V, I_{OUT} = 200mA V_{IN} = 12V, I_{OUT} = 100µA, T_J ≤ 85°C V_{IN} = 12V, V_{REF}/ENABLE = 0V, T_J ≤ 85°C		15 50 10	25 100 30	mA µA µA
Reverse Current	V_{OUT} = 5V, V_{IN} = 0V		0.2	1.5	mA
Ripple Rejection	*f* = 120Hz, I_{OUT} = 200mA, 4.5V ≤ V_{IN} ≤ 26V	60			dB
Thermal Shutdown	GBD	150	180	210	°C
■ V_{REF}/ENABLE					
Enable Voltage		0.80	2.00	2.75	V
Input Bias Current	V_{REF}/ENABLE	0		1	µA

Note 1: V_{OUT} connected to Adj lead.

Package Lead Description

PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
5 Lead D²PAK	**8 Lead SOIC Narrow**		
1	8	V_{IN}	Input voltage.
2	1	V_{OUT}	Regulated output.
3	2, 3, 6, 7	Gnd	Ground.
4	4	Adj	Adjust lead.
5	5	V_{REF}/ENABLE	Reference voltage and ENABLE input.

Circuit Description

ENABLE Function

By pulling the V_{REF}/ENABLE lead below 2V typically, (see Figure 4 or Figure 5), the IC is disabled and enters a sleep state where the device draws less than 10μA from supply. When the V_{REF}/ENABLE lead is greater than 2.75V, V_{OUT} tracks the V_{REF}/ENABLE lead normally.

Output Voltage

The output is capable of supplying 200mA to the load while configured as a similar (Figure 1), lower (Figure 3), or higher (Figure 2) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the V_{REF} lead as the non-inverting.

The device can also be configured as a high-side driver as displayed in Figure 6.

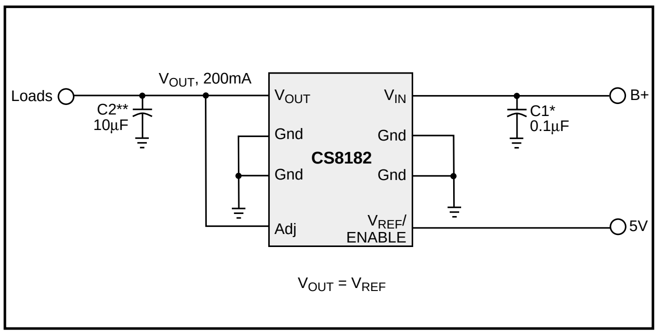


Figure 1: Tracking regulator at the same voltage.

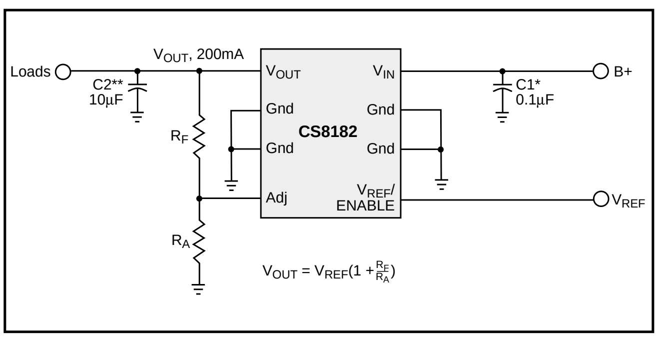


Figure 2: Tracking regulator at higher voltages.

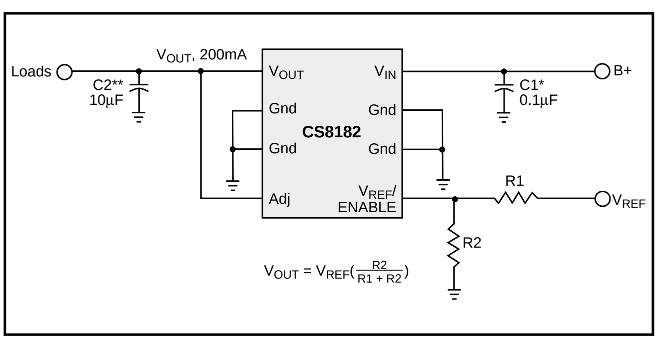


Figure 3: Tracking regulator at lower voltages.

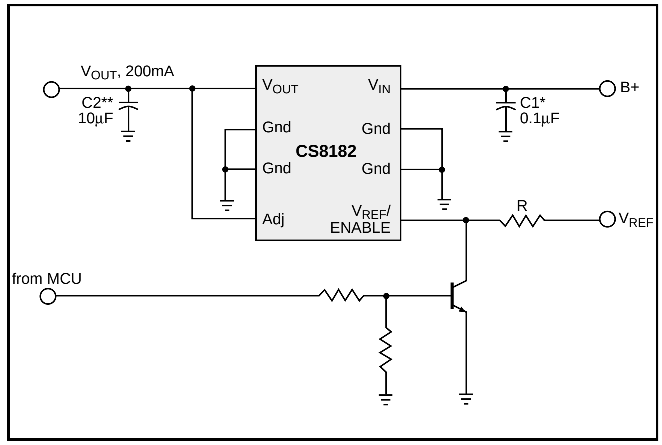


Figure 4: Tracking regulator with ENABLE circuit.

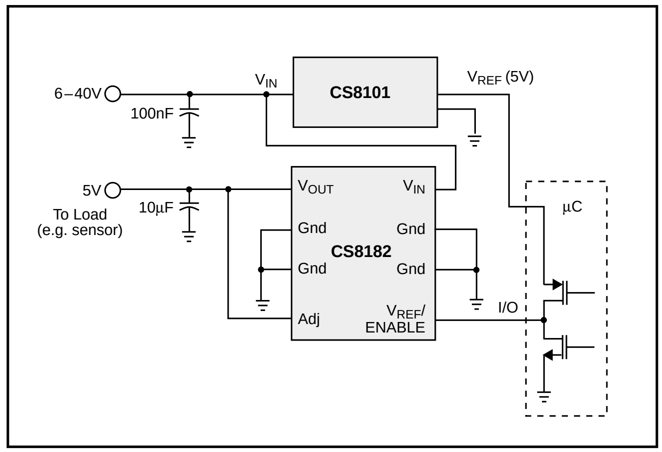


Figure 5: Alternative ENABLE circuit.

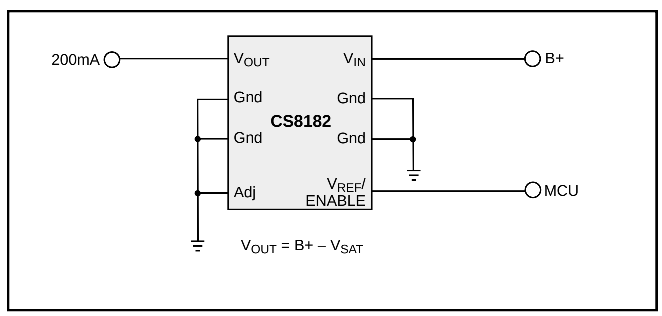


Figure 6: High-Side Driver.

* C_1 is required if the regulator is far from the power source filter.

** C_2 is required for stability.

Application Notes

External Capacitors

The output capacitor for the CS8182 is required for stability. Without it, the regulator output will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is determined at the minimum ambient temperature and maximum load expected.

The output capacitor can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitor must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to -40°C, a capacitor rated at that temperature must be used.

More information on capacitor selection for Smart Regulators™ is available in the Smart Regulator application note, "Compensation for Linear Regulators."

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 1) is:

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT(min)}\}I_{OUT(max)} + V_{IN(max)}I_Q \qquad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \qquad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

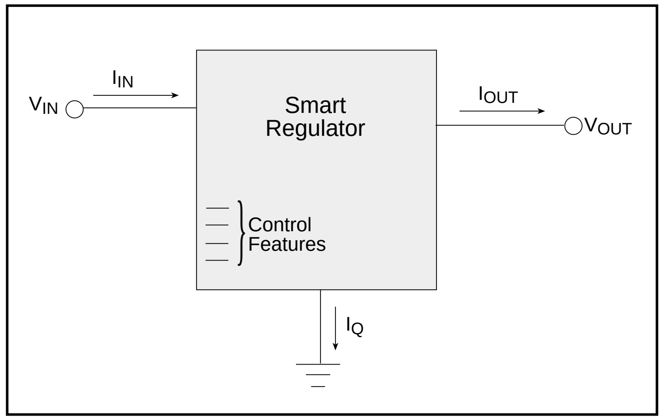


Figure 1. Single output regulator with key performance parameters labeled.

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \qquad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heatsink manufacturers.

Package Specification

PACKAGE DIMENSIONS IN mm (INCHES)

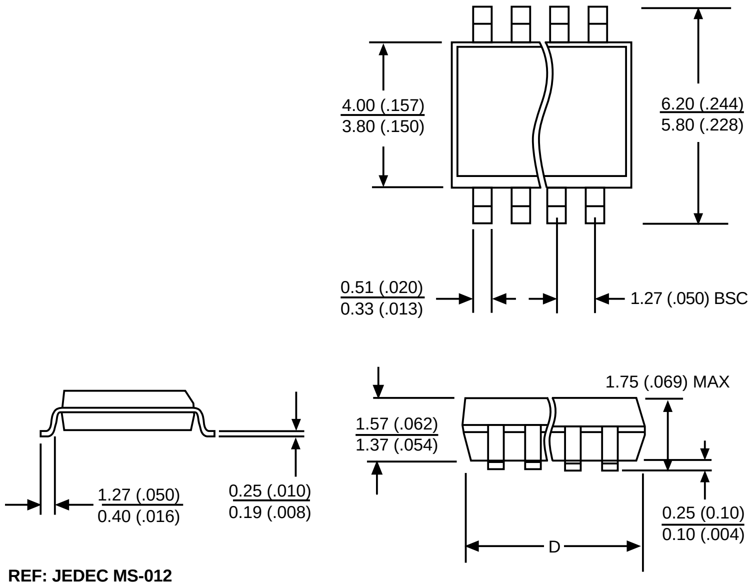
Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8 Lead SOIC Narrow	5.00	4.80	.197	.189

PACKAGE THERMAL DATA

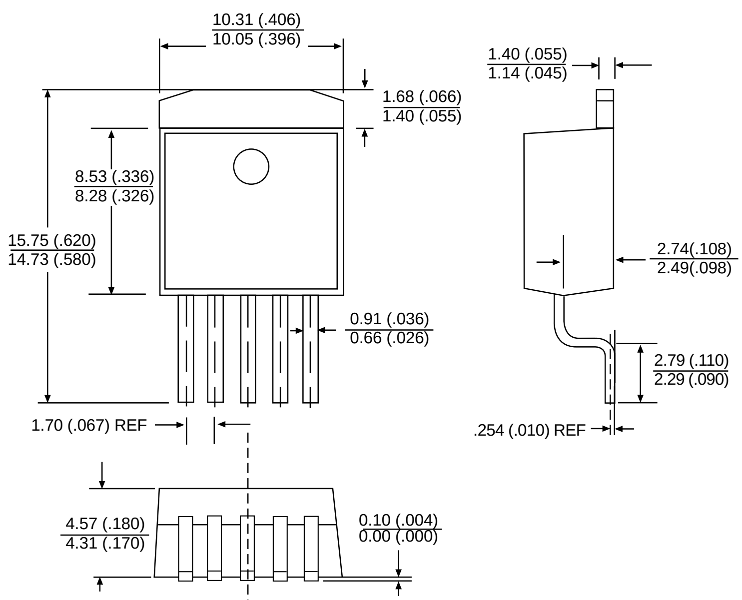
Thermal Data		5 Lead D^2PAK	8 Lead SOIC Narrow	
$R_{\Theta JC}$	typ	4.0	45	°C / W
$R_{\Theta JA}$	typ	10-50*	165	°C / W

* *Depending on thermal properties of substrate.* $R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$

Surface Mount Narrow Body (D); 150 mil wide



5 Lead D^2PAK (DP)



Ordering Information

Part Number	Description
CS8182YDP5	5 Lead D^2PAK
CS8182YDPR5	5 Lead D^2PAK *(tape & reel)*
CS8182YD8	8 Lead SOIC Narrow
CS8182YDR8	8 Lead SOIC Narrow *(tape & reel)*

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