AUTOMOTIVE GRADE

CS8101

Micropower 5V, 100mA Low Dropout Linear Regulator with $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$

Description

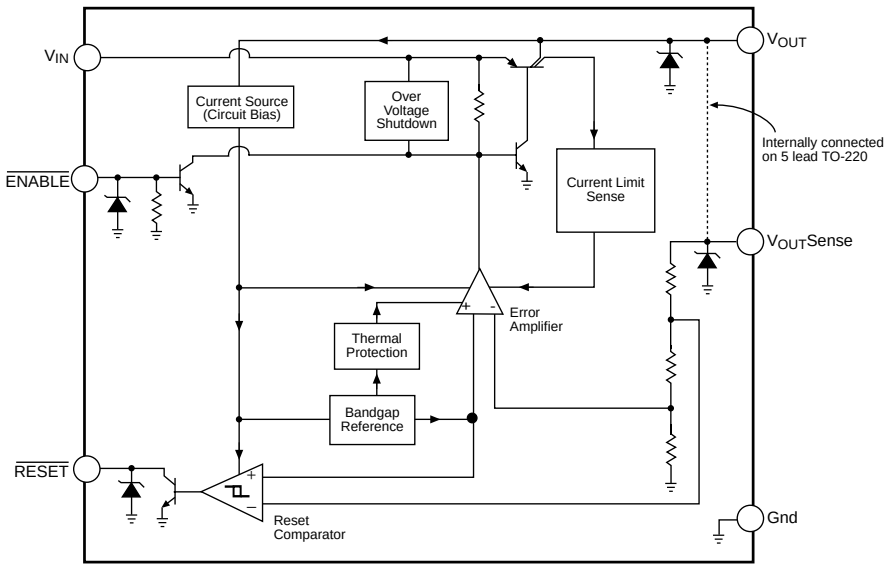
The CS8101 is a precision 5V micropower voltage regulator with very low quiescent current (70µA typ at 100µA load). The 5V output is accurate within ±2% and supplies 100mA of load current with a typical dropout voltage of only 400mV. Microprocessor control logic includes an $\overline{\text{ENABLE}}$ input and an active $\overline{\text{RESET}}$. This combination of low quiescent current, outstanding regulator performance and control logic makes the CS8101 ideal for any battery operated, microprocessor controlled equipment.

The active $\overline{\text{RESET}}$ circuit includes hysteresis, and operates correctly at an output voltage as low as 1V. The $\overline{\text{RESET}}$ function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits by more than 200mV typ. The logic level compatible $\overline{\text{ENABLE}}$ input allows the user to put the regulator into a shutdown mode where it draws only 20µA typical of quiescent current.

The regulator is protected against reverse battery, short circuit, over voltage, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

The CS8101 is functionally equivalent to the National Semiconductor LP2951 series low current regulators.

Block Diagram



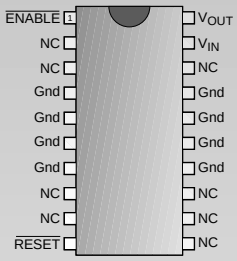
Features

- **5V ±2% Output**
- **Low 70µA Quiescent Current**
- **Active $\overline{\text{RESET}}$**
- **$\overline{\text{ENABLE}}$ Input for ON/OFF and Active/Sleep Mode Control**
- **100mA Output Current Capability**
- **Fault Protection**
  - **+60V Peak Transient Voltage**
  - **–15V Reverse Voltage**
  - **Short Circuit**
  - **Thermal Overload**
- **Low Reverse Current (Output to Input)**

Package Options

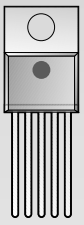
20L SOIC Wide

(Internally Fused Leads)



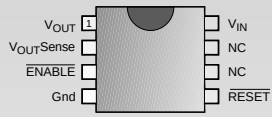
5L TO-220

Tab (Gnd)



1. V_{OUT}
2. $\overline{\text{ENABLE}}$
3. Gnd
4. $\overline{\text{RESET}}$
5. V_{IN}

8L SOIC



Other Packages: D^2PAK (consult factory)

ON Semiconductor

ON Semiconductor
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885–3600 Fax: (401)885–5786
N. American Technical Support: 800-282-9855
Web Site: www.cherry–semi.com

Absolute Maximum Ratings

Power Dissipation ..... Internally Limited
Transient Peak Voltage (46V Load Dump) ..... –15V, 60V
Output Current ..... Internally Limited
ESD Susceptibility (Human Body Model) 2kV
Operating Temperature ..... –40°C to 125°C
Junction Temperature ..... –40°C to 150°C
Storage Temperature ..... –55C to 150°C
Lead Temperature Soldering Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak
Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: $6V \le V_{IN} \le 26V$; $I_{OUT} = 1mA$; $-40 \le T_A \le 125$; $-40 \le T_J \le 150°C$; unless otherwise specified.

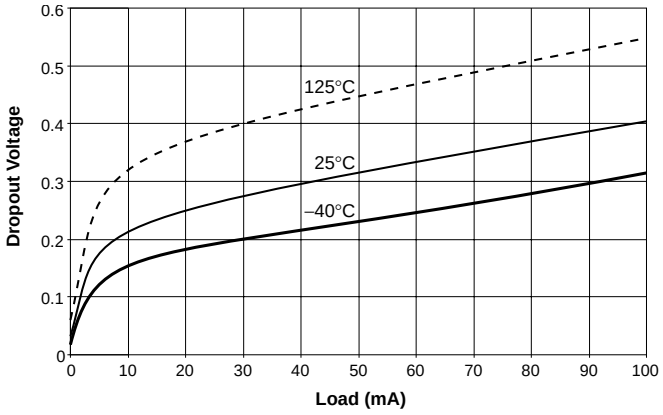
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Output Stage					
Output Voltage, V_{OUT}	$9V < V_{IN} < 16V$, $100\mu A \le I_{OUT} \le 100mA$	4.90	5.00	5.10	V
	$6V \le V_{IN} \le 26V$, $100\mu A \le I_{OUT} \le 100mA$	4.85	5.00	5.15	V
Dropout Voltage ($V_{IN} - V_{OUT}$)	$I_{OUT} = 100mA$		400	600	mV
	$I_{OUT} = 100\mu A$		100	150	mV
Load Regulation	$V_{IN} = 14V$, $100\mu A \le I_{OUT} \le 100mA$		5	50	mV
Line Regulation	$6V < V < 26V$, $I_{OUT} = 1mA$		5	50	mV
Quiescent Current, (I_Q)					
Active Mode	$I_{OUT} = 100\mu A$, $V_{IN} = 6V$		70	140	µA
	$I_{OUT} = 50mA$		4	6	mA
	$I_{OUT} \le 100mA$		12	20	mA
Sleep Mode	V_{OUT} = OFF, $V_{IN} = 6V$, $V_{\overline{ENABLE}} = 2V$		20	50	µA
Ripple Rejection	$7 \le V_{IN} \le 17V$, $I_{OUT} = 100mA$, f = 120Hz	60	75		dB
Current Limit		105	200		mA
Short Circuit Output Current	$V_{OUT} = 0V$	25	125		mA
Thermal Shutdown		150	180		°C
Overvoltage Shutdown	$V_{OUT} \le 1V$	30	34	38	V
Reverse Current	$V_{OUT} = 5V$, $V_{IN} = 0V$		100	200	µA
■ Enable Input ($\overline{ENABLE}$)					
Threshold					
HIGH	(V_{OUT} OFF)		1.4	2.0	V
LOW	(V_{OUT} ON)	0.6	1.4		V
Input Current	$V_{\overline{ENABLE}} = 2.4V$		30	100	µA
■ Reset Function ($\overline{RESET}$)					
$\overline{RESET}$ Threshold					
HIGH (V_{RH})	V_{OUT} Increasing	4.525	4.75	$V_{OUT} - 0.05$	V
LOW (V_{RL})	V_{OUT} Decreasing	4.500	4.700	$V_{OUT} - 0.075$	V
$\overline{RESET}$ Hysteresis	(HIGH – LOW)	25	50	100	mV
Reset Output Leakage $\overline{RESET}$ = HIGH	$V_{OUT} \ge V_{RH}$			25	µA
Output Voltage					
Low (V_{RLO}) $R_{\overline{RESET}} = 10K$	$1V \le V_{OUT} \le V_{RL}$		0.1	0.4	V
Low (VRpeak)	V_{OUT}, Power up, Power down		0.6	1.0	V

Package Lead Description

PACKAGE LEAD #			LEAD SYMBOL	FUNCTION
8 Lead SOIC	**20 Lead SOIC** (Internally Fused Leads)	**5 Lead TO-220**		
8	19	5	V_{IN}	Input voltage.
1	20	1	V_{OUT}	5V, ±2%, 100mA output.
3	1	2	$\overline{\text{ENABLE}}$	Logic level switches output off when toggled HIGH.
4	4,5,6,7 14,15,16,17	3	Gnd	Ground. All Gnd leads must be connected to Ground.
5	10	4	$\overline{\text{RESET}}$	Active reset (accurate to $V_{OUT} \geq 1V$).
2			V_{OUT}Sense	Kelvin connection which allows remote sensing of output voltage for improved regulation. If remote sensing is not required, connect to V_{OUT}.
6,7	2,3,8,9,11,12,13,18		NC	No Connection.

Typical Performance Characteristics

CS8101 Dropout Voltage vs Load over Temperature



Circuit Description

Voltage Reference and Output Circuitry

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 1).

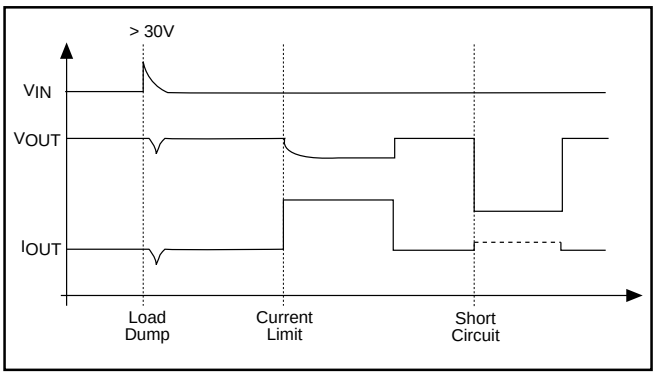


Figure 1. Typical Circuit Waveforms for Output Stage Protection.

If the input voltage rises above 30V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed 180°C (typ) the load current capability is reduced thereby preventing thermal overload. This thermal management function is an effective means to prevent die overheating since the load current is the principle heat source in the IC.

Regulator Control Functions

The CS8101 contains two microprocessor compatible control functions: $\overline{\text{ENABLE}}$ and $\overline{\text{RESET}}$ (Figure 2).

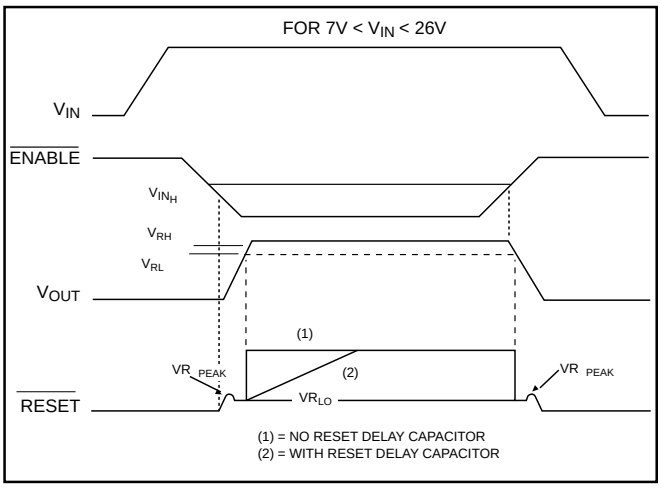


Figure 2. Circuit Waveform

$\overline{\text{ENABLE}}$ Function

The $\overline{\text{ENABLE}}$ function switches the output transistor ON and OFF. When the voltage on the $\overline{\text{ENABLE}}$ lead exceeds 1.4V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only 50µA, until the voltage on this input drops below the $\overline{\text{ENABLE}}$ threshold.

$\overline{\text{RESET}}$ Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up until V_{OUT} is within 250mV of the regulated output voltage, or when V_{OUT} drops out of regulation,and is lower than 300mV below the regulated output voltage. A hysteresis of 50mV is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1V.

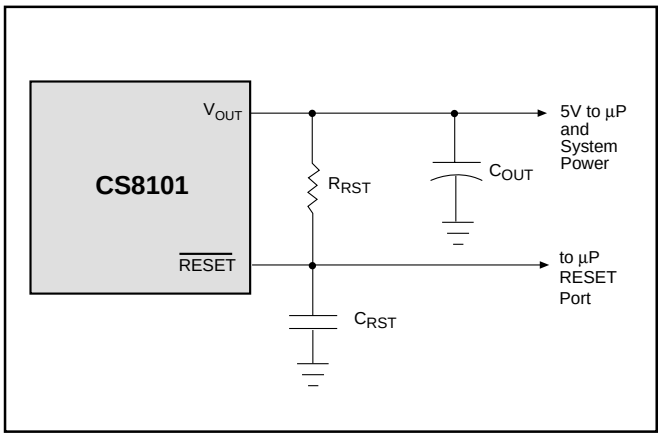


Figure 3. RC Network for $\overline{\text{RESET}}$ Delay

An external RC network on the $\overline{\text{RESET}}$ lead (Figure 3) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$R_{TOT}C_{RST} = \left[\frac{-t_{Delay}}{\ln\left(\frac{V_T - V_{OUT}}{V_{RST} - V_{OUT}}\right)}\right]$$

where:
- R_{RST} = $\overline{\text{RESET}}$ Delay resistor
- R_{IN} = µP port impedance
- R_{TOT} = R_{RST} in parallel with R_{IN}
- C_{RST} = $\overline{\text{RESET}}$ Delay capacitor
- t_{Delay} = desired delay time
- V_{RST} = V_{SAT} of $\overline{\text{RESET}}$ lead (0.7V @ turn - ON)
- V_T = $\overline{\text{RESET}}$ threshold

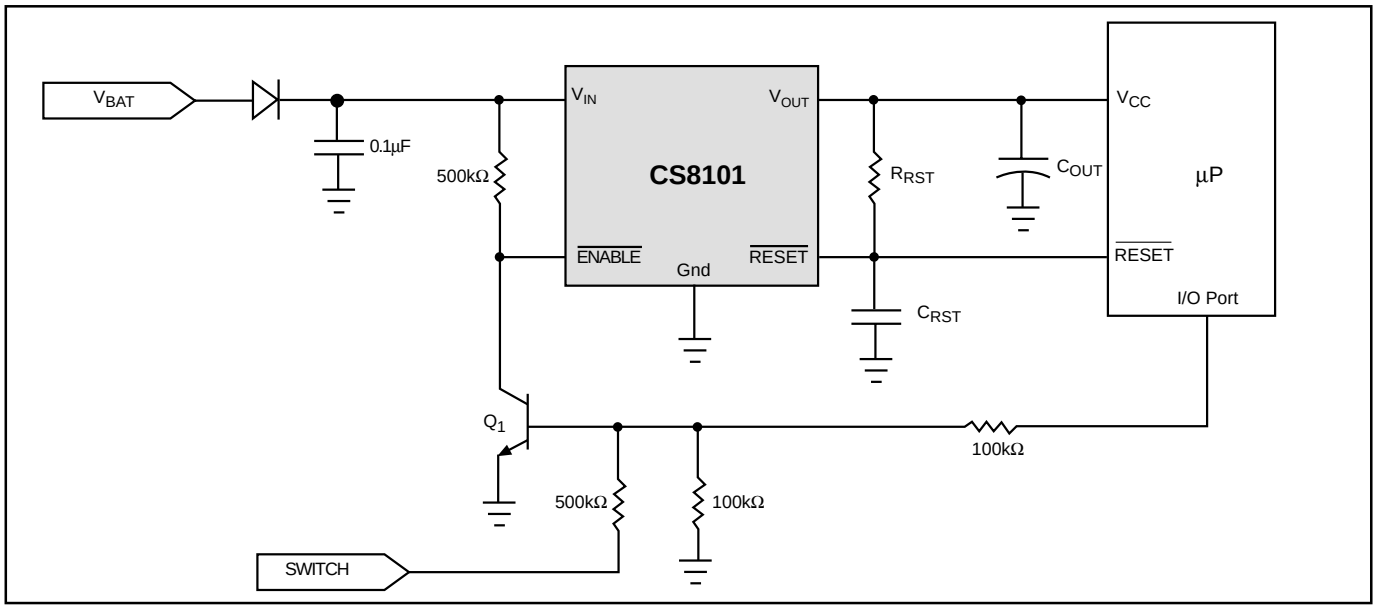


Figure 4. Microprocessor Control of CS8101 using external switching transistor Q1.

The circuit depicted in Figure 4 lets the microprocessor control its power source, the CS8101 regulator. An I/O port on the µP and the SWITCH port are used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the $\overline{\text{ENABLE}}$ lead falls below its lower threshold. The regulator's output is enabled. When the drive current is removed, the voltage on the $\overline{\text{ENABLE}}$ lead rises, the output is switched off and the IC moves into Sleep mode where it draws 50µA (max).

By coupling these two controls with the $\overline{\text{ENABLE}}$ lead, the system has added flexibility. Once the system is running, the state of the SWITCH is irrelevant as long as the I/O port continues to drive Q1. The microprocessor can turn off its own power by withdrawing drive current, once the SWITCH is open. This software control at the I/O port allows the microprocessor to finish key housekeeping functions before power is removed.

The logic options are summarized in Table 1.

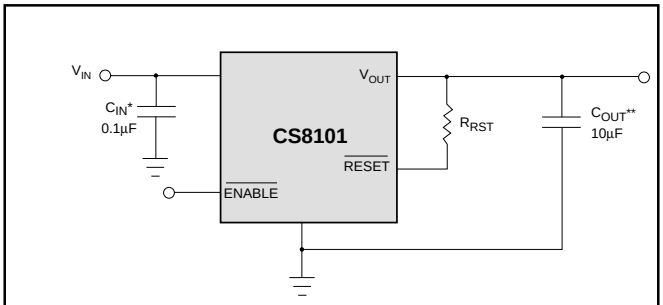
Table 1. Logic Control of CS8101 Output

Microprocessor I/O drive	Switch	$\overline{\text{ENABLE}}$	Output
ON	Closed	LOW	ON
	Open	LOW	ON
OFF	Closed	LOW	ON
	Open	HIGH	OFF

The I/O port of the microprocessor typically provides 50µA to Q1. In automotive applications the SWITCH is connected to the ignition switch.

Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.



*C_{IN} required if regulator is located far from the power supply filter.
**C_{OUT} required for stability. Capacitor must operate at minimum temperature expected.

Figure 5. Test and application circuit showing output compensation.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 5 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the

higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 6) is:

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT(min)}\}I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

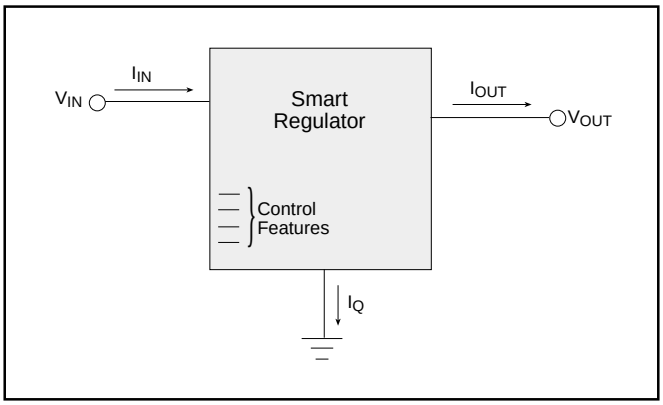


Figure 6: Single output regulator with key performance parameters labeled.

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

Package Specification

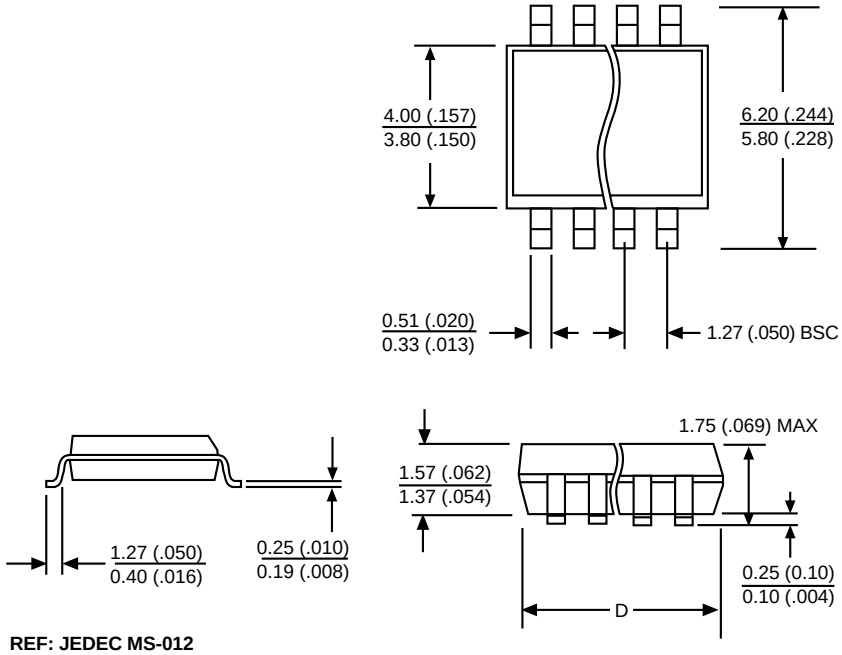
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8L SOIC	5.00	4.80	.197	.189
20L SOIC	13.00	12.60	.512	.496

PACKAGE THERMAL DATA

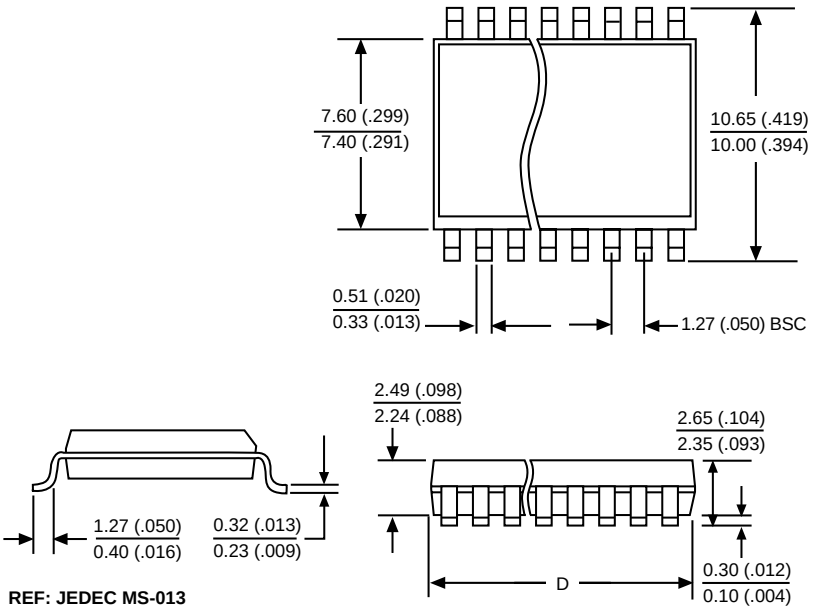
Thermal Data		8 Lead SOIC	20 Lead SOIC Wide	5 Lead TO-220	
$R_{\Theta JC}$	typ	45	9	3.3	°C / W
$R_{\Theta JA}$	typ	165	55	50	°C / W

Surface Mount Narrow Body (D); 150 mil wide



REF: JEDEC MS-012

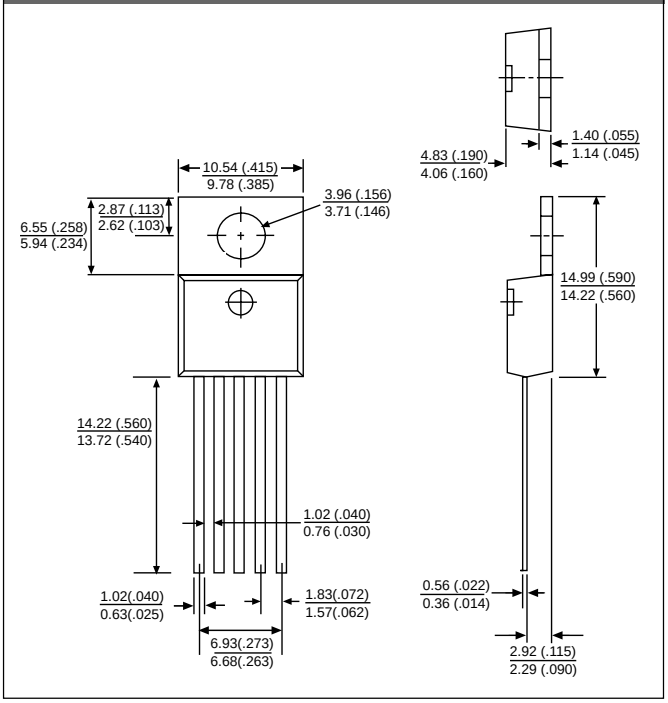
Surface Mount Wide Body (DW); 300 mil wide



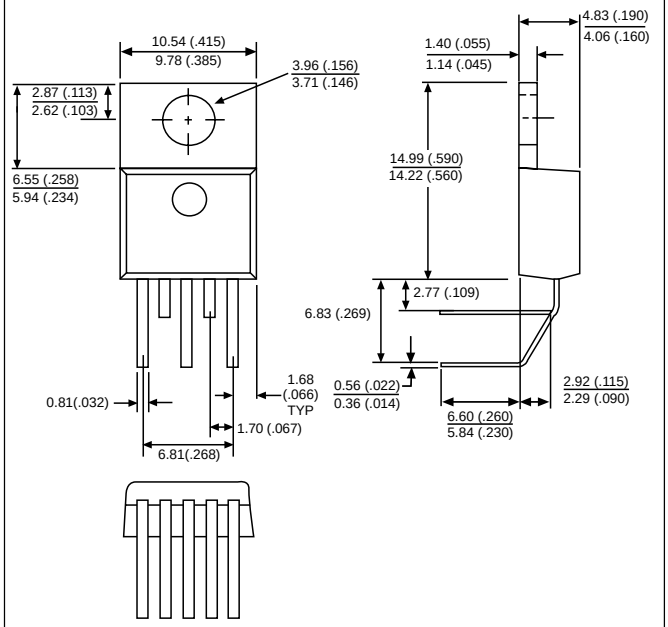
REF: JEDEC MS-013

Package Specification

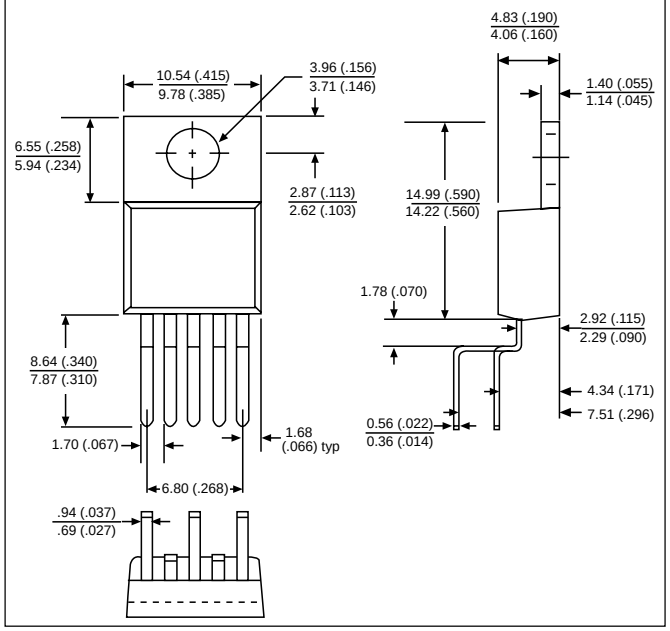
5 Lead TO-220 (T) Straight



5 Lead TO-220 (THA) Horizontal



5 Lead TO-220 (TVA) Vertical



Ordering Information

Part Number	Description
CS8101YD8	8L SOIC
CS8101YDR8	8L SOIC *(tape & reel)*
CS8101YDWF20	20L SOIC (internally fused leads)
CS8101YDWFR20	20L SOIC (internally fused leads) *(tape & reel)*
CS8101YT5	5L TO-220
CS8101YTVA5	5L TO-220 Vertical
CS8101YTHA5	5L TO-220 Horizontal