AUTOMOTIVE GRADE

CS7054

Low Side PWM FET Controller

Description

The CS7054 is a monolithic integrated circuit designed primarily to control the rotor speed of permanent magnet, direct current (DC) brush motors. It drives the gate of an N channel power MOSFET or IGBT with a user-adjustable, fixed frequency, variable duty cycle, pulse width modulated (PWM) signal. The CS7054 can also be used to control other loads such as incandescent bulbs and solenoids. Inductive current from the motor or solenoid is recirculated through an external diode.

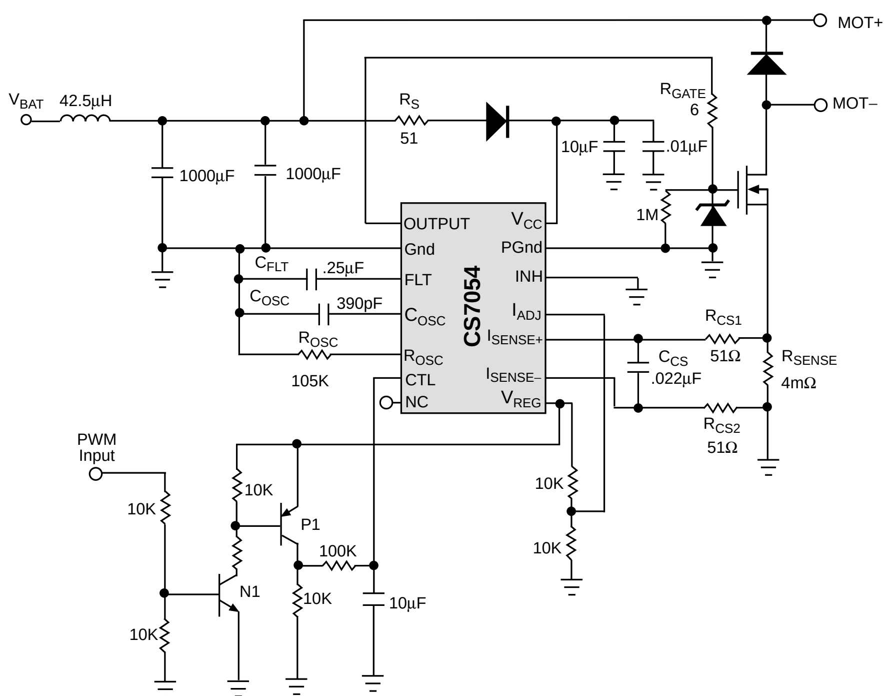
The CS7054 accepts a DC level input signal of 0 to 5V to control the pulse width of the output signal. This signal can be generated by a potentiometer referenced to the on-chip 5V linear regulator, or a filtered 0% to 100% PWM signal also referenced to the 5V regulator.

The IC is placed in a sleep state by pulling the CTL lead below 0.5V. In this mode everything on the chip is shut down except for the on-chip regulator and the overall current draw is less than 275 µA. There are a number of on-chip diagnostics that look for potential failure modes and can disable the external power MOSFET.

Features

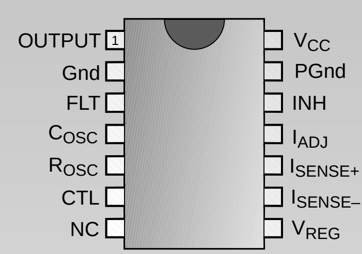
- 200mA Peak PWM Gate Drive Output
- Patented Voltage Compensation Circuit
- 100% Duty Cycle Capability
- 5V, ± 3% Linear Reg.
- Low Current Sleep Mode
- Overvoltage Protection
- Over Current Protection of External MOSFET / IGBT
- Output Inhibit

Application Diagram

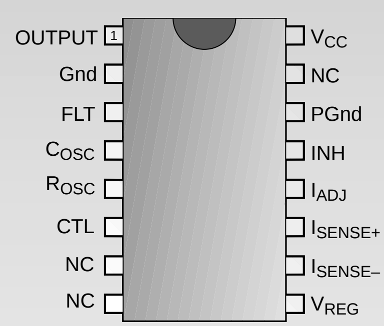


Package Options

14 Lead PDIP



16 Lead SO Wide



ON Semiconductor
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885–3600 Fax: (401)885–5786
N. American Technical Support: 800-282-9855
Web Site: www.cherry–semi.com

ON Semiconductor

Absolute Maximum Ratings

Storage Temperature .... –65°C to 150°C
V_{CC} .... –0.3V to 30V
Supply Voltage Range (load dump = 26Vw / series 51Ω resistor) V_{CC} Peak Transient Voltage 40V
Input Voltage Range (at any input) .... –0.3V to 10V
Maximum Junction Temperature .... 150°C
ESD Capability (Human Body Model) 2kV
Lead Temperature Soldering: Wave Solder (through hole styles only) .... 10 sec. max, 260°C peak
Reflow (SMD styles only) .... 60 sec. max above 183°C, 230°C peak

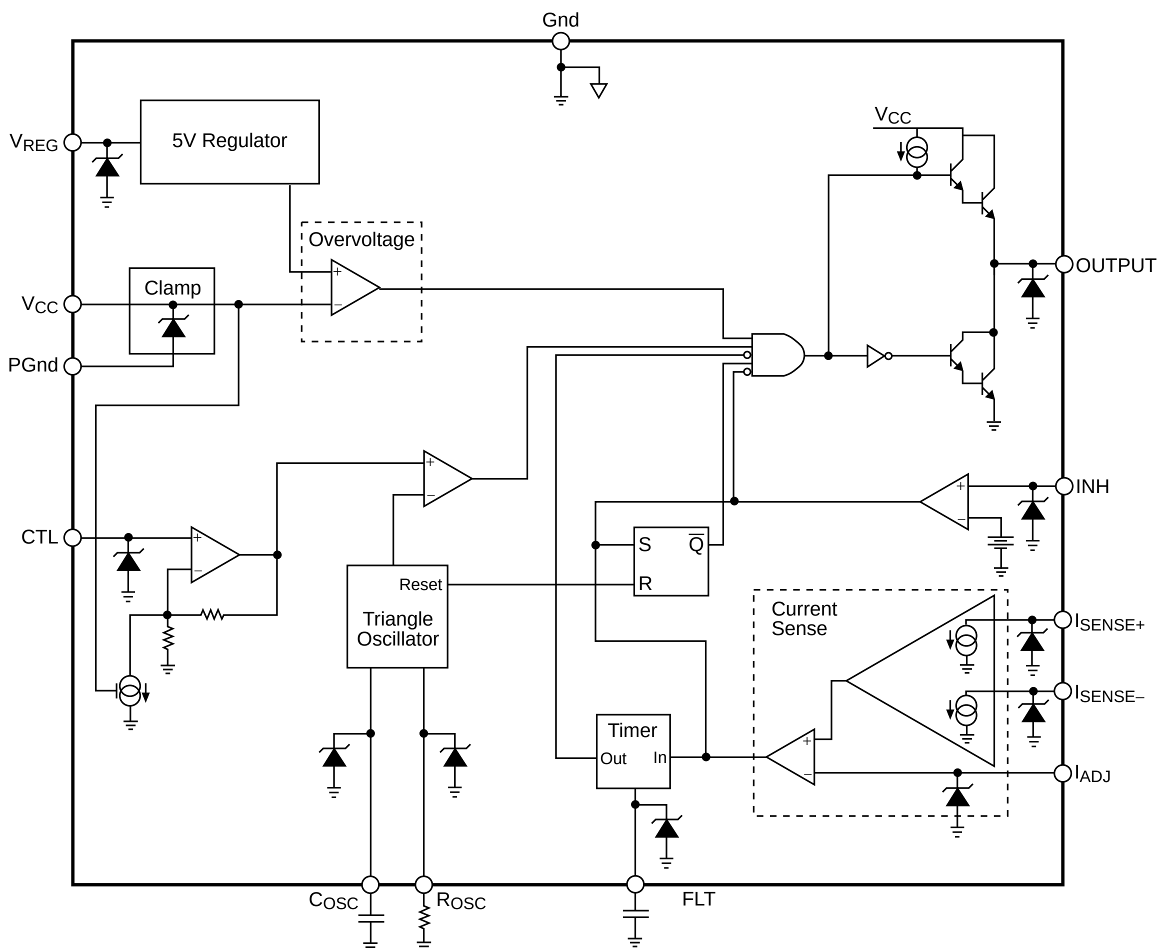
Electrical Characteristics: 8V < V_{CC} < 16V; –40°C < T_A < 125°C; unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ V_{CC} Supply					
Operating Current Supply			5	10	mA
Quiescent Current	V_{CC} = 12V		170	275	µA
Overvoltage Shutdown		18	19.5	21	V
Overvoltage Hysteresis		150	325	500	mV
■ Control (CTL)					
Control Input Current	CTL = 0V to 5V	–2	0.1	2	µA
Sleep Mode Threshold		8%	10%	12%	V_{REG}
Sleep Mode Hysteresis		50	100	150	mV
■ Current Sense					
Differential Voltage Sense	I_{ADJ} = 51.2% V_{REG} and R_{CS1} = 51Ω	60.5		79.5	mV
I_{ADJ} Input Current	I_{ADJ} = 0V to 5V	–5	0.3	2	µA
■ Linear Regulator V_{REG}					
Output Voltage	V_{CC} = 13.2V	4.85	5.00	5.15	V
■ Inhibit					
Inhibit Threshold		40%	50%	60%	V_{REG}
Inhibit Hysteresis		150	325	575	mV
■ External Drive (OUTPUT)					
Output Frequency	R_{OSC} = 105kΩ, C_{OSC} = 390pF	17	20	23	kHz
Voltage to Duty Cycle Conversion	V_{CC} = 13V, CTL = 30% V_{REG} V_{CC} = 13V, CTL = 70% V_{REG}	26.3 69.5		38.5 81.5	% %
Output Rise Time	V_{CC} = 13V, R_{GATE} = 6Ω, C_{GATE} = 5nF		.25	1	µs
Output Fall Time	V_{CC} = 13V, R_{GATE} = 6Ω, C_{GATE} = 5nF		.30	1	µs
Output Sink Current	V_{CC} = 13V, R_{GATE} = 6Ω, C_{GATE} = 5nF		400		mA
Output Source Current	V_{CC} = 13V, R_{GATE} = 6Ω, C_{GATE} = 5nF		400		mA
Output High Voltage	I_{OUT} = 1mA	V_{CC} – 1.7			V
Output Low Voltage	I_{OUT} = –1mA			1.3	V

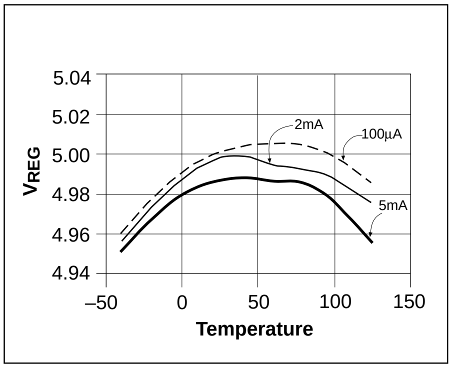
Package Lead Description

PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
14 Lead PDIP	16 Lead SO Wide		
1	1	OUTPUT	MOSFET Gate Drive.
2	2	Gnd	Ground.
3	3	FLT	Fault time out capacitor.
4	4	C_{OSC}	Oscillator capacitor.
5	5	R_{OSC}	Oscillator resistor.
6	6	CTL	Pulse width control input.
7	7/8	NC	No connection.
8	9	V_{REG}	5V linear regulator.
9	10	I_{SENSE-}	Current sense minus.
10	11	I_{SENSE+}	Current sense plus.
11	12	I_{ADJ}	Current limit adjust.
12	13	INH	Output Inhibit.
13	14	PGnd	Power ground for on chip clamp.
	15	NC	No connection
14	16	V_{CC}	Positive power supply input.

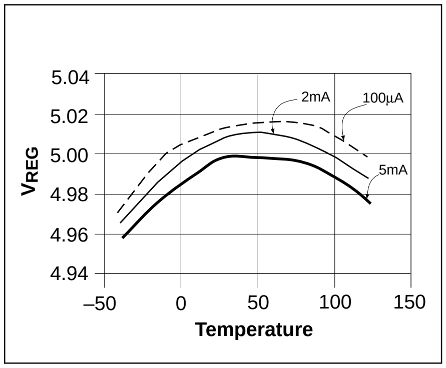
Block Diagram



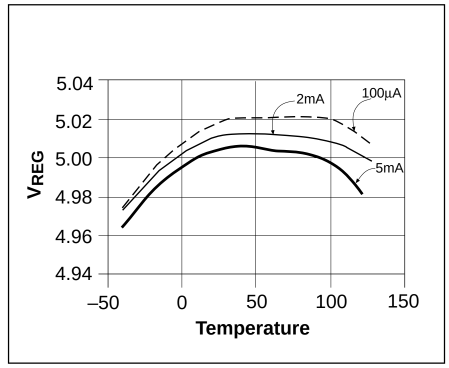
Typical Performance Characteristics



V_{REG} vs. Temperature @ V_{CC} = 8V



V_{REG} vs. Temperature @ V_{CC} = 12V



V_{REG} vs. Temperature @ V_{CC} = 16V

Application Information

Theory Of Operation

Oscillator

The IC sets up a constant frequency triangle wave at the C_{OSC} lead whose frequency is determined by the external components R_{OSC} and C_{OSC} by the following equation:

$$\text{Frequency} = \frac{0.83}{R_{OSC} \times C_{OSC}}$$

The peak and valley of the triangle wave are proportional to V_{CC} by the following:

$$V_{VALLEY} = 0.2 \times V_{CC}$$

$$V_{PEAK} = 0.8 \times V_{CC}$$

This is required to make the voltage compensation function properly. In order to keep the frequency of the oscillator constant the current that charges C_{OSC} must also vary with supply. R_{OSC} sets up the current which charges C_{OSC}. The voltage across R_{OSC} is 50% of V_{CC} and therefore:

$$I_{ROSC} = 0.5 \times \frac{V_{CC}}{R_{OSC}}$$

I_{ROSC} is multiplied by two (2) internally and transferred to the C_{OSC} lead. Therefore:

$$I_{COSC} = \pm \frac{V_{CC}}{R_{OSC}}$$

The period of the oscillator is:

$$T = 2C_{OSC} \times \frac{(V_{PEAK} - V_{VALLEY})}{I_{COSC}}$$

The R_{OSC} and C_{OSC} components can be varied to create frequencies over the range of 15Hz to 25kHz. With the suggested values of 105kΩ and 390pF for R_{OSC} and C_{OSC} respectively, the nominal frequency will be approximately 20 kHz. I_{ROSC}, at V_{CC} = 14V, will be 66.7 µA. I_{ROSC} should not change over a more than 2:1 ratio and therefore C_{OSC} should be changed to adjust the oscillator frequency.

Voltage Duty Cycle Conversion

The IC translates an input voltage at the CTL lead into a duty cycle at the OUTPUT lead. The transfer function incorporates ON Semiconductor’s patented Voltage Compensation method to keep the average voltage and current across the load constant regardless of fluctuations in the supply voltage. The duty cycle is varied based upon the input voltage and supply voltage by the following equation:

$$\text{Duty Cycle} = 100\% \times \frac{2.8 \times V_{CTL}}{V_{CC}}$$

An internal DC voltage equal to:

$$V_{DC} = (1.683 \times V_{CTL}) + (V_{VALLEY})$$

is compared to the oscillator voltage to produce the compensated duty cycle. The transfer is set up so that at V_{CC} = 14V the duty will equal V_{CTL} divided by V_{REG}. For example at V_{CC} = 14V, V_{REG} = 5V and V_{CTL} = 2.5V, the duty cycle would be 50% at the output. This would place a 7V average voltage across the load. If V_{CC} then drops to 10V, the IC would change the duty cycle to 70% and hence keep the average load voltage at 7V.

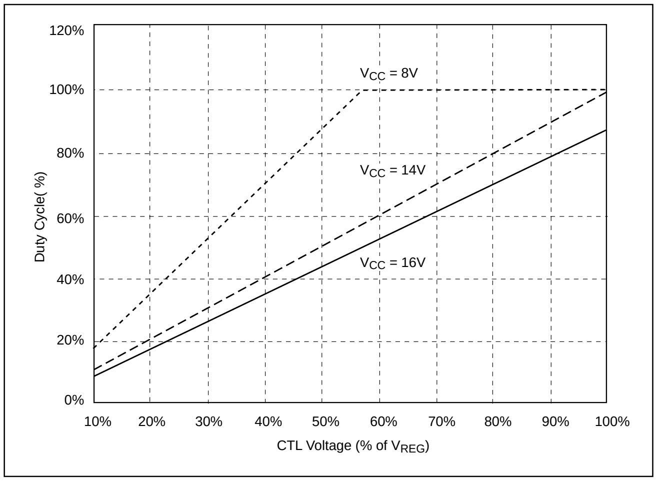


Figure 1: Voltage Compensation

5V Linear Regulator

There is a 5V, 5mA linear regulator available at the V_{REG} lead for external use. This voltage acts as a reference for many internal and external functions. It has a drop out of approximately 1.5V at room temperature and does not require an external capacitor for stability.

Current Sense and Timer

The IC differentially monitors the load current on a cycle by cycle basis at the I_{SENSE+} and I_{SENSE-} leads. The differential voltage across these two leads is amplified internally and compared to the voltage at the I_{ADJ} lead. The gain, A_V, is set internally and externally by the following equation:

$$A_V = \frac{V_{I(ADJ)}}{I_{SENSE+} - I_{SENSE-}} = \frac{37000}{1000 + R_{CS}}$$

The current limit (I_{LIM}) is set by the external current sense resistor (R_{SENSE}) placed across the I_{SENSE+} and I_{SENSE-} terminals and the voltage at the I_{ADJ} lead.

$$I_{LIM} = \frac{(1000 + R_{CS})}{37000} \times \frac{V_{I(ADJ)}}{R_{SENSE}}$$

The R_{CS} resistors and C_{CS} components form a differential low pass filter which filters out high frequency noise generated by the switching of the external MOSFET and the associated lead noise. R_{CS} also forms an error term in the gain of the I_{LIM} equation because the I_{SENSE+} and I_{SENSE-} leads are low impedance inputs thereby creating a good current sensing amplifier. Both leads source 50µA while the chip is in run mode. R_{CS} should be much less than 1000Ω to minimize error in the I_{LIM} equation. I_{ADJ} should be biased between 1V and 4V.

When the current through the external MOSFET exceeds I_{LIM}, an internal latch is set and the output pulls the gate of the MOSFET low for the remainder of the oscillator cycle (fault mode). At the start of the next cycle, the latch is reset and the IC reverts back to run mode until another fault occurs. If a number of faults occur in a given period of time, the IC "times out" and disables the MOSFET for a long period of time to let it cool off. This is accomplished by charging the C_{FLT} capacitor each time an over current condition occurs. If a cycle goes by with no overcurrent fault occurring, an even smaller amount of charge will be removed from C_{FLT}. If enough faults occur together, eventually C_{FLT} will charge up to 2.4V and the fault latch will be set. The fault latch will not be reset until the C_{FLT} discharges to 0.6V. This action will continue indefinitely if the fault persists.

The off time and on time are set by the following:

$$\text{Off Time} = C_{FLT} \times \frac{2.4V - 0.6V}{4.5\mu A}$$

$$\text{On Time} = C_{FLT} \times \frac{2.4V - 0.6V}{I_{AVG}}$$

where:

$$I_{AVG} = (295.5\mu A \times DC) - [4.5\mu A \times (1 - DC)]$$

$$I_{AVG} = (300\mu A \times DC) - 4.5\mu A$$

$$DC = \text{PWM Duty Cycle}$$

Sleep State

This device will enter into a low current mode (< 275µA) when CTL lead is brought to less than 0.5V. All functions are disabled in this mode, except for the regulator.

Inhibit

When the inhibit voltage is greater than 2.5V the internal latch is set and the external MOSFET will be turned off for the remainder of the oscillator cycle. The latch is then reset at the start of the next cycle.

Overvoltage Shutdown

The IC will disable the output during an overvoltage event. This is a real time fault event and does not set the internal latch and therefore is independent of the oscillator timing (i.e. asynchronous). There is no undervoltage lockout. The device will shutdown gracefully once it runs out of headroom. This happens at the point when V_{REG} falls out of regulation.

Reverse Battery

The CS7054 will not survive a reverse battery condition. Therefore, a series diode is required between the battery and the V_{CC} lead.

Load Dump

V_{CC} is internally clamped to 30V. It is recommended that a 51Ω resistor, (R_S) is placed in series with V_{CC} to limit the current flow into the IC in the event of a 40V peak transient condition.

Application Information: continued

Additional Application Diagram

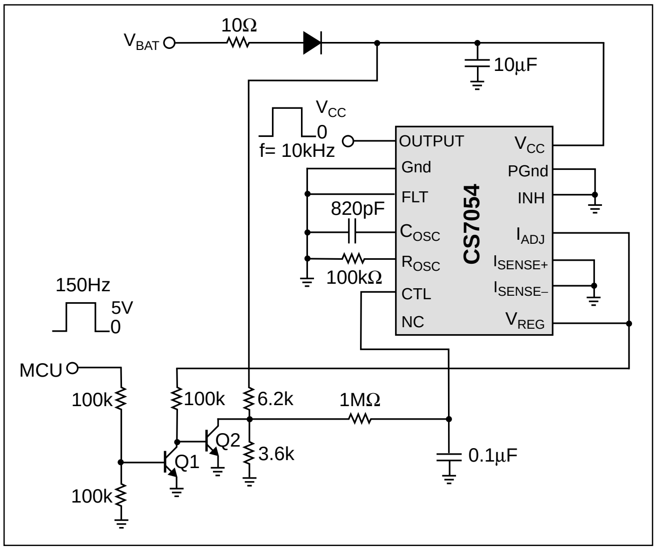


Figure 2: Frequency Converter

Figure 2 shows the CS7054 configured for the use as a frequency converter. In the setup shown, a 150Hz square wave from a microprocessor is converted to a 10kHz square wave. The duty cycle of each waveform is identical.

The amplitude of the input waveform is 5V, but does not need to be. The input amplitude requirement just needs to be high enough to switch the external bipolar transistor. The 10kHz oscillator frequency is setup per the oscillator section of this data sheet.

The external resistor divider composed of the 3.6k and 6.2k resistors supplies 5V to the CTL pin when the input duty cycle is at 100%. This also makes the output waveform 100%.

The RC filter (1MΩ and 0.1μF) sets up a pole at 1.6Hz:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi\left[1M\Omega + \left(\frac{(6.2k)(3.6k)}{6.2k + 3.6k}\right)\right](0.1\mu F)}$$

$$= 1.6Hz$$

In this case, the pole is 2 orders of magnitude below the input waveform. Care must be taken to provide the appropiate DC lvel on the control pin in addition to providing the required response time.

*Note the current limit feature of the CS7054 has been defeated by grounding the I_{SENSE+} and the I_{SENSE-} pins and connecting the I_{ADJ} lead to V_{REG}.

Package Specification

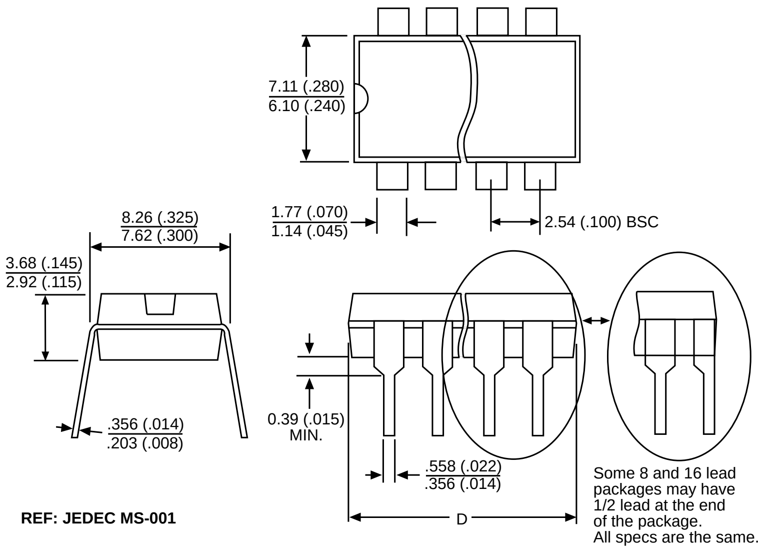
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
14 Lead PDIP	19.69	18.67	.775	.735
16 Lead SO Wide	10.50	10.10	.413	.398

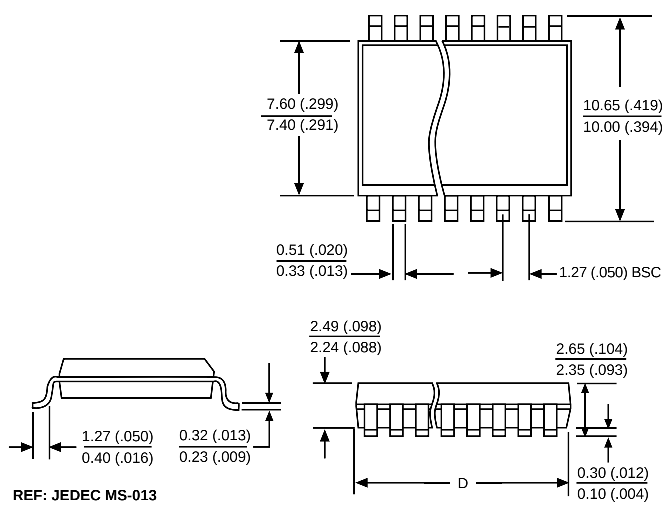
PACKAGE THERMAL DATA

Thermal Data		14 Lead PDIP	16 Lead SO Wide	
$R_{\Theta JC}$	typ	48	23	°C/W
$R_{\Theta JA}$	typ	85	105	°C/W

Plastic DIP (N); 300 mil wide



Surface Mount Wide Body (DW); 300 mil wide



Ordering Information

Part Number	Description
CS7054YN14	14 Lead PDIP
CS7054YDW16	16 Lead SO Wide
CS7054YDWR16	16 Lead SO Wide (tape & reel)

ON Semiconductor and the ON Logo are trademarks of Semiconductor Components Industries, LLC (SCILLC). ON Semiconductor reserves the right to make changes without further notice to any products herein. For additional information and the latest available information, please contact your local ON Semiconductor representative.

Notes