CS5651

High Performance Dual Channel Current Mode Controller with ENABLE

Description

The CS5651 is a high performance, fixed frequency, dual current mode controller specifically designed for Off-Line and DC to DC converter applications. It offers the designer a cost effective solution with minimal external components. This integrated circuit features a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, and two high current totem pole outputs ideally suited for driving power MOSFETs. One of the outputs, V_{OUT_2} is switchable via the $ENABLE_2$ pin.

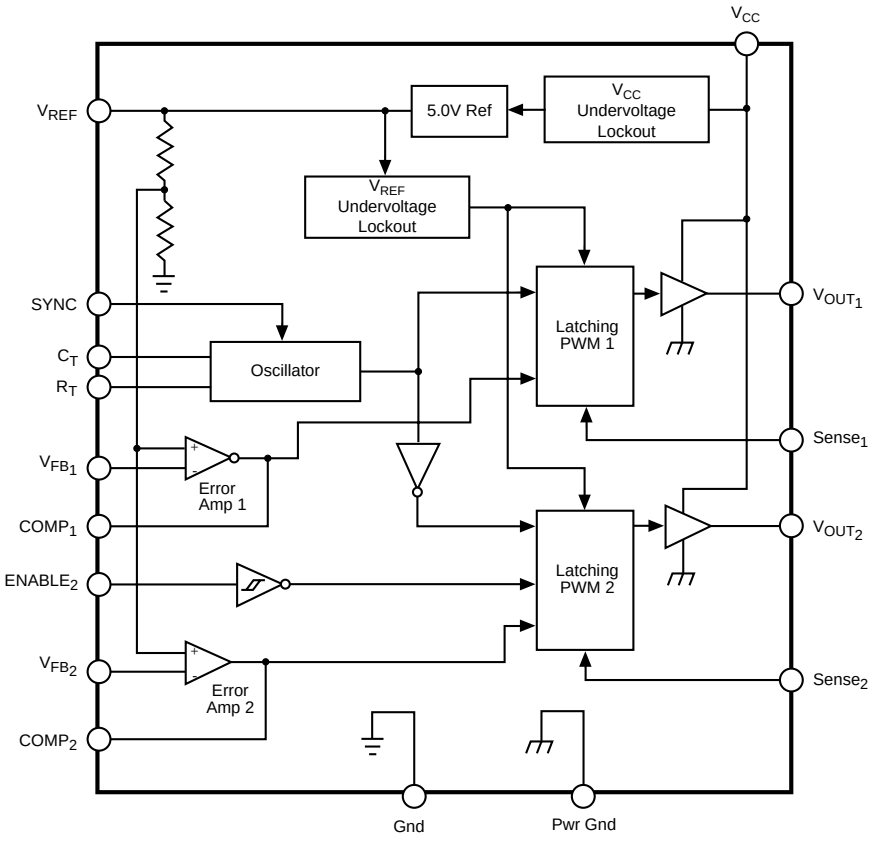
Also included are protective features consisting of input and reference undervoltage lockouts, each with hysteresis; cycle-by-cycle current limiting; and a latch for single pulse metering of each output.

The CS5651 is pin compatible with the MC34065H.

Features

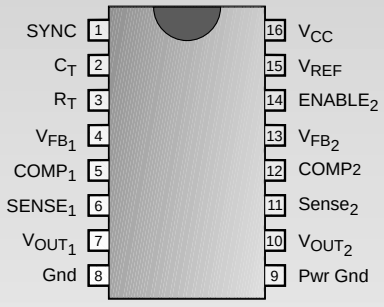
- **Oscillator has Precise Duty Cycle Limit and Frequency Control**
- **500kHz Current Mode Operation**
- **Automatic Feed Forward Compensation**
- **Separate Latching PWMs for Cycle-By-Cycle Current Limiting**
- **Internally Trimmed Reference with Undervoltage Lockout**
- **Switchable Second Output**
- **Two High Current Totem Pole Outputs**
- **Input Undervoltage Lockout with Hysteresis**

Block Diagram



Package Options

16L PDIP & SO Wide



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Absolute Maximum Ratings

Output Current, Source or Sink (Note 1) 400mA
Output Energy (capacitive load per cycle) 5.0µJ
Current Sense, Enable and Voltage ..... -0.3 to +5.5V
Feedback Inputs
Sync Input
High State (Voltage) 5.5V
Low State (Reverse Current) ..... -5.0mA
Error Amp Output Sink Current 10mA
Storage Temperature Range ..... -65 to +150°C
Operating Junction Temperature ..... +150°C
Lead Temperature Soldering
Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak
Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: V_{CC} = 15V, R_T = 8.2kΩ, C_T = 3.3nF, 0°C ≤ T_A ≤ 70°C [Note 2], unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Reference Section					
Reference Output Voltage, V_{REF}	I_{OUT} = 1.0mA, T_J = 25°C	4.9	5.0	5.1	V
Line Regulation	11V ≤ V_{CC} ≤ 15V		2.0	20.0	mV
Load Regulation	1.0mA ≤ I_{OUT} ≤ 10mA		3.0	25.0	mV
Total Output Variation over Line, Load and Temperature		4.85		5.15	V
Output Short Circuit Current		30	100		mA
■ Oscillator and PWM Sections					
Total Frequency Variation over Line and Temperature	11V ≤ V_{CC} ≤ 15V, T_{low} ≤ T_A ≤ T_{high}	46.5	49.0	51.5	kHz
Frequency Change with Voltage	11V ≤ V_{CC} ≤ 15V		0.2	1.0	%
Duty Cycle at each Output	Maximum	46.0	49.5	52.0	%
SYNC Current	High State V_{IN} = 2.4V Low State V_{IN} = 0.8V		170 80	250 160	µA
■ Error Amplifiers					
Voltage Feedback Input	V_{OUT} = 2.5V	2.42	2.50	2.58	V
Input Bias Current	V_{FB} = 5.0V		-0.1	-1.0	µA
Open-Loop Voltage Gain	2.0V ≤ V_{OUT} ≤ 4.0V	65	100		dB
Unity Gain Bandwidth	T_J = 25°C (Note 5)	0.7	1.0		MHz
Power Supply Rejection Ratio	V_{CC} = 11V to 15V	60	90		dB
Output Current	Source V_{OUT} = 3.0V, V_{FB} = 2.3V Sink V_{OUT} = 1.2V, V_{FB} = 2.7V	-0.45 2.00	-1.00 12.00		mA mA
Output Voltage Swing	High State R_L = 15kΩ to ground, V_{FB} = 2.3V Low State R_L = 15kΩ to V_{REF}, V_{FB} = 2.7V	5.0	6.2 0.8	 1.1	V V

Electrical Characteristics: V_{CC} = 15V, R_T = 8.2kΩ, C_T = 3.3nF, 0°C ≤ T_A ≤ 70°C [Note 2], unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Current Sense Section					
Current Sense Input Voltage Gain	(Notes 3 and 4)	2.75	3.00	3.25	V/V
Maximum Current Sense Input Threshold	(Note 3)	0.9	1.0	1.1	V
Input Bias Current			-2.0	-30.0	µA
Propagation Delay	Current Sense Input to Output (Note 5)		150	300	ns
■ Output 2 Enable Pin					
Enable Pin Voltage					V
High State	$ENABLE_2$ enabled	3.5		V_{REF}	V
Low State	$ENABLE_2$ disabled	0.0		1.5	V
Low State Input Current	V_{IL} = 0V	100	250	400	µA
■ Drive Outputs					
Output Voltage					
Low State	I_{SINK} = 20mA		0.1	0.4	V
	I_{SINK} = 200mA		1.6	2.5	V
High State	I_{SOURCE} = 20mA	13.0	13.5		V
	I_{SOURCE} = 200mA	12.0	13.4		V
Output Voltage with UVLO Activated	V_{CC} = 6.0V, I_{SINK} = 1.0mA		0.1	1.1	V
Output Voltage Rise Time	C_L = 1.0nF (Note 5)		28	150	ns
Output Voltage Fall Time	C_L = 1.0nF (Note 5)		25	150	ns
■ Undervoltage Lockout Section					
Start-Up Threshold		13	14	15	V
Minimum Operating Voltage		9.0	10.0	11.0	V
Hysteresis			4.0		V
■ Total Device					
Start-Up Current	V_{CC} = 12V		0.6	1.0	mA
Operating Current	(Note 2)		20	25	mA

Note 1: Maximum package power dissipation limits must be observed.

Note 2: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Note 3: This parameter is measured at latch trip point with V_{FB} = 0V.

Note 4: Comparator gain is defined as:

$$AV = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$$

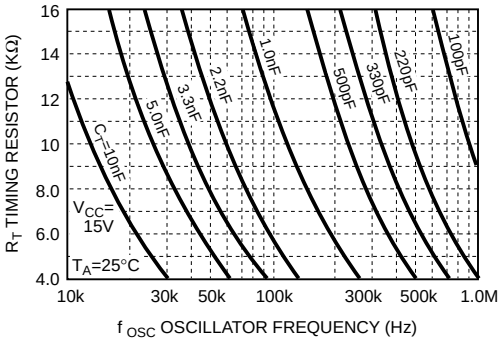
Note 5: These parameters are guaranteed by design but not 100% tested in production.

Package Pin Description

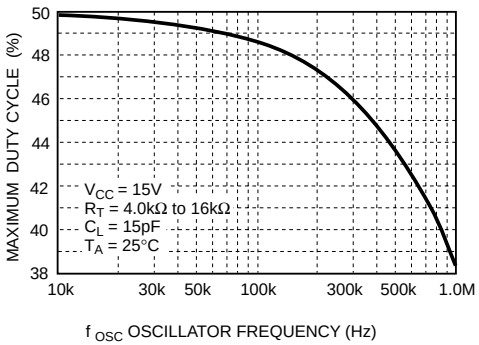
PACKAGE PIN #	PIN SYMBOL	FUNCTION
16 L PDIP & SO Wide		
1	SYNC	A positive going pulse applied to this input will synchronize the oscillator. A DC voltage within the range of 2.4V to 5.5V will inhibit the oscillator.
2	C_T	Timing capacitor C_T connects pin to ground setting oscillator frequency.
3	R_T	Resistor R_T connects to ground setting the charge current for C_T. Its value must be between 4.0kΩ and 16kΩ.
4	V_{FB_1}	The inverting input of error amplifier 1. Normally it is connected to the switching power supply output.
5	$COMP_1$	The output of error amplifier 1, for loop compensation.
6	$Sense_1$	Output 1 pulse by pulse current limit.
7	V_{OUT_1}	Drives the power switch at output 1.
8	Gnd	Logic ground
9	Pwr Gnd	Power ground. Power device return is connected to this pin.
10	V_{OUT_2}	Drives the power switch at output 2.
11	$Sense_2$	Output 2 pulse by pulse current limit.
12	$COMP_2$	Output of error amplifier 2, for loop compensation.
13	V_{FB_2}	Inverting input of error amplifier 2. Normally it is connected to the switching power supply output.
14	$ENABLE_2$	Output 2 disable. A logic low at this pin disables V_{OUT_2}.
15	V_{REF}	5.0V reference output. It can source current in excess of 30mA.
16	V_{CC}	The positive supply of the IC. The minimum operating voltage range after start-up is 9V.

Typical Performance Characteristics

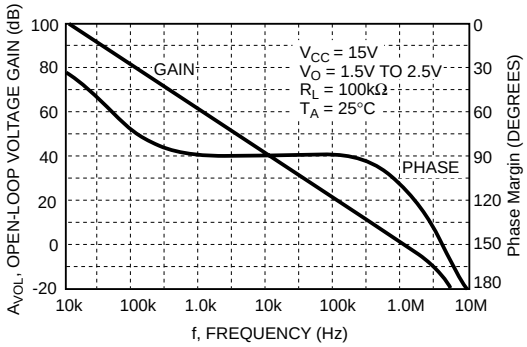
Timing Resistor vs. Oscillator Frequency



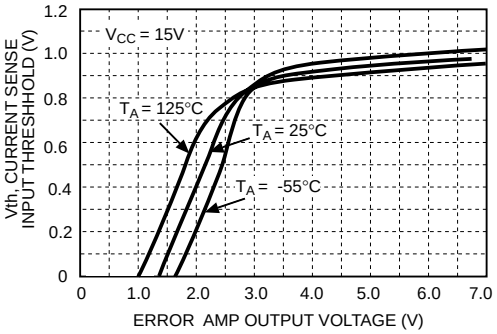
Max. Output Duty Cycle vs. Oscillator Frequency



Error Amp Open-Loop Gain & Phase vs. Frequency

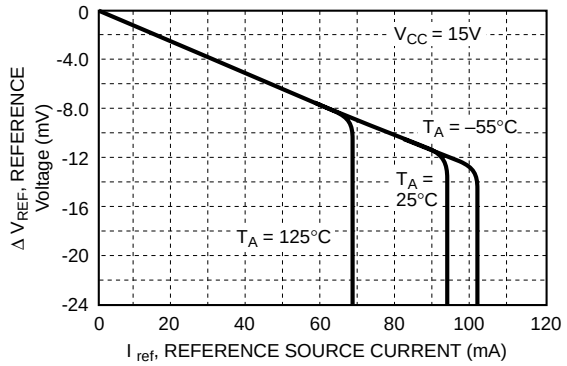


Current Sense Input Threshold vs. Error Amp Output Voltage

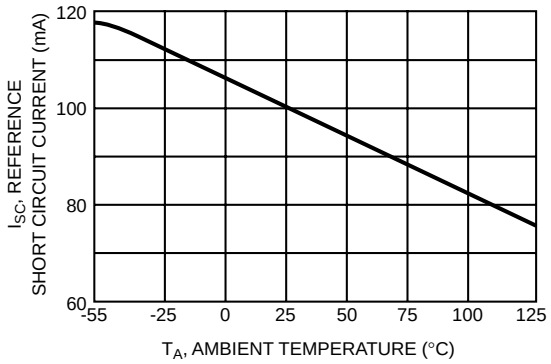


Typical Performance Characteristics: continued

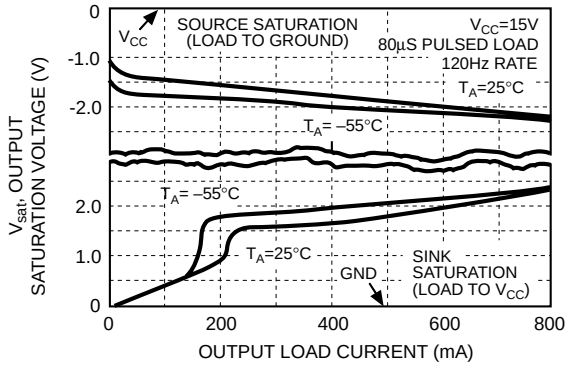
Reference Voltage Change vs. Source Current



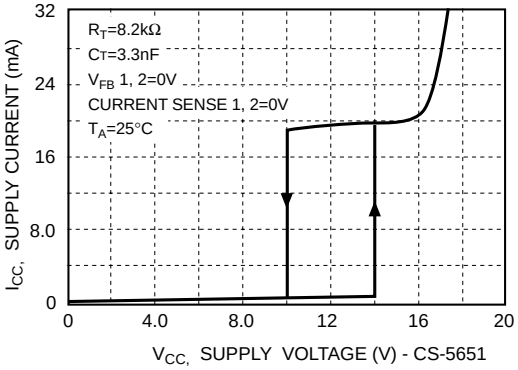
Reference Short Circuit Current vs. Temperature



Output Saturation Voltage vs. Load Current



Supply Current vs. Supply Voltage



Operating Description

The CS5651 is a high performance, fixed frequency, dual channel current mode PWM controller for Off-Line and DC to DC converter applications. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference, and undervoltage lockout circuits are common to both channels.

Oscillator

The oscillator has both precise frequency and duty cycle control. The oscillator frequency is programmed by the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, that generates a symmetrical 50 percent duty cycle waveform at C_T. The oscillator peak and valley thresholds are 3.5V and 1.6V respectively. The source / sink current is controlled by resistor R_T. For proper operation over temperature range R_T's value should be between 4.0kΩ to 16kΩ.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non-overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Even at 500kHz, each output is capable of approximately 44% duty cycle, making this controller suitable for high frequency power conversion applications.

In noise sensitive applications it may be necessary to synchronize the converter with an external system clock. This can be accomplished by applying an external clock signal. For reliable synchronization, the oscillator frequency should be set about 10% slower than the clock frequency. The rising edge of the clock signal applied to SYNC, terminates the charging of C_T and V_{OUT_2} conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved.

Error Amplifier

Each channel contains a fully-compensated error amplifier with access to the output and inverting input. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71 degrees of phase margin. The non-inverting input is internally biased at 2.5V. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is -1.0 µA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider resistance.

Its output voltage is offset by two diode drops (≈1.4V) and divided by three before it connects to the inverting input of the current sense comparator. This guarantees that both

Operating Description: continued

outputs are disabled when the error amplifier output is at its lowest state ($V_{OUT(LOW)}$). This occurs when the power supply is operating at light or no-load conditions, or at the beginning of a soft-start interval.

The minimum allowable error amplifier feedback resistance is limited by the amplifier's source current capability (0.5 mA) and the output voltage ($V_{OUT(High)}$) required to reach the current sense comparator 1.0V clamp level with the error amplifier inverting input at ground. This condition happens during initial system start up or when the sensed output is shorted:

$$R_{F(min)} \approx \frac{(3 \times 1.0V) + 1.4V}{0.5mA} = 8.8k\Omega$$

Current Sense Comparator and PWM Latch

The CS5651 operates as a current mode controller. Output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the error amplifier output. The error signal controls the peak inductor current on a cycle-by-cycle basis. The current sense comparator-PWM Latch combination ensures that only a single pulse appears at the output during any given oscillator cycle. The current is converted to a voltage by connecting sense resistor R_{Sense} in series with the source of output switch Q1 and ground. This voltage is monitored via the $Sense_{1,2}$ pins and compared to a voltage derived from the error amp output. The peak current under normal operating conditions is controlled by the voltage at COMP where:

$$I_{pk} = \frac{V_{COMP} - 1.4V}{3R_{Sense}}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage is too high. Under these conditions, the current sense comparator threshold will be internally clamped to 1.0V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0V}{R_{Sense}}$$

Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. The addition of an RC filter on the current sense input reduces this spike to an acceptable level.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. V_{CC} and the reference output V_{REF} are monitored by separate comparators. Each comparator has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14V and 10V for the CS5651. The V_{REF} comparator disables the outputs until the internal circuitry is functional. This comparator has upper and lower thresholds of 3.6V and 3.4V. The guaranteed minimum operating voltage after turn-on is 11V for CS5651.

Outputs and Power Ground

Each channel contains a single totem-pole output stage specifically designed for driving a power MOSFET. The outputs have up to ±1.0A peak current capability and have a typical rise and fall time of 28ns with a 1.0nF load. Internal circuitry has been added to keep the outputs in active pull-down mode whenever undervoltage lockout is active. An external pull-down resistor is not needed.

Cross-conduction current in the totem-pole output stage has been minimized for high speed operation. The average added power due to cross-conduction with V_{CC} = 15V is only 60mW at 500kHz.

Although the outputs were optimized for MOSFET's, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn-off. Because the outputs do not contain internal current limiting circuitry, an external series resistor may be required to prevent the peak output current from exceeding the ±1.0A maximum rating. The sink saturation voltage (V_{OL}) is less than 0.4V at 100mA.

A separate Power Ground pin is provided and will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly important when the $I_{pk(max)}$ clamp level is reduced.

$ENABLE_2$

This input is used to switch V_{OUT_2}. V_{OUT_1} can be used to control circuitry that runs continuously; e.g. volatile memory, the system clock, or a remote controlled receiver. The V_{OUT_2} output can control the high power circuitry that can be turned off when not needed.

Voltage Reference

The 5.0V bandgap reference is trimmed to ±2.0% tolerance. The reference has short circuit protection and is capable of sourcing 30mA for powering any additional external circuitry.

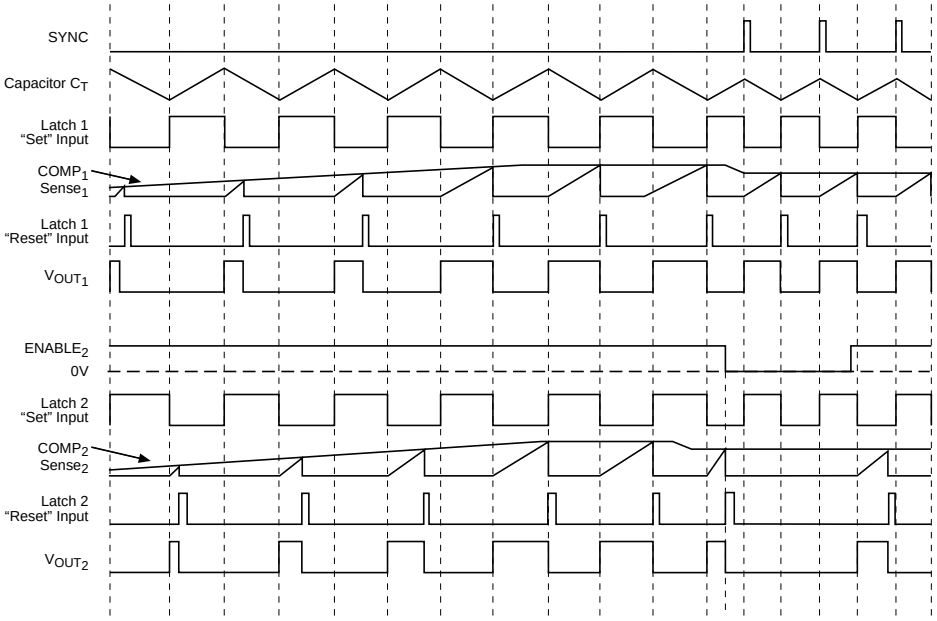
Design Considerations

High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the current sense or voltage feed-back inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit board layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input fil-

Operating Description: continued

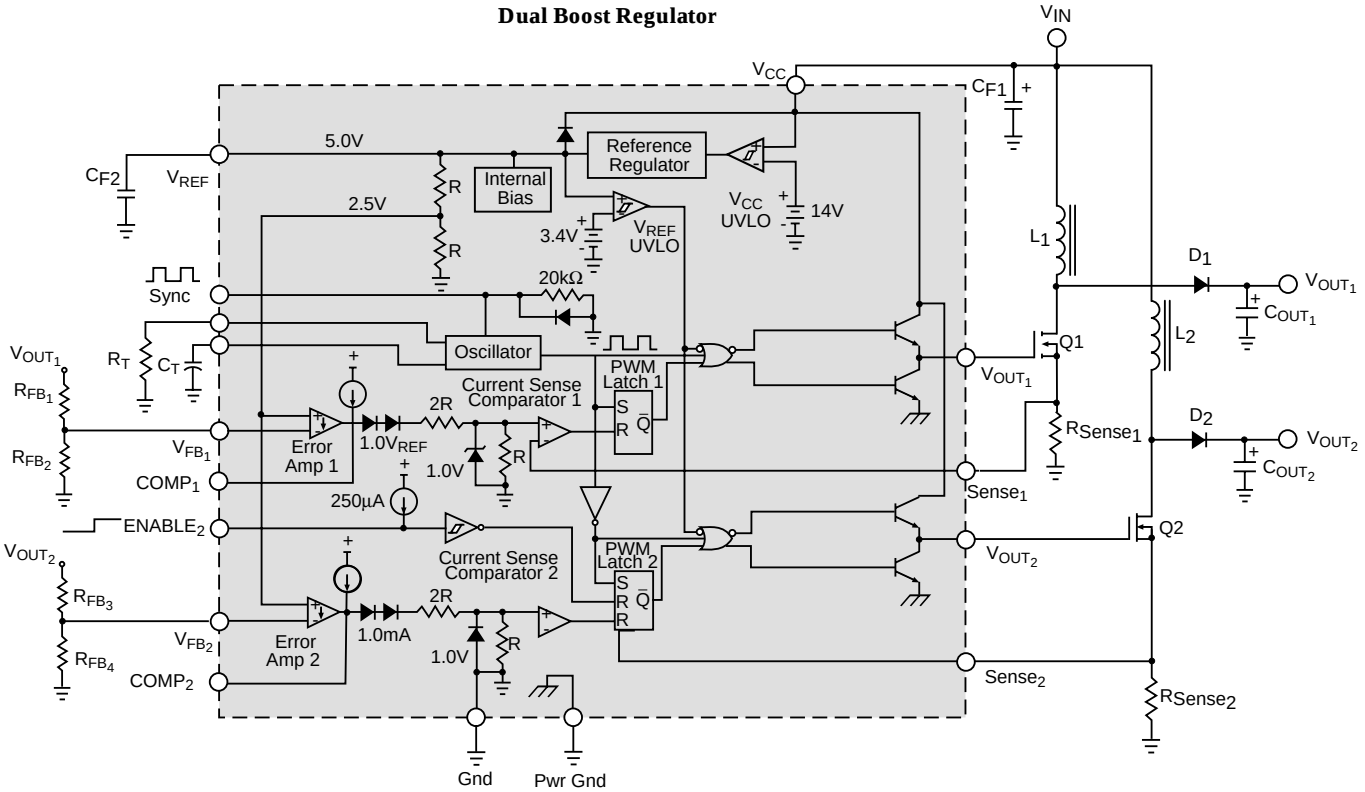
ter capacitor. Ceramic bypass capacitors (0.1µF) connected directly to V_{CC} and V_{REF} may be required to improve noise filtering. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs. The error amp compensation circuitry and the converter output voltage-divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Timing Diagram



Typical Application Diagram

Dual Boost Regulator



Package Specification

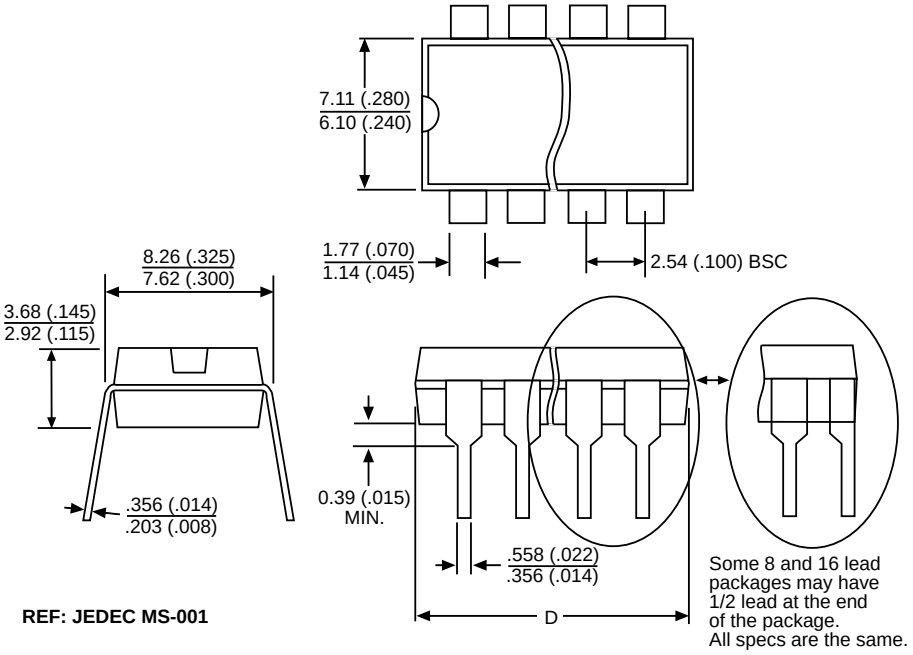
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16 Lead PDIP	19.69	18.67	.775	.735
16 Lead SO Wide	10.50	10.10	.413	.398

PACKAGE THERMAL DATA

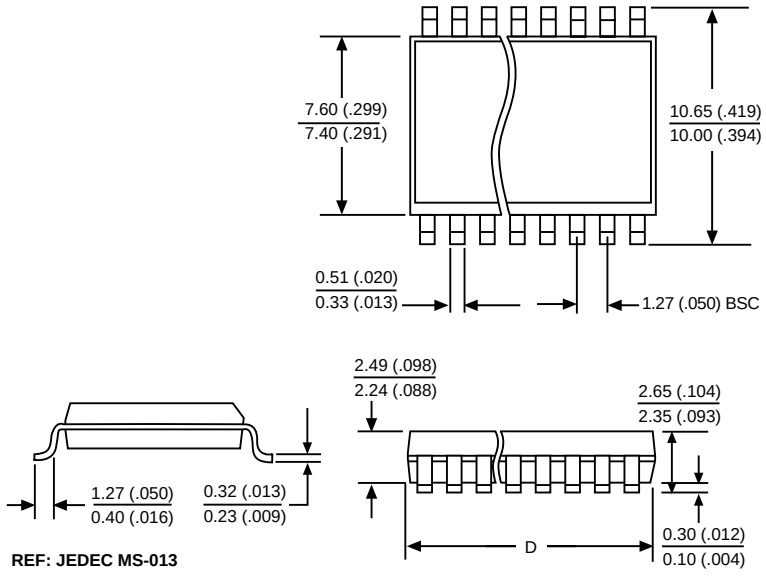
Thermal Data		16 Lead PDIP	16 Lead SO Wide	
$R_{\Theta JC}$	typ	42	23	°C / W
$R_{\Theta JA}$	typ	80	105	°C / W

Plastic DIP (N); 300 mil wide



REF: JEDEC MS-001

Surface Mount Wide Body (DW); 300 mil wide



REF: JEDEC MS-013

Ordering Information

Part Number	Description
CS5651GN16	16L PDIP
CS5651GDW16	16L SO Wide
CS5651GDWR16	16L SO Wide *(Tape & Reel)*