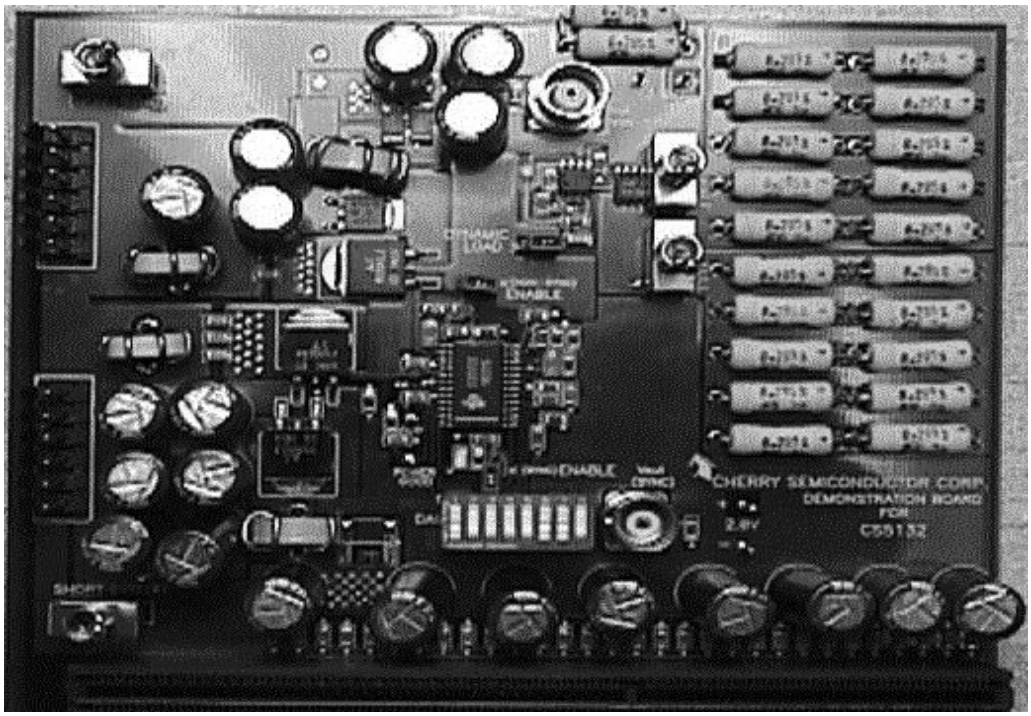
Dual Output CPU Buck Regulator (+2V/20A, +3.3V/8A) Based on the CS5132 Dual Output CPU Buck Controller

a CS5132 Demonstration Manual
08/26/98



November, 1998 - Rev. 0
CS5132DM

ON Semiconductor

Description

This demonstration board is a dual output CPU NFET buck regulator based on the CS5132 dual output controller. These synchronous and nonsynchronous buck regulators are designed to power the core and I/O logic of the latest high performance CPUs such as the Intel® Deschutes or AMD-K7™ processor . The CS5132 utilizes the V^{2}™ control method to achieve the fastest possible transient response and best overall regulation. The CS5132 demonstration board has input voltages of +5V, and +12V and they are provided by a standard AT computer power supply. +12V is the IC supply voltage, and +5V is the $V_{CC(CORE)}$ synchronous and $V_{I/O}$ nonsynchronous buck regulator supply voltage. The $V_{CC(CORE)}$ synchronous NFET buck regulator has a user-programmed 5-bit DAC output voltage, which at +2V/16A has a DC accuracy of ± 70mV and an AC accuracy of ± 100mV. The $V_{I/O}$ nonsynchronous NFET buck regulator regulator has a fixed output voltage of +3.3V/8A DC with a DC accuracy of ± 100mV and an AC accuracy of ± 135mV. The CS5132 demonstration board combines mixed-assembly technologies. The input and output inductors and capacitors are through-hole, while the remaining regulator components are SMT. The CS5132 demonstration board provides adjustable hiccup mode current limit and short-circuit protection through a discrete sense resistor that can also be implemented as an inexpensive embedded PCB trace. The only external component needed to implement hiccup mode overcurrent protection is the RC filter at the V_{FB} and V_{OUT} pins. The current sensing PCB trace is placed between the output choke and output capacitors. Once the voltage drop across this PCB trace exceeds the internal reference voltage of 86mV (typical), the CS5132 forces the buck regulator to go into hiccup mode. This protection scheme minimizes thermal stress to the regulator components, input power supply, and PC board traces. The current sensing resistor (discrete or embedded) is also used to implement Adaptive Voltage Positioning (AVP), which provides the benefit of improved headroom during load transient conditions. The total PCB trace variation is typically ±56%, compared to ±96% using the $R_{DS(ON)}$ current limit method. As seen the $V_{CC(CORE)}$ power supply section is located next to the 242-pin Slot 1 socket, where the Intel Slot 1 EMT Tool or ON Semiconductor's test card can be inserted.

Today's advanced processors such as the Intel® Deschutes or AMD-K7™ have the capability of shutting down unused sections of the CPU in order to conserve power. Furthermore, they provide a 5-bit DAC code to the CPU power supply, demanding that the voltage regulator delivers an output voltage corresponding to the DAC code. When power resumes to the unused sections of the CPU, current transients from the Stop-Grant state to the Normal Operating state can place a severe burden on the processor power supply which has to provide a regulated output voltage as quickly as possible. When current transients as high as 16A can occur the CS5132 demonstration board is able to provide regulation in a very short period of time due to ON's proprietary V^{2}™ control topology

The V^{2}™ feedback architecture makes use of the ramp signal developed across the ESR of the output capacitors. This ramp signal is fed back into the V_{FB} pins and it is driven into two feedback loops. The slow feedback loop consists of an error amplifier that is only responsible for setting the DC output voltage accuracy. The fast feedback loop involves the PWM comparator and logic gates. When current transients occur, the change in the ramp signal across the output capacitors is fed back through the V_{FB} pin, into the PWM comparator of the CS5132. This voltage feedback signal is only delayed by the PWM comparator and a minimal number of logic gates before the duty cycle of the external switching MOSFET is adjusted. As a result, the CS5132 demonstration board provides a tightly regulated output voltage to the CPU core.

This dual output buck regulator provides a highly integrated solution, minimizing external component count, size, and cost. Among the features are a Power-Good output, a dedicated Overvoltage Protection (OVP) pin , and regulator ON/OFF control through the COMP pins.

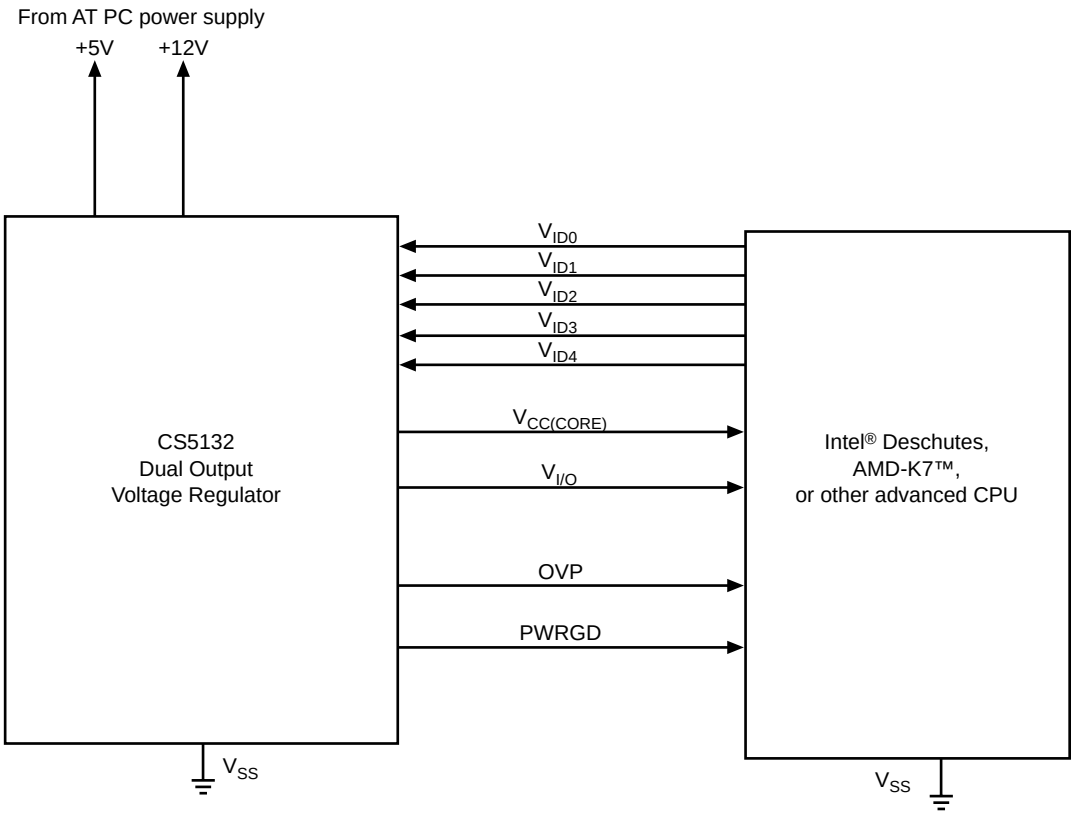
The CS5132 will operate over an 8.5V to 20V range and is available in a 24 lead surface mount package.

V^{2} is a trademark of Switch Power, Inc.
Intel is a registered trademark of Intel Corporation.
AMD-K7 is a trademark of Advanced Micro Devices, Inc.

Features

- Low External Component Count and Solution Cost for AT-based motherboard designs
- V^{2TM} Control Topology provides fast response to changes in both Line and Load
- Intel-specified PWRGD function
- 65ns Adaptive Non-Overlap Time between High and Low Side FET gate pulses
- Output Voltage programmable from 1.2V to 3.5V by 5-Bit logic level input
- Provides 16A for 500MHz Deschutes $V_{CC(CORE)}$, and 8A for 500MHz Deschutes $V_{I/O}$.
- 2% DC Regulation, 5% AC Regulation
- Dedicated Overvoltage Protection (OVP) pin provides overall system power supply control
- Synchronous Rectification for $V_{CC(CORE)}$ provides 90% Efficiency
- 1.2µH Output Inductor provides 6-8µs Response Time to a 16A Load Transient
- Adaptive Voltage Positioning improves AC Regulation and reduces response time during Load Transients
- Hiccup Mode Overcurrent Protection minimizes component stress
- Discrete sense resistor functions as a “Droop Resistor” and Current Sensing Element
- Dual logic-level N-Channel MOSFET Design - D^2PAK FS70VSJ-03
- 5V Supply Input and 12V Bias Input with 4.25V UVL
- On-board outputs can be exercised using resistive loads, electronic loads, or the Intel Slot1 EMT Tool
- Easy evaluation of DC and AC performance, Hiccup Mode Short-Circuit Protection and Current Limit
- OVP and PWRGD signals available for monitoring

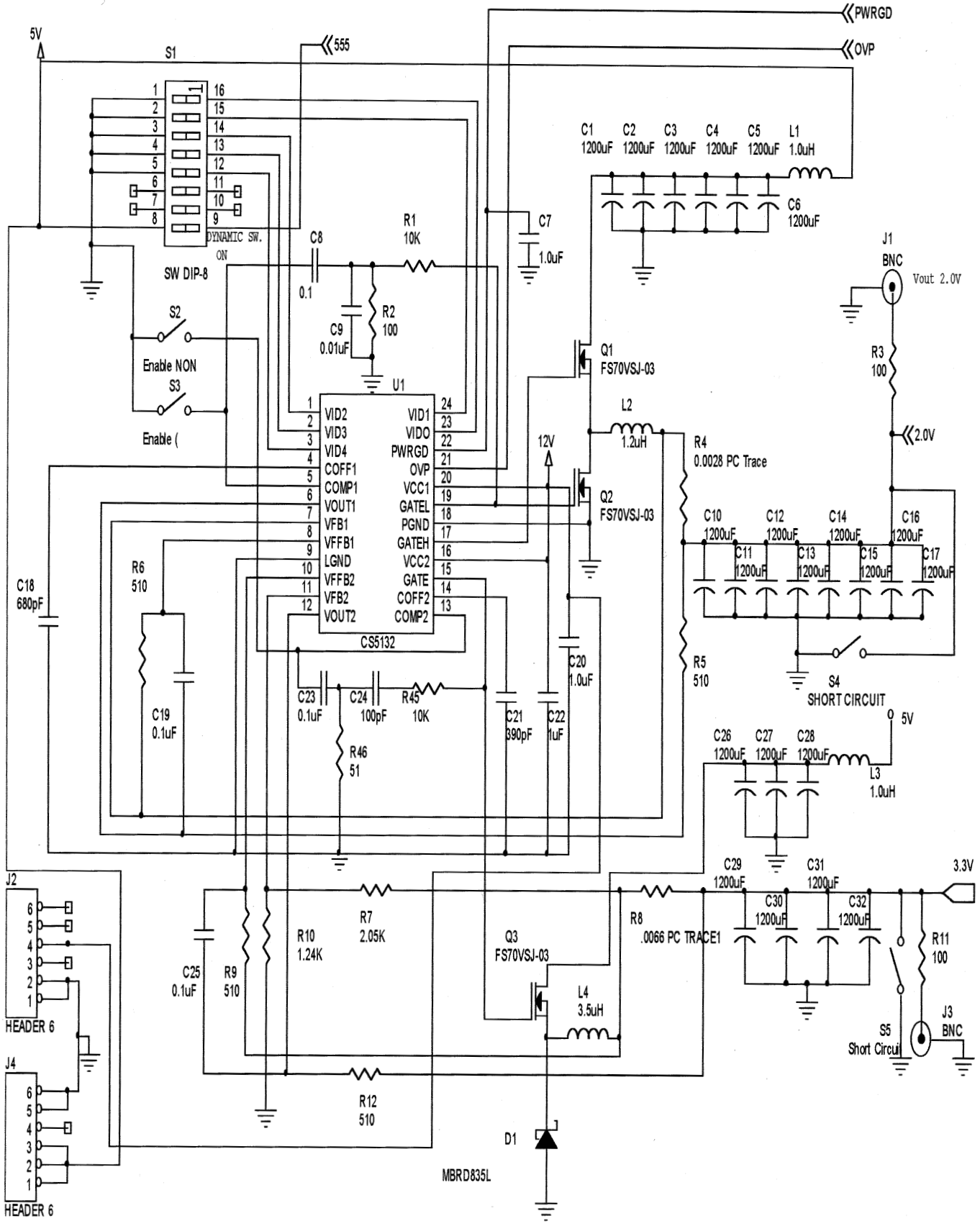
Application Diagram

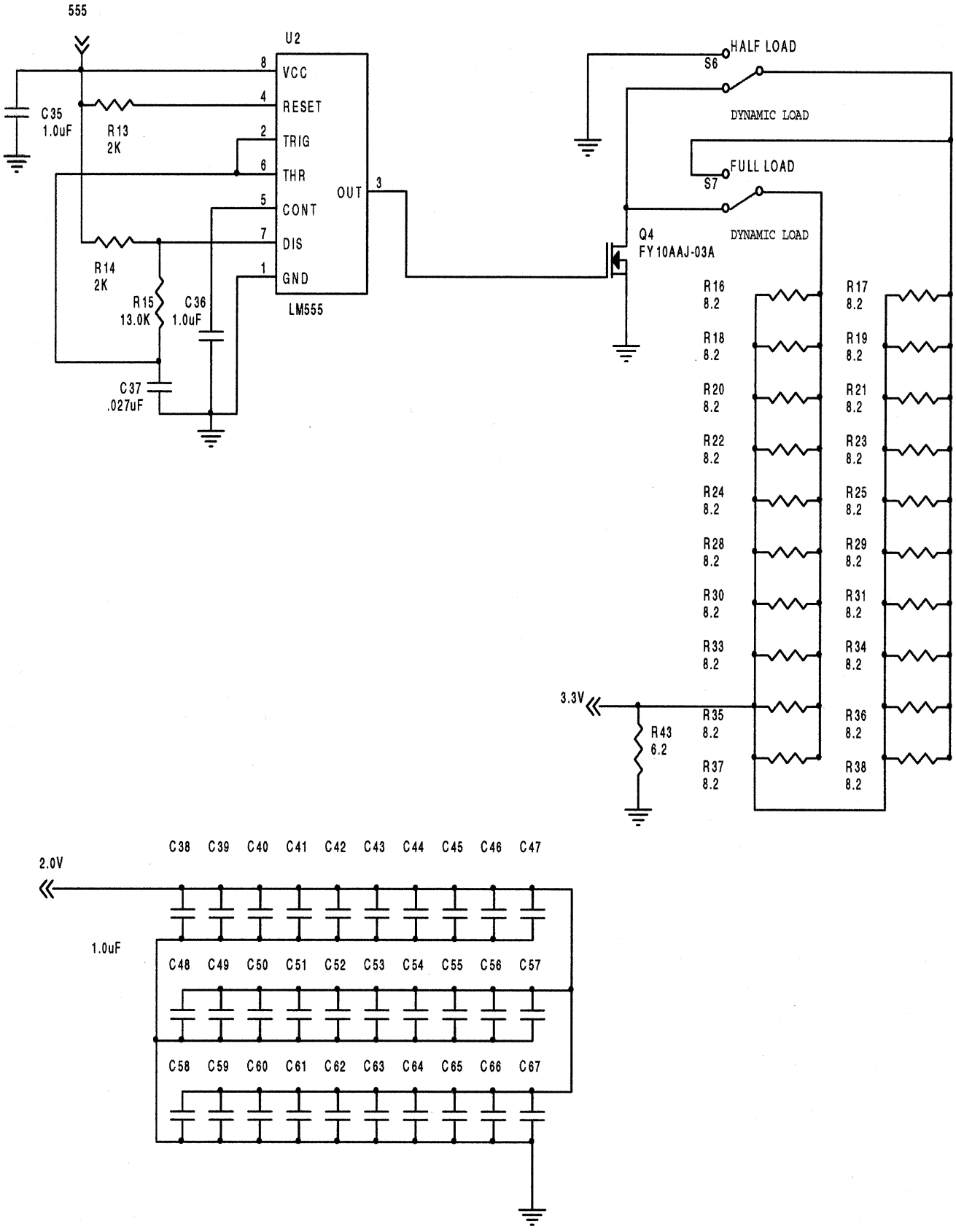


$V_{CC(CORE)}$ Output Voltage vs VID (Voltage Identification Code)

T_A = +25°C, $5V_{IN}$ = 5V, $12V_{IN}$ = 12V, 0A < I_{OUT} < 16A, 2% DC accuracy								
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	MIN	TYP	MAX	UNITS
0	1	1	1	1	1.2985	1.325	1.3515	V
0	1	1	1	0	1.3475	1.375	1.4025	V
0	1	1	0	1	1.3965	1.425	1.4535	V
0	1	1	0	0	1.4455	1.475	1.5045	V
0	1	0	1	1	1.4945	1.525	1.5555	V
0	1	0	1	0	1.5435	1.575	1.6065	V
0	1	0	0	1	1.5925	1.625	1.6575	V
0	1	0	0	0	1.6415	1.675	1.7085	V
0	0	1	1	1	1.6905	1.725	1.7595	V
0	0	1	1	0	1.7395	1.775	1.8105	V
0	0	1	0	1	1.7885	1.825	1.8615	V
0	0	1	0	0	1.8375	1.875	1.9125	V
0	0	0	1	1	1.8865	1.925	1.9635	V
0	0	0	1	0	1.9355	1.975	2.0145	V
0	0	0	0	1	1.9845	2.025	2.0655	V
0	0	0	0	0	2.0335	2.075	2.1165	V
1	1	1	1	1	1.2210	1.246	1.2709	V
1	1	1	1	0	2.0825	2.125	2.1675	V
1	1	1	0	1	2.1805	2.225	2.2695	V
1	1	1	0	0	2.2785	2.325	2.3715	V
1	1	0	1	1	2.3765	2.425	2.4735	V
1	1	0	1	0	2.4745	2.525	2.5755	V
1	1	0	0	1	2.5725	2.625	2.6775	V
1	1	0	0	0	2.6705	2.725	2.7795	V
1	0	1	1	1	2.7685	2.825	2.8815	V
1	0	1	1	0	2.8665	2.925	2.9835	V
1	0	1	0	1	2.9645	3.025	3.0855	V
1	0	1	0	0	3.0625	3.125	3.1875	V
1	0	0	1	1	3.1605	3.225	3.2895	V
1	0	0	1	0	3.2585	3.325	3.3915	V
1	0	0	0	1	3.3565	3.425	3.4935	V
1	0	0	0	0	3.4545	3.525	3.5955	V

Demonstration Board Schematic




555
U2
8
VCC
4
RESET
2
TRIG
6
THR
5
CONT
7
DIS
1
GND
OUT
3
LM555
C35
1.0uF
R13
2K
R14
2K
R15
13.0K
C36
1.0uF
C37
.027uF
HALF LOAD
S6
DYNAMIC LOAD
FULL LOAD
S7
DYNAMIC LOAD
Q4
FY10AAJ-03A
R16 8.2
R17 8.2
R18 8.2
R19 8.2
R20 8.2
R21 8.2
R22 8.2
R23 8.2
R24 8.2
R25 8.2
R28 8.2
R29 8.2
R30 8.2
R31 8.2
R33 8.2
R34 8.2
R35 8.2
R36 8.2
R37 8.2
R38 8.2
3.3V
R43
6.2
2.0V
1.0uF
C38 C39 C40 C41 C42 C43 C44 C45 C46 C47
C48 C49 C50 C51 C52 C53 C54 C55 C56 C57
C58 C59 C60 C61 C62 C63 C64 C65 C66 C67

Demonstration Board Operation Guidelines

The CS5132 Demonstration Board is configured to demonstrate all the performance features and benefits of the CS5132 dual buck controller IC with V^{2}™ technology.

- The power supply input connectors *J2* and *J4* are the straight friction lock header type (Molex) and they are located on the left-hand side of the board top layer.
- The power supply used is a computer AT form factor 250W "silver box" type.

$V_{CC(CORE)}$ Output

- The $V_{CC(CORE)}$ voltage output terminal *J1* is a female BNC connector, located on the bottom side of the board top layer near the bulk output capacitors. Using a standard BNC coax cable, the output voltage waveform can be observed on an oscilloscope during DC and AC load operation.
- The $V_{CC(CORE)}$ voltage output terminals *TP3* and *TP4* are gold pins located next to *J1*. An external electronic or resistive load can be connected to these terminals.
- The on-board 242-pin AMP Slot1 socket accepts the Intel Slot1 EMT Tool or ON Semiconductor's test card.
- Using the Intel-provided software, $V_{CC(CORE)}$ can be exercised in AC and DC conditions. The AC test conditions are user-programmable. Refer to Intel's Slot1 EMT Tool User's Guide for instructions.
- Using ON Semiconductor's test card $V_{CC(CORE)}$ can be exercised in AC and DC conditions. The AC and DC test conditions are fixed (0-16A load pulse), 8A DC half load, and 16A DC full load.
- *Current Limit* on $V_{CC(CORE)}$ can be tested by connecting an electronic load at the $V_{CC(CORE)}$ terminals *TP3* and *TP4* and then increasing the load current until the CS5132 goes into "hiccup" mode.
- The *Short Circuit Switch S4* is a SPDT type (AMP) and is located near the Slot 1 socket. By turning *S4* on, the $V_{CC(CORE)}$ output is shorted to ground, and the CS5132 is placed in over-current hiccup mode.
- *S1* is the eight-position DIP switch located near *J1* and is used to set the $V_{CC(CORE)}$ DAC-programmable output voltage.
- *Switches 1-5* are used to set the five DAC bits to either logic 1 or 0 (V_{ID0}, V_{ID1}, V_{ID2}, V_{ID3}, V_{ID4}).
- *Switches 6*, *7*, and *8* are not used.
- In order to measure the voltage drop across the "Droop" Resistor when the regulator is loaded, connect a DC voltmeter across its terminals. The actual "Droop" Resistor value used for Adaptive Voltage Positioning can then be determined and verified.
- The $V_{CC(CORE)}$ DC output voltage can be measured by attaching voltmeter leads on terminals *TP3* (positive meter lead) and *TP4* (ground meter lead).
- The $V_{CC(CORE)}$ regulator can be disabled by installing jumper *JP2*. Removing jumper *JP2* enables the $V_{CC(CORE)}$ regulator.

$V_{I/O}$ Output

- The $V_{I/O}$ voltage output terminal *J3* is a female BNC connector, located on the top side of the board top layer near the bulk output capacitors. Using a standard BNC coax cable, the output voltage waveform can be observed on an oscilloscope during DC and AC load operation.
- The $V_{I/O}$ voltage output terminals *TP53* and *TP6* are gold pins located next to *J3*. An external electronic load can be connected to these terminals.
- The on-board $V_{I/O}$ resistive load banks are 4A (half load) and 8A (full load).
- The *Half Load Switch S6* is a SPDT type (AMP) and is located near the on-board resistive load bank. *Switch S6* is used to apply a load of 4A on the $V_{I/O}$ output.
- The *Full Load Switch S7* is a SPDT type (AMP) and is located near the on-board resistive load bank. *Switch S7* is used to apply a load of 8A on the $V_{I/O}$ output.
- *Current Limit* on $V_{I/O}$ can be tested in two ways: 1) by connecting an electronic load at the $V_{I/O}$ terminals *TP5* and *TP6* and increasing the load current until the CS5132 goes into "hiccup" mode, and 2) by turning both *Switches S6* and *S7* on, thereby applying 12A on $V_{I/O}$. The $V_{I/O}$ current limit setpoint is set at 11.3A, therefore with a 12A load the CS5132 is placed in over-current hiccup mode.
- The *Short Circuit Switch S5* is a SPDT type (AMP) and is located near the AT power supply connector *J2*. By turning *S5* on, the $V_{I/O}$ output is shorted to ground, and the CS5132 is placed in over-current hiccup mode.

Demonstration Board Operation Guidelines continued

- In order to measure the voltage drop across the "Droop" Resistor when the regulator is loaded, connect a DC voltmeter across its terminals. The actual "Droop" Resistor value used for Adaptive Voltage Positioning can then be determined and verified.
- The $V_{I/O}$ DC output voltage can be measured by attaching voltmeter leads on terminals *TP6* (positive meter lead) and *TP5* (ground meter lead).
- The $V_{I/O}$ regulator can be disabled by installing jumper *JP1*. Removing jumper *JP1* enables the $V_{CC(CORE)}$ regulator.

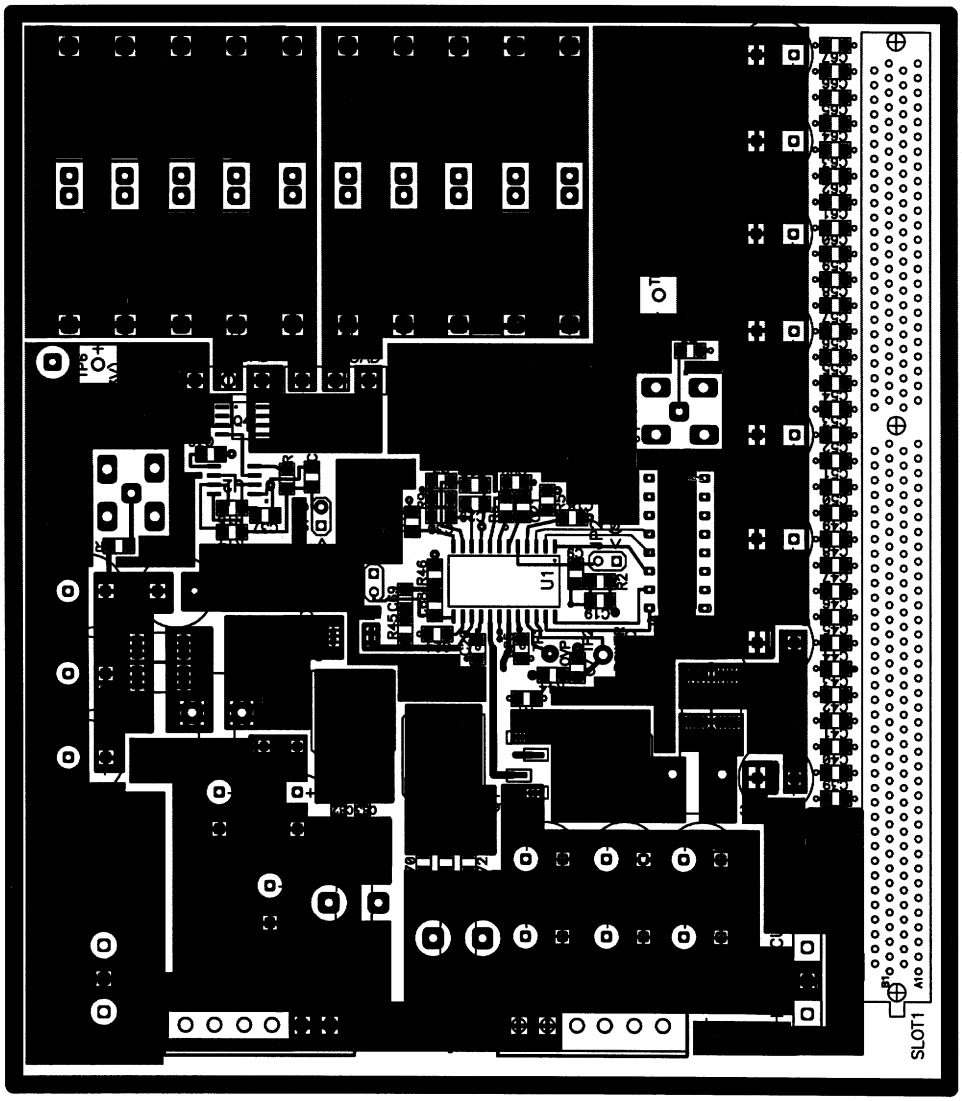
Demonstration Board Bill of Materials

Item #	Part Ident #	Qty Per Bd	Description of Part	Supplier	Catalog p/n
1	C1-6,C10-17, C26-28,C31-34	21	(Sanyo Vidio Components 3333 Sanyo Rd Forrest City, Ar. 72335) Electrolytic Cap 1200µF/10V	Sanyo	10MV 1200GX+T
2	C7,C20,C25, C35,36,C38-67	40	(Kyocera) Ceramic Surface Mt. Cap Size 1206 1.0µF 16V X7R	Farnell/ Newark	499-717
3	C9, C21, C30, C68	2	(Panasonic) Ceramic Surface Mt. Ca Size 1206 100000pF 50V	Digi-Key	PCC104 BCT-ND
4	C18	1	(Panasonic) Ceramic Surface Mt. Cap Size 1206 680pF 50V	Digi-Key	PCC681 BCT-ND
5	C19	1	(Panasonic) Ceramic Surface Mt. Cap Size 1206 10000pF 50V	Digi-Key	PCC103 BCT-ND
6	C69	1	(Panasonic) Ceramic Surface Mt. Cap Size 1206 100pF 50V	Digi-Key	PCC101 BCT-ND
7	C24	1	(Panasonic) Ceramic Surface Mt. Cap Size 1206 390pF 50V	Digi-Key	PCC391 BCT-ND
8	C37	1	(Panasonic) Ceramic Surface Mt. Cap Size 1206 27000pF 50V	Digi-Key	PCC273BCT-ND
9	D1	1	(Motorola) Power Rectifier DPak Surface Mt. MBRD835L Schottky	Newark	MBRD835L
10	JP1,2,3	3	(3M) Board Mount Interconnect (Jumper Pins) 36 Post Strip	Digi-Key	929647-09-36-ND
10A	SHUNTS	3	(3M) Board Mount Interconnect (SHUNTS) 2 Posts	Digi-Key	929955-06-ND
11	J1 + J3	2	(Multicomp) Straight Round PCB Socket BNC	Farnell/Newark	583-558
12	J2 + J4	2	(Molex) Straight Friction Lock Header p/n 26-48-1065	Digi-Key	WM4604-ND
13	L1,L3	2	(XFMRS) 1.0µH Coil	XFMRS,Ltd.	S26-10007
14	L2	1	(XFMRS) 1.2µH Coil	XFMRS,Ltd.	XF0016-V04
15	L4	1	(XFMRS) 3.5µH Coil	XFMRS,Ltd.	XF0046-V01
16	Q1,Q2 ,Q3	3	(Mitsubishi) N-Channel FET D2 Surface Mt. FS70VSJ-03	Richardson Electronics	FS70VSJ-03
17	Q4	1	(Mitsubishi) N-Channel FET (SO-8) FY10AAJ-03A (Branded FAJWA80E)	Gerber Electronics	FY10AAJ-03A
18	R1,R44	2	(Panasonic) Surface Mt. Resistor Size 1206 10.0kΩ 1/8 W	Digi-Key	P-10.0K-ECT-ND

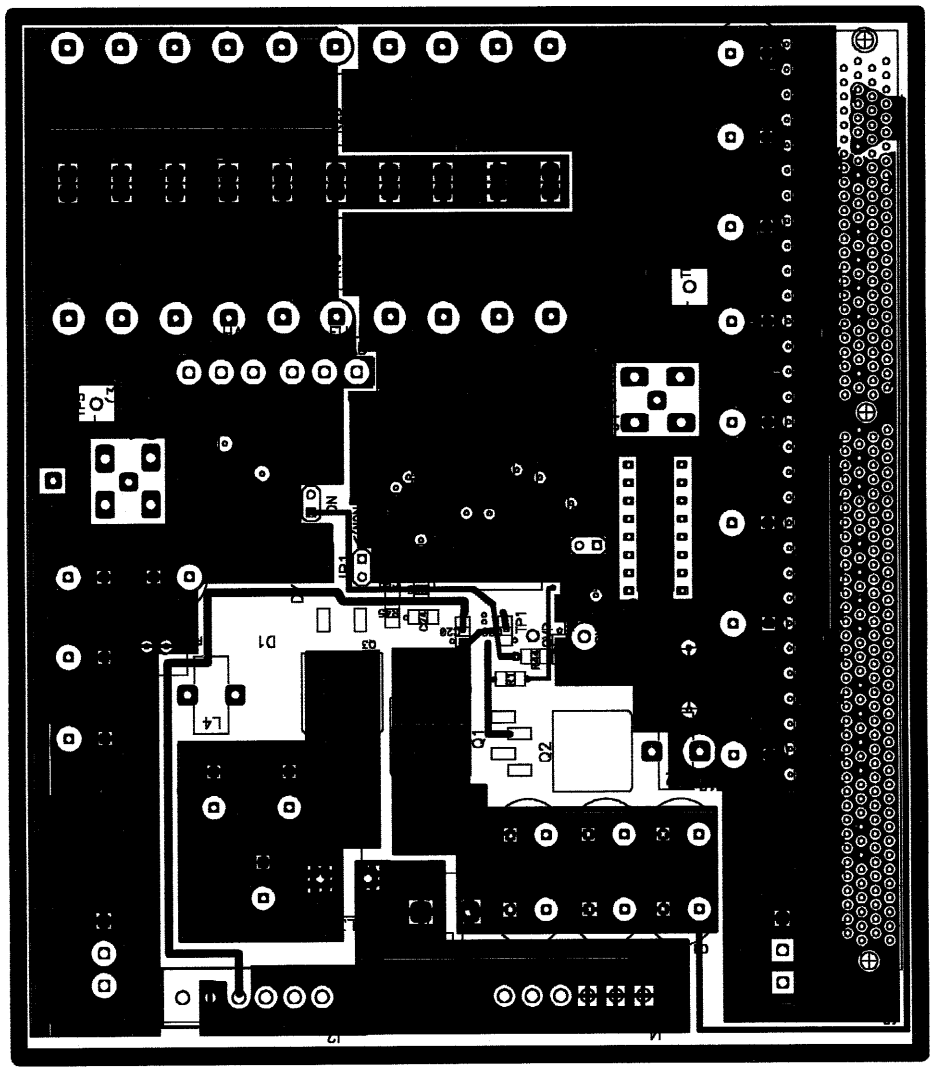
Demonstration Board Bill of Materials continued

Item #	Part Ident #	Qty Per Bd	Description of Part	Supplier	Catalog p/n
19	R2,R3,R11	3	(Panasonic) Surface Mt. Resistor Size 1206 100Ω 1/8 W	Digi-Key	P-100-ECT-ND
20	R4	1	(IRC) TYPE LR2512 **NEED (8)0.025 OHM 1W RESISTORS IN // = .0032**	NEWARK	96F7806
21	R5,R6,R9,R12	4	(Panasonic) Surface Mt. Resistor Size 1206 510Ω 1/8 W	Digi-Key	P-510-ECT-ND
22	R7	1	(Panasonic) Surface Mt. Resistor Size 1206 2.05kΩ 1/8 W 1%	Digi-Key	P-2.05K-FCT-ND
23	R8	1	(IRC) TYPE LR2512 **NEED (4)0.025 OHM 1W RESISTORS IN // = .0066**	NEWARK	96F7806
24	R10	1	(Panasonic) Surface Mt. Resistor Size 1206 1.24kΩ 1/8 W 1%	Digi-Key	P-1.24K-FCT-ND
25	R13,R14	2	(Panasonic) Surface Mt. Resistor Size 1206 2.0kΩ 1/8 W	Digi-Key	P-2.0K-ECT-ND
26	R15	1	(Panasonic) Surface Mt. Resistor Size 1206 13kΩ 1/8 W	Digi-Key	P-13K-ECT-ND
27	R16-25,R28-31,R33-38	20	(Panasonic) 8.2 ohm Metal Oxide Resistor 3W 5%	Digi-Key	P-8.2-W-3BK-ND
28	R43	1	(Panasonic) 6.2 ohm Metal Oxide Resistor 3W 5%	Digi-Key	P-6.2-W-3BK-ND
29	R45	1	(Panasonic) Surface Mt. Resistor Size 1206 12.0kΩ 1/8 W	Digi-Key	P-12.0K-ECT-ND
30	R46	1	(Panasonic) Surface Mt. Resistor Size 1206 51Ω 1/8 W	Digi-Key	P-51-ECT-ND
31	S1	1	(Amp) 8 Position DIP Switches Type 435640-5	Newark	44F7899
31A	S1-a	1	(Amp) 16 pin DIP Socket Type 2-640358-2	Newark	44F7974
32	S4-S5-S6-S7	4	(C&K) Switch (SPDT) on-on Mfg # 7101SYCQE	Digi-Key	CKN1004-ND
33	TP1-TP6	6	(Vector) Inboard Pins (Gold) K24A/M (1000 pcs)	Digi-Key	V1054-ND
34	U1	1	(ON Semiconductor) CS5132	–	–
35	U2	1	(National Semiconductor) 555 Timer Surface Mt. (SO-8)	Digi-Key	LM555CM-ND
36	Slot-1	1	(Amp) 242 Position Slot1 Connector	Newark	145251-2
37	CS5132	1	(CS5132) Demonstration Board Mfg Tel # 508-823-9888	CGI Circuits	–

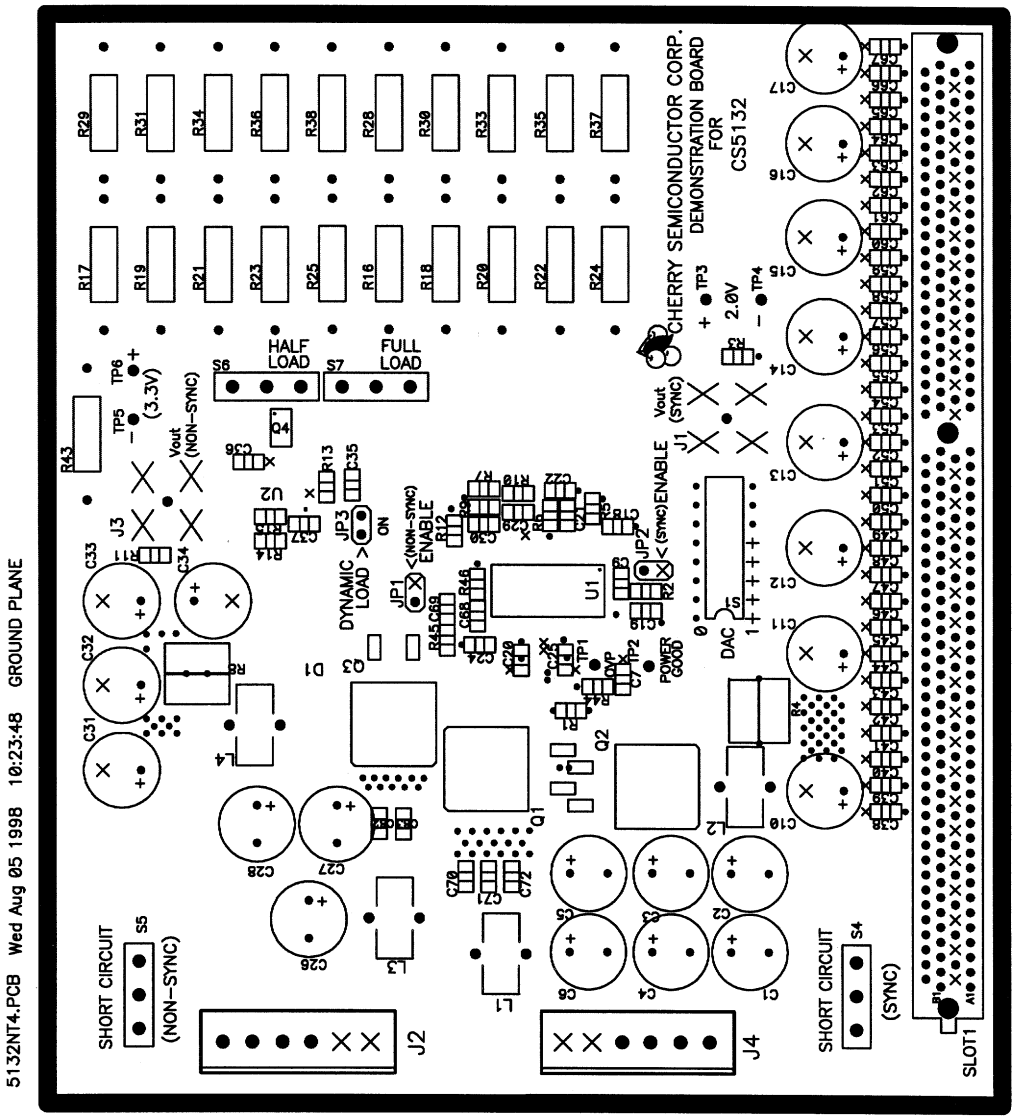
Top Layer



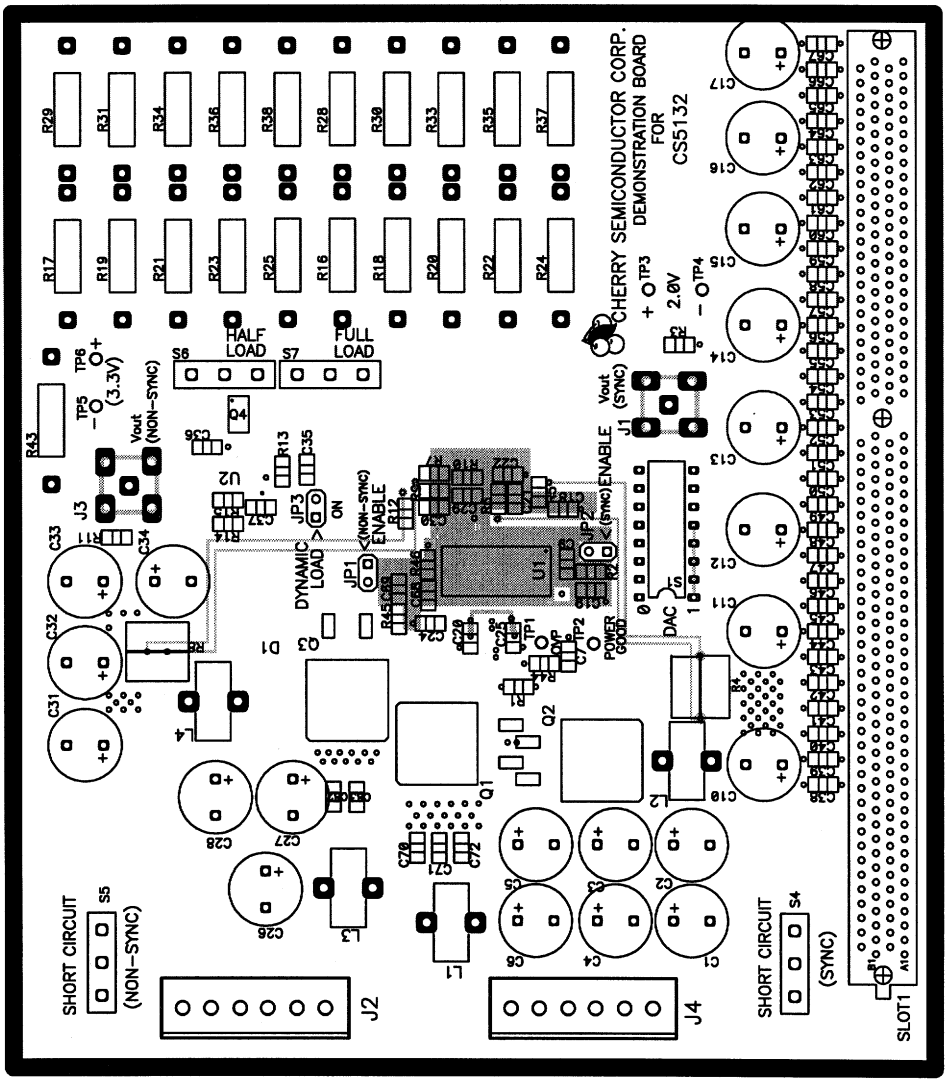
Mid Layer



Ground Plane



Bottom Layer



Notes

Notes

Notes