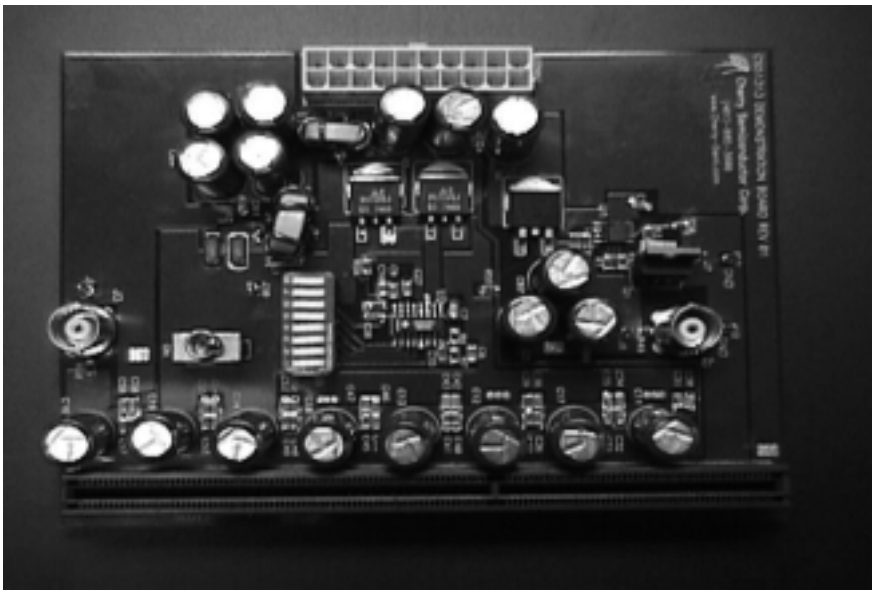
A Low Cost 500MHz Deschutes Demonstration Board Using the CS51313 5-Bit DAC Synchronous CPU Buck Controller IC with Power-Good, Hiccup Mode Current Limit, Precision Reference, and OVP

a CS51313 Demonstration Manual
10/09/98



November, 1998 - Rev. 0
CS51313DM

ON Semiconductor

Description

ON Semiconductor's low cost 500MHz Deschutes CS51313 Demonstration Board is a complete power solution for motherboards that feature high performance processors employing 5-bit supply voltage control and Power-Good function such as the Intel® Deschutes and AMD-K7™. The CS51313 demonstration board has input voltages of +5V, +12V, and +3.3V, and they are provided by a standard ATX computer power supply. +12V is the IC supply voltage, +5V is the $V_{CC(CORE)}$ synchronous buck regulator supply voltage and +3.3V is the V_{GTL+}, V_{CLOCK} linear regulator supply voltage. The on-board synchronous buck regulator regulates +2V / 16A (500MHz Deschutes $V_{CC(CORE)}$). The on-board V_{GTL+} linear regulator is implemented with the CS51313 V_{REF} output driving a general purpose dual LM358A operational amplifier, which in turn drives an IRL3303S or IRLZ24 MOSFET switch. The V_{GTL+} linear regulator regulates +1.5V / 3A with ± 3% DC and ± 9% AC tolerance (V_{GTL+}). The on-board V_{CLOCK} linear regulator is implemented with the CS51313 V_{REF} output driving the same general purpose dual LM358A operational amplifier, whose second output drives the TIP31A bipolar switch. The V_{CLOCK} linear regulator regulates +2.5V / 1A with ± 3% DC tolerance. Even though the CPU clock (V_{CLOCK}) only requires +2.5V / 250mA, the 1A output current capability of the on-board V_{CLOCK} linear regulator makes it possible to supply power to additional motherboard circuits that use a +2.5V supply, such as the chipset or RDRAM. The CS51313 demonstration board combines mixed assembly technologies. The input and output capacitors, input and output inductor, as well as the V_{CLOCK} linear regulator power bipolar switch are through- hole components. The synchronous buck regulator switching and synchronous MOSFETS, the V_{GTL+} linear regulator MOSFET switch, as well as the remaining external components are SMT. The CS51313 incorporates internal circuitry in the gate driver section, guaranteeing a typical 65ns adaptive non-overlap time between the High and Low side MOSFET gate voltages. This protection feature eliminates the possibility of external MOSFET shoot-through current that may potentially have catastrophic effects on the MOSFET itself as well as on the CPU. Additionally, the CS51313 provides adjustable hiccup mode current limit through a discrete sense resistor that can also be implemented as an inexpensive embedded PCB trace. The total PCB trace variation is typically ±56%, compared to ±96% using the $R_{DS(ON)}$ current limit method. As seen the power supply section is located next to the 242-pin Slot 1 socket, where the Intel Slot 1 EMT Tool can be inserted.

Today's advanced processors such as the Intel® Deschutes or AMD-K7™ have the capability of shutting down unused sections of the CPU in order to conserve power. Furthermore, they provide a 5-bit DAC code to the CPU power supply, demanding that the voltage regulator delivers an output voltage corresponding to the DAC code. When power resumes to the unused sections of the CPU, current transients from the Stop-Grant state to the Normal Operating state can place a severe burden on the processor power supply which has to provide a regulated output voltage as quickly as possible. When such extreme dynamic loads occur the CS51313 demonstration board is able to provide regulation in a very short period of time due to ON's proprietary V^{2}™ control topology

The V^{2}™ feedback architecture makes use of the ramp signal developed across the ESR of the output capacitors. This ramp signal is fed back into the V_{FB} pin (pin 7), and it is driven into two feedback loops. The slow feedback loop consists of an error amplifier that is only responsible for setting the DC output voltage accuracy. The fast feedback loop involves the PWM comparator and logic gates. When current transients occur, the change in the ramp signal across the output capacitors is fed back through the VFB pin, into the PWM comparator of the CS51313. This voltage feedback signal is only delayed by the PWM comparator and a minimal number of logic gates before the duty cycle of the external switching MOSFET is adjusted. As a result, the CS51313 demonstration board provides a tightly regulated output voltage to the CPU core.

The CS51313 demonstration board peak-to-peak output voltage is typically ±140 – 160mV during a 16A step@20A / µs. The CS51313 demonstration board also features the Intel-specified Power-Good output signal. When the regulator output voltage typically exceeds ± 8.5% of the nominal output voltage, the PWRGD pin (pin 14) is pulled low. Maximum output voltage deviation before PWRGD is pulled low is ± 12%.

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AMD-K7 is a trademark of Advanced Micro Devices, Inc.

Description continued

The CS51313 demonstration board employs adjustable hiccup mode Current Limit using a discrete sense resistor that also functions as the “Droop Resistor” for Adaptive Voltage Positioning (improved AC response). The only external component needed to implement hiccup mode Overcurrent protection is the COMP pin capacitor. Internally the CS51313 features a current sense comparator with a threshold voltage range of 74mV – 98mV. Once the voltage drop across the sense resistor exceeds the current sense comparator threshold voltage, the CS51313 power supply goes into “hiccup” mode. This protection scheme minimizes thermal stress to the regulator components, input power supply, and PCB traces, as the overcurrent condition persists.The discrete sense resistor (or embedded PCB trace) is placed between the output choke and output capacitors. The current limit trip point can be adjusted through selection of the desired sense resistor value or control of the length and width of the embedded PCB trace.

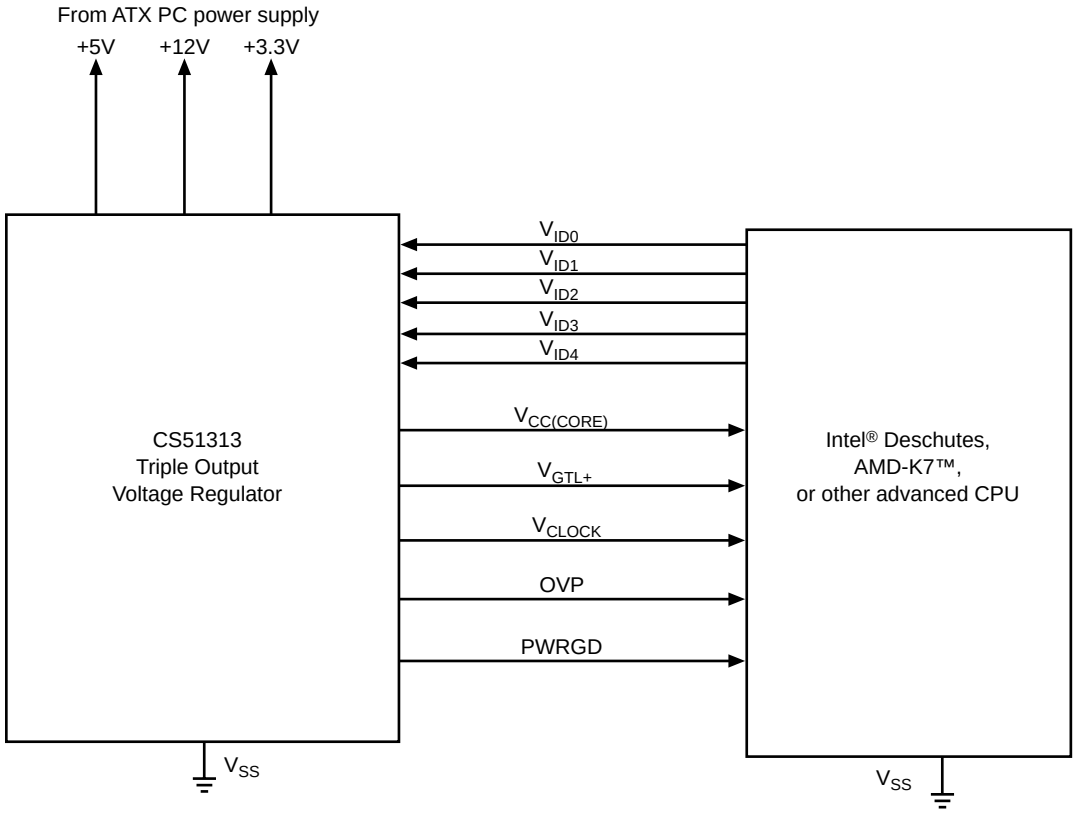
The guaranteed-by-design 65ns adaptive non-overlap time between the upper (switching) and lower (synchronous) FET is a significant feature of the CS51313 demonstration board. In conventional CPU buck regulator designs, there may be overlap between the upper FET switching off, and the lower FET switching on. Depending on the voltage level at which their gate pulses intersect, the shoot-through current can potentially be high enough to short the +5V supply line to ground, thereby destroying the lower FET, and, most importantly, inflicting irreversible damage to the microprocessor. The CS51313 provides a typical 65ns delay between the switching and synchronous FET gate pulse transitions, eliminating the need for a Schottky diode across the lower FET, whose fast recovery characteristic causes ringing in the order of 200MHz, and may eventually lead to EMI issues. The output voltage range of a CS51313-based CPU power supply is +1.2V – +3.5V, available at 50mV increments from +1.3V – +2.1V, and at 100mV increments from +1.2V – +1.3V and +2.1V – +3.5V. Such versatility is demanded by the various speeds of the processors that may be used in the Slot1 socket.

The CS51313 demonstration board demonstrates the features and benefits of the CS51313 5-bit DAC CPU Buck Controller IC with $V^{2™}$ technology controlling a triple-output PC motherboard power supply.

Features

- $V^{2™}$ Control Topology provides fast response to changes in both Line and Load
- Intel-specified PWRGD function
- 65ns Adaptive Non-Overlap Time between High and Low Side FET gate pulses
- Output Voltage programmable from 1.2V to 3.5V by 5-Bit logic level input
- Provides 16A for 500MHz Deschutes $V_{CC(CORE)}$, 3A for 500MHz Deschutes V_{GTL+}, and 1A for 500MHz Deschutes V_{CLOCK}.
- Low External Component Count and Solution Cost
- 2% DC Regulation, 5% AC Regulation
- Dedicated Overvoltage Protection (OVP) pin provides overall system power supply control
- Synchronous Rectification provides 90% Efficiency
- 1.2µH Output Inductor provides 8µs Response Time to a 16A Load Transient
- Adaptive Voltage Positioning improves AC Regulation and reduces response time during Load Transients
- Hiccup Mode Overcurrent Protection minimizes component stress
- Discrete sense resistor functions as a “Droop Resistor” and Current Sensing Element
- Dual logic-level N-Channel MOSFET Design – D^2PAK FS70VSJ-03
- 5V Supply Input with 4.25V UVL, 12V Bias Input
- On-board outputs can be exercised using resistive loads, electronic loads, or the Intel Slot1 EMT Tool
- Easy evaluation of DC and AC performance, Hiccup Mode Short-Circuit Protection and Current Limit
- OVP and PWRGD signals available for monitoring

Application Diagram



Demonstration Board Description

The CS51313 Demonstration Board is a four-layer $5^1/_2" \times 4^1/_4"$ PCB, with the actual triple output voltage regulator section occupying approximately a $3" \times 2^1/_2"$ area. This board incorporates all the circuitry required to fully evaluate the performance of the CS51313 CPU buck controller IC.

$V_{CC(CORE)}$ Output Voltage vs VID (Voltage Identification Code)

$10°C < T_A < 50°C$, $5V_{IN} = 5V$, $12V_{IN} = 12V$, $0A < I_{OUT} < 16A$, 2% DC accuracy								
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	MIN	TYP	MAX	UNITS
0	1	1	1	1	1.2985	1.325	1.3515	V
0	1	1	1	0	1.3475	1.375	1.4025	V
0	1	1	0	1	1.3965	1.425	1.4535	V
0	1	1	0	0	1.4455	1.475	1.5045	V
0	1	0	1	1	1.4945	1.525	1.5555	V
0	1	0	1	0	1.5435	1.575	1.6065	V
0	1	0	0	1	1.5925	1.625	1.6575	V
0	1	0	0	0	1.6415	1.675	1.7085	V
0	0	1	1	1	1.6905	1.725	1.7595	V
0	0	1	1	0	1.7395	1.775	1.8105	V
0	0	1	0	1	1.7885	1.825	1.8615	V
0	0	1	0	0	1.8375	1.875	1.9125	V
0	0	0	1	1	1.8865	1.925	1.9635	V
0	0	0	1	0	1.9355	1.975	2.0145	V
0	0	0	0	1	1.9845	2.025	2.0655	V
0	0	0	0	0	2.0335	2.075	2.1165	V
1	1	1	1	1	1.2210	1.246	1.2709	V
1	1	1	1	0	2.0825	2.125	2.1675	V
1	1	1	0	1	2.1805	2.225	2.2695	V
1	1	1	0	0	2.2785	2.325	2.3715	V
1	1	0	1	1	2.3765	2.425	2.4735	V
1	1	0	1	0	2.4745	2.525	2.5755	V
1	1	0	0	1	2.5725	2.625	2.6775	V
1	1	0	0	0	2.6705	2.725	2.7795	V
1	0	1	1	1	2.7685	2.825	2.8815	V
1	0	1	1	0	2.8665	2.925	2.9835	V
1	0	1	0	1	2.9645	3.025	3.0855	V
1	0	1	0	0	3.0625	3.125	3.1875	V
1	0	0	1	1	3.1605	3.225	3.2895	V
1	0	0	1	0	3.2585	3.325	3.3915	V
1	0	0	0	1	3.3565	3.425	3.4935	V
1	0	0	0	0	3.4545	3.525	3.5955	V

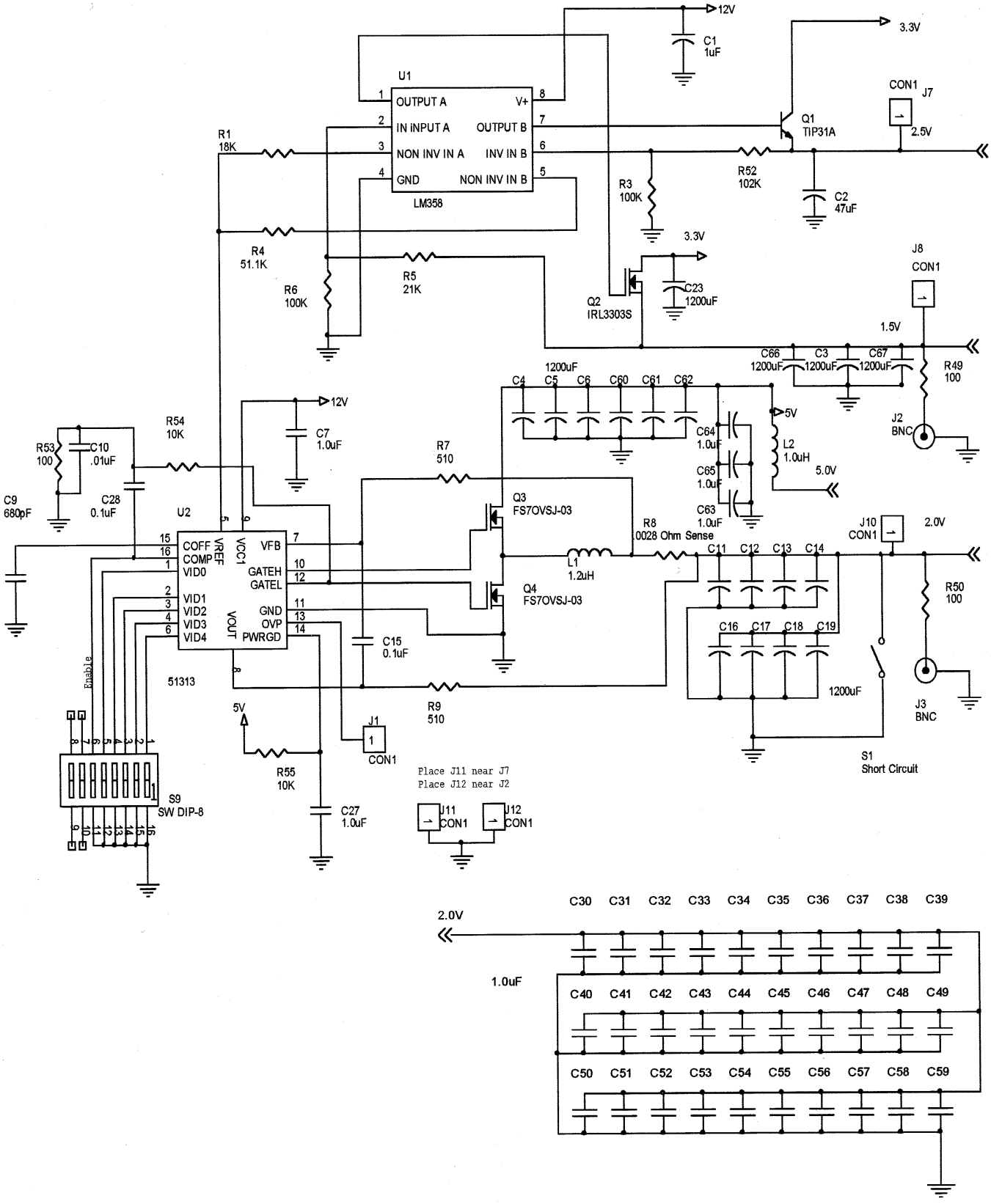
V_{GTL+} Output Voltage

$10°C < T_A < 50°C$, $3.3V_{IN} = 3.3V$, $12V_{IN} = 12V$, $0A < I_{OUT} < 3A$, 3% DC accuracy, 9% AC Accuracy				
	MIN	TYP	MAX	UNITS
V_{GTL+}(DC)	1.05	1.5	1.545	V
V_{GTL+}(AC)	1.365	1.5	1.635	V

V_{CLOCK} Output Voltage

$10°C < T_A < 50°C$, $3.3V_{IN} = 3.3V$, $12V_{IN} = 12V$, $0A < I_{OUT} < 1A$, 3% DC accuracy				
	MIN	TYP	MAX	UNITS
V_{CLOCK}(DC)	2.425	2.5	2.575	V

Demonstration Board Schematic



Demonstration Board Operation Guidelines

The CS51313 Demonstration Board is configured to demonstrate all the performance features and benefits of the CS51313 buck controller IC with V^{2TM} technology.

- The power supply input connector *CONN1* is the Molex Mini-Fit Jr.™ straight friction lock header type and is located on the board top layer.
- The power supply used is a computer ATX form factor 250W "silver box" type.

$V_{CC(CORE)}$ Output

- The $V_{CC(CORE)}$ voltage output terminal *J3* is a female BNC connector, located on the left near the bulk output capacitors. Using a standard BNC coax cable, the output voltage waveform can be observed on an oscilloscope during DC and AC load operation.
- The on-board 242-pin AMP Slot1 socket accepts the Intel Slot1 EMT Tool. Using the Intel-provided software, $V_{CC(CORE)}$ can be exercised in AC and DC conditions. Refer to Intel's Slot1 EMT Tool User's Guide for instructions.
- *Current Limit* can be tested by connecting an electronic load at the $V_{CC(CORE)}$ terminals and increasing the load current until the CS51313 goes into "hiccup" mode. The current limit is set at 30A, but can be decreased by replacing the two 5.1m discrete sense resistors (combined value = 2.55m with a higher value (3.2m sets the current limit trip-point at 25A).
- The *Short Circuit Switch S1* is a SPDT type (AMP) and is located near the $V_{CC(CORE)}$ terminal *J3*. By turning *S1* on, $V_{CC(CORE)}$ is shorted to ground, and the CS51313 is placed in hiccup mode.
- *S9* is the eight-position DIP switch located near *S1* and is used to set several CS51313 functions:
  1) *Switches 1-5* are used to set the five DAC bits to either logic 1 or 0.
  2) *Switch 6* is used to pull the COMP pin low, thus disabling the triple-output regulator. When *switch 6* is open, the triple-output regulator is enabled and normal operation occurs.
  3) *Switch 7* is not used.
  4) *Switch 8* is not used
- In order to measure the voltage drop across the "Droop" Resistor when the regulator is loaded, connect a DC voltmeter across its terminals. The actual "Droop" Resistor value used for Adaptive Voltage Positioning can then be determined and verified. Also, the DC output voltage can be measured by attaching voltmeter leads on terminal *J3* (positive meter lead) and *GND* (ground meter lead).

V_{GTL+} Output

- The V_{GTL+} voltage output terminal *J2* is a female BNC connector, located on the right near the bulk output capacitors. Using a standard BNC coax cable, the output voltage waveform can be observed on an oscilloscope during DC and AC load operation.
- *J8* and *J12* are the V_{GTL+} positive and GND voltage output terminals respectively. They can be used to connect an electronic or resistive load. The V_{GTL+} output voltage can be measured by attaching voltmeter leads to these terminals.

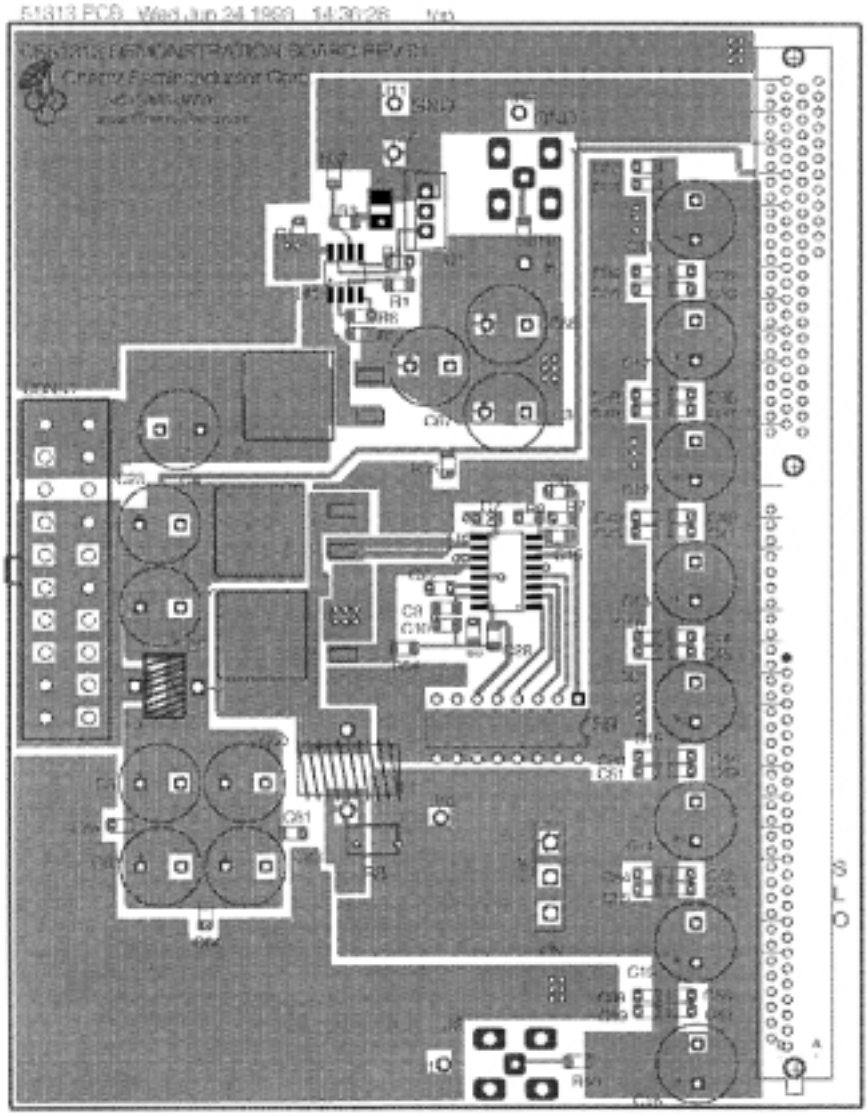
V_{CLOCK} Output

- The V_{CLOCK} voltage output terminals *J7* and *J11* are located on the right, and can be used to connect an electronic or resistive load. The V_{CLOCK} output voltage can be measure by attaching voltmeter leads to these terminals.

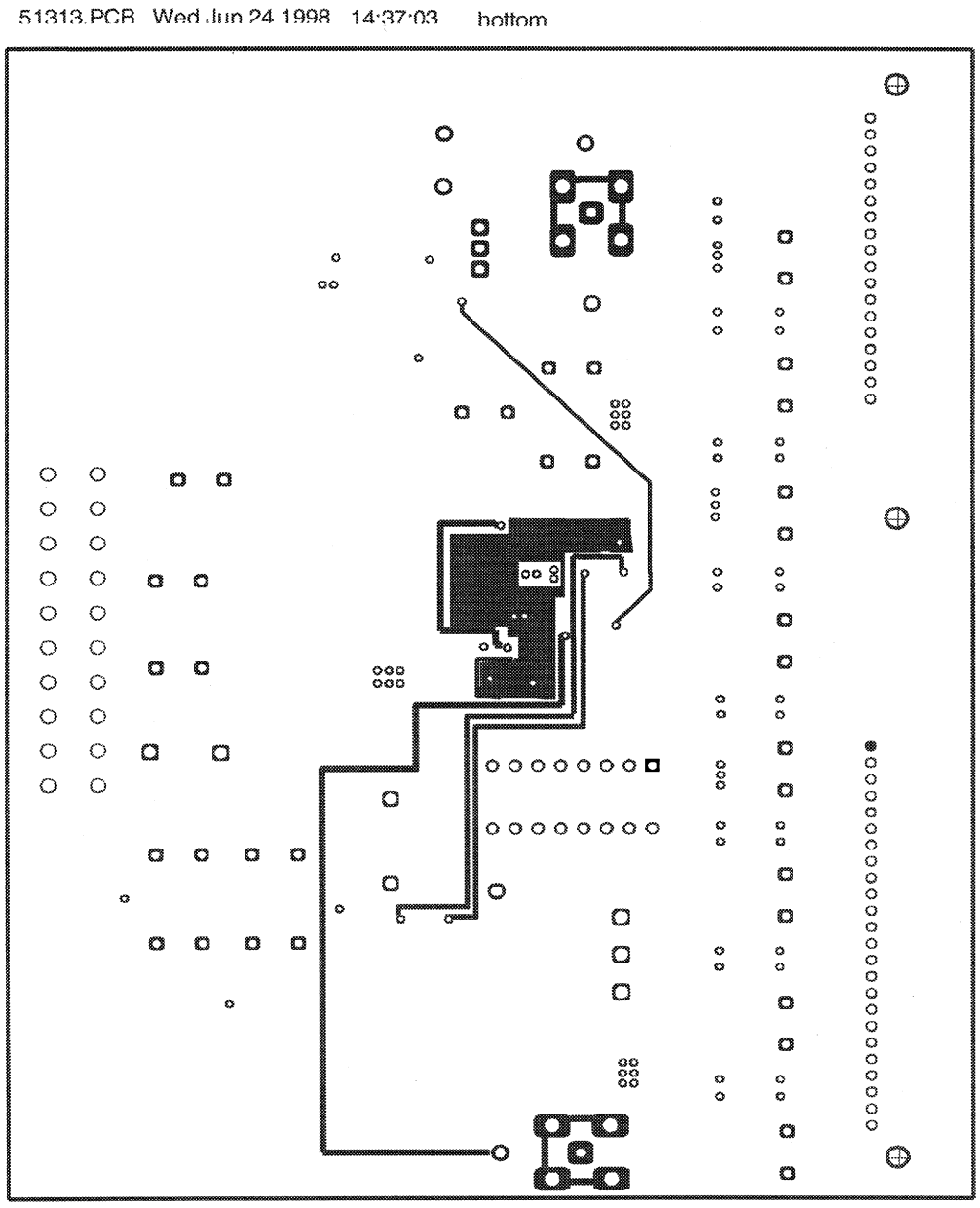
Demonstration Board Bill of Materials

Ref. Designator	Supplier	Part Number	Part Description	PC/Board	Value
C1,7,27,C30-59,C63-65	Newark	499-717	(Kyocera) Ceramic 1206	35	1.0µF
C2	Digikey	AVX TAJB476K006	Low ESR Tantalum	1	47µF
C3-6,C11-14,C16-19,23, C60-62,66,67	Sanyo	10MV 1200GX+T	10mm x 20mm Aluminum Electrolytic	18	1200µF
C8	Digikey	PCC101CCT-ND	50V Ceramic 1206	1	100pF
C9	Digikey	PCC681BCT-ND	50V Ceramic 1206	1	680pF
C10	Digikey	PCF1024CT-ND	50V Ceramic 1206	1	0.01µF
C15	Digikey	PCC223BCT-ND	50V Ceramic 1206	1	22nF
C28	Digikey	PCC472BCT-ND	50V Ceramic 1206	1	4.7nF
J2,3	Farnell	583-558	BNC	3	
J1,7,8,10,11,12	Digikey	V1054	Testpoint	6	
Q1	Digikey	TIP31A	NPN Transistor	1	
Q2	Newark	IRL3303S	N Channel Fet	1	
Q3,4	Mitsubishi	FS70VSJ-03	N Channel Fet	2	
R1	Digikey	P18K-ECT-ND	Res. 1% 1/8 w	1	18K
R3,6	Digikey	P100K-FCT-ND	Res. 1% 1/8 w	2	100K
R4	Digikey	P51.1K-FCT-ND	Res. 1% 1/8 w	1	51.1K
R5	Digikey	P21.5K-FCT-ND	Res. 1% 1/8 w	1	21.5K
R7,9	Digikey	P3.3K-ECT-ND	Res. 1% 1/8 w	2	3.3K
R49,50,53	Digikey	P100-ECT-ND	Res. 1% 1/8 w	3	100Ω
R8	KOA	SL1TE5LGOF	Low Ohmic Sense Res.	1	0.0028Ω
R52	Digikey	P102K-FCT-ND	Res. 1% 1/8 w	1	102K
R54	Digikey	P12K-ECT-ND	Res. 5% 1/8 w	1	12K
R55	Digikey	P10K-ECT-ND	Res. 5% 1/8 w	1	10K
S9	Newark	44F7899	8 DIP SW.	1	
S1	Newark	CKN 1004	SPDT Switch	1	
S1-A	Newark	44F7974	Dip Socket	1	
Conn1	MOLEX	39-28-1203	ATX Female Recepticle	1	
U1	Digikey	LM358-ND	Operational Amplifier	1	
U2	ON	CS51313	Controller	1	
L1	Xfmrs	XF0016-V03	Inductor	1	1.2-1.6µH
L2	Xfmrs	S26-10007	Inductor	1	1.0µH

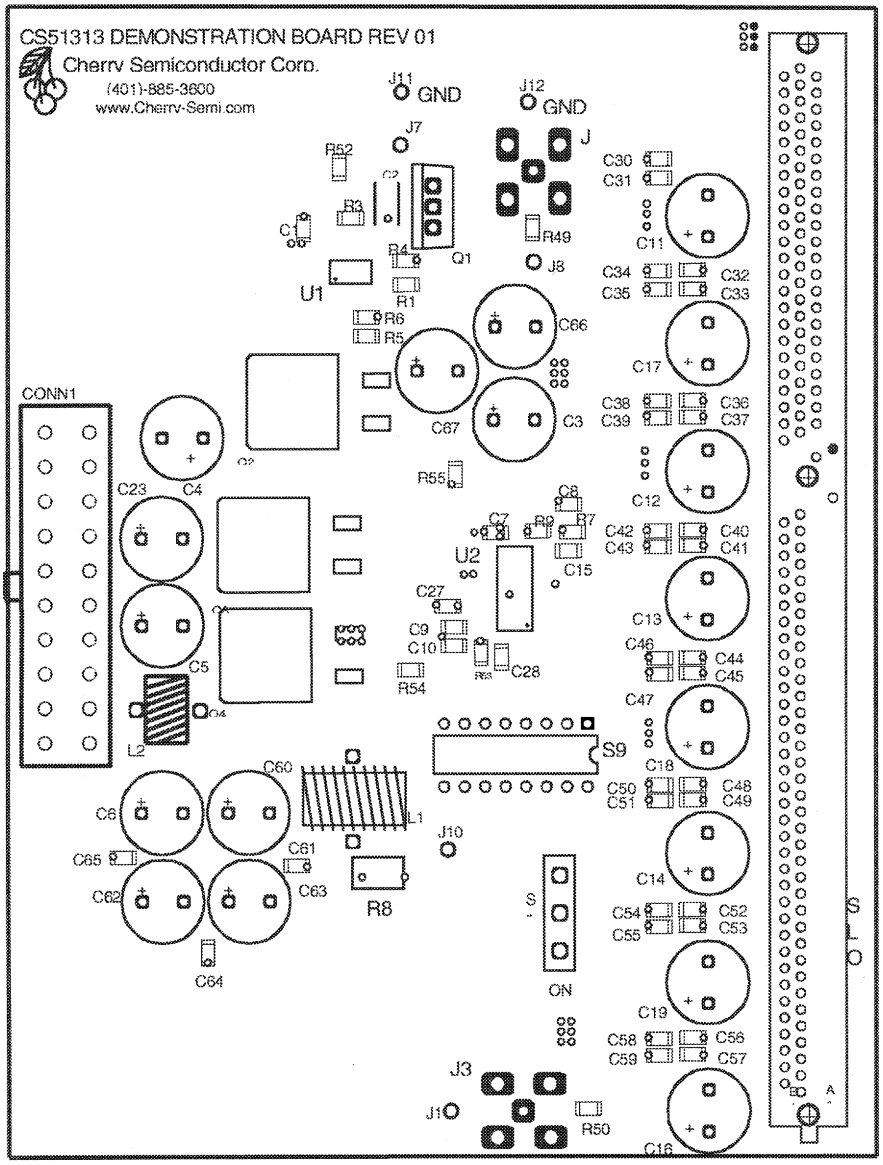
Top Layer



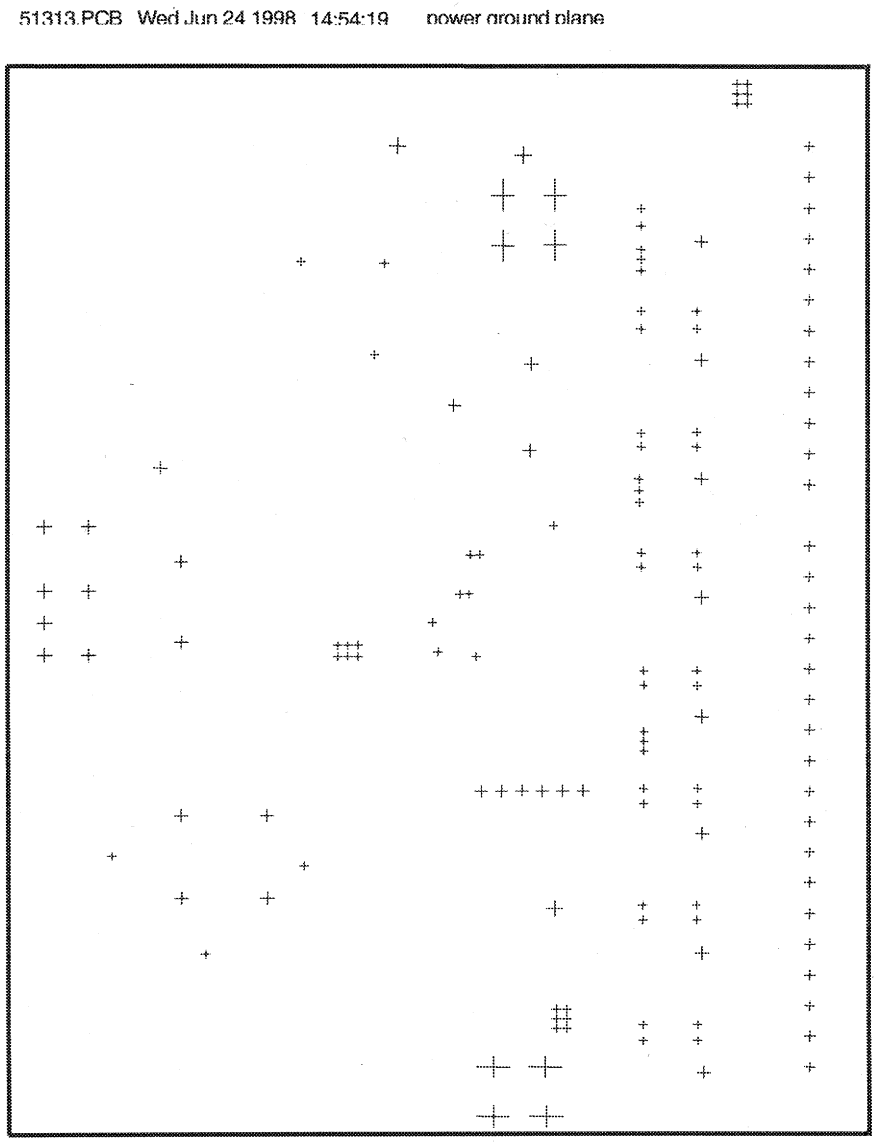
Bottom Layer



Silk Screen Layer



Power Ground Plane



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