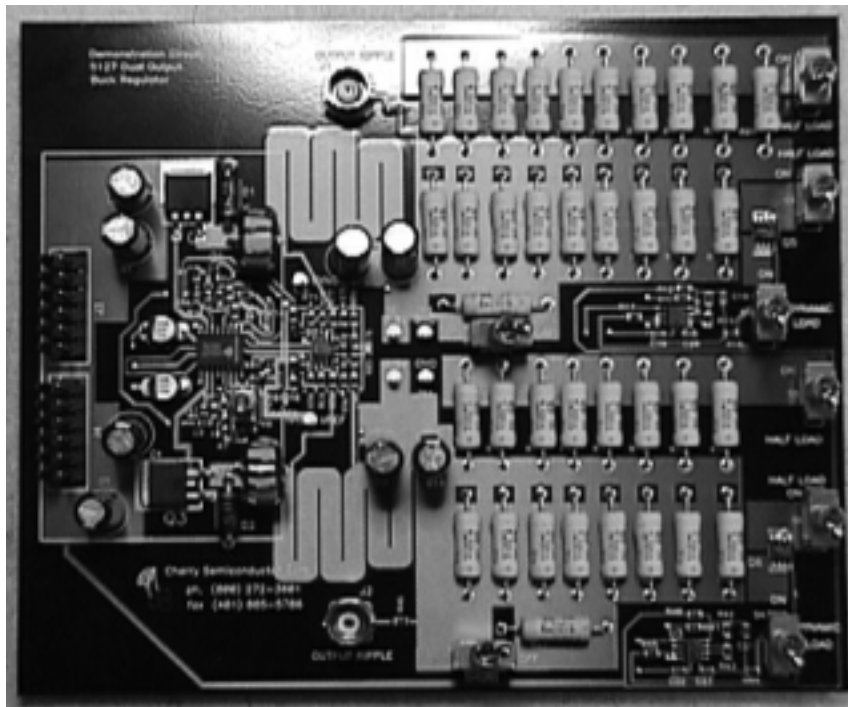# 2.8V, 7A and 3.3V, 7A Dual Output Buck Mode Power Supply with External Current Limit Circuit for V_{CORE} and V_{IO} Motherboard Applications

a CS5127 Demonstration Manual
05/08/98

ON Semiconductor

Description

This demonstration circuit showcases a dual output switching power supply. Using a 12V/5V input, two non-synchronous buck controller channels are used to provide separate 3.3V and 2.8V outputs, each capable of supplying 7A. The CS5127 controller IC features the proprietary V^{2TM} control architecture, and provides the fastest transient response available to date in a switch-mode power supply. Use of a single controller IC reduces component count. Additionally, the fixed frequency architecture makes noise minimization easier, since both outputs have the same switching frequency.

An external current limit circuit is added in this design. The current limit circuit requires a dual comparator, two capacitors, two PNP transistors, fourteen resistors and two current sense elements. These current sense elements may be high power, low value resistors or they may be fabricated using PC board metal traces. The demonstration circuit included in this note uses embedded PC traces as the sense elements.

Design of the CS5127 was completed with the goal of putting performance and value in the hands of every power supply designer. The external components and printed circuit board layout contained in this demonstration note are optimized for computer motherboard applications. This dual controller is a cost-effective solution for providing V_{CORE} and V_{IO} power solutions in computing applications using a single controller.

Features

- Nonsynchronous buck design
- V^{2TM} control topology
- 100ns transient loop response
- 200kHz oscillator frequency
- 55ns typical gate rise and 38ns typical gate fall times
- ENABLE input controls channel 2 gate driver
- External current limit circuit
- V_{REF} pin provides up to 10mA of current to power external circuitry

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V^2 is a trademark of Switch Power, Inc.

Application Diagram
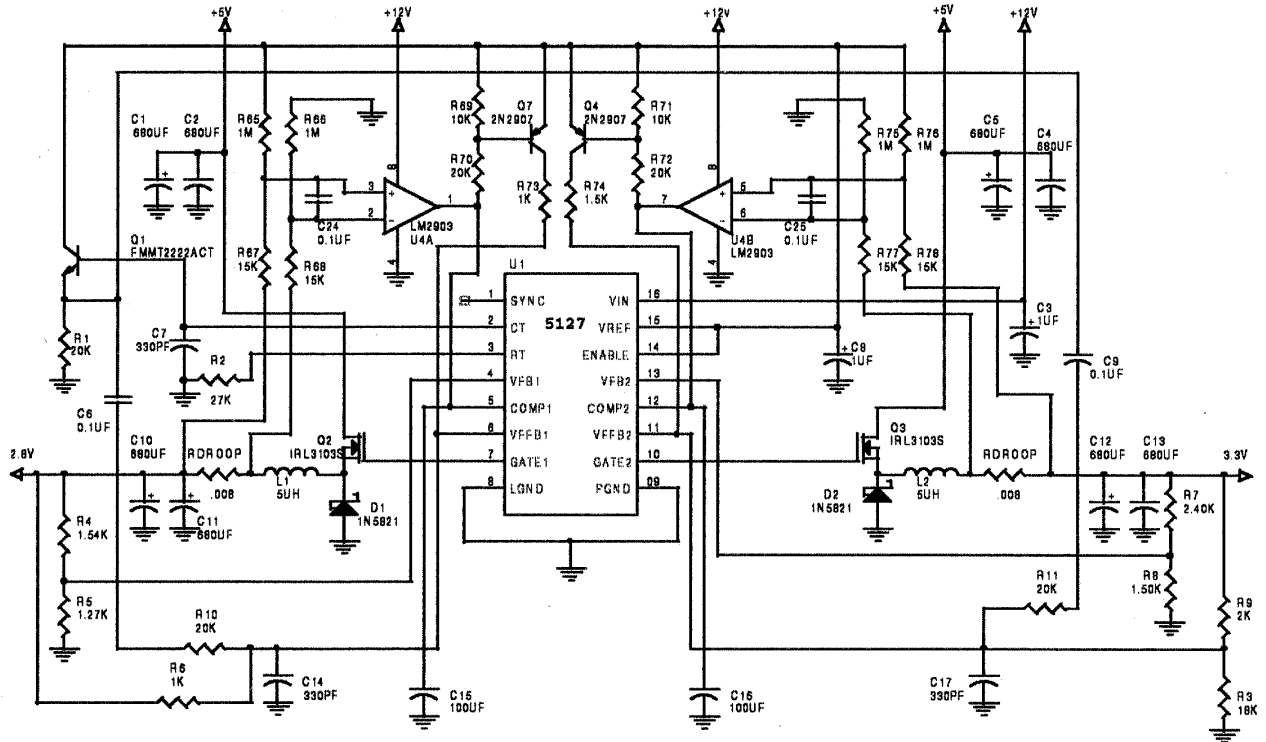
12V, 5V Input to Dual Output 3.3V @ 7A and 2.8V @ 7A for 233MHz Pentium MMX V_{IO} and V_{CORE}

Demonstration Board Description

The CS5127 Demonstration Board is a 7" by 6", two-layer printed circuit board holding both the dual supply and the test circuitry for the supply. The dual supply occupies an area about 2.5" by 3.5"including the current limit circuitry, and the test circuitry fills the rest of the board. The test circuitry is capable of exercising the dual supply in a number of ways. Each output channel can be run at minimum load (70 mA) DC, half load (3.5A) DC or full load (7.0A) DC. A transient test is also possible, where the load current steps from minimum load to half load or from half load to full load. Finally, a short circuit test is included. BNC connectors allow the output waveforms to be viewed with minimum noise pick-up. Standard oscilloscope probes are used to measure all other waveforms.

Application Interface Diagram

+12V   +5V

CS5127
Application
Circuit

+3.3V @ 7A

+2.8V @ 7A
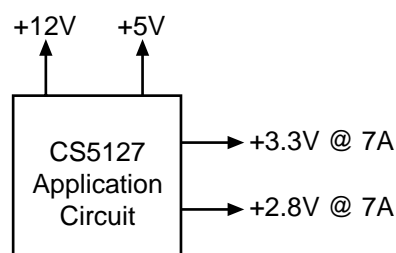
Absolute Maximum Ratings

Pin Name	Maximum Voltage	Maximum Current
+5V	+6V/−0.3V	20A (DC)
+12V	+15V/−0.3V	100mA (DC)
3.3V$_{OUT}$	+5V/−0.3V	10A (DC)
2.8V$_{OUT}$	+5V/−0.3V	10A (DC)

| Electrical Characteristics: 0°C ≤ T$_A$ ≤ 50°C, 4.75V ≤ +5V ≤ 5.25V, 11.8V ≤ +12V ≤ 13.2V, I(+5V) = 1A (both channels at minimum load), Unless Otherwise Specified					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**UNITS**
3.3V Output					
DC Output Voltage	500mA ≤ I$_{OUT}$ ≤ 7A	3.23	3.30	3.37	V
AC Voltage Regulation	3.5A load step, scope bandwidth at 20MHz		80		mV
Load Transient Response	I$_{SLEW}$ = 15A/μs, 100Hz TO 100kHz 3.5A load step, scope bandwidth at 20MHz Measure time 3.3V$_{OUT}$ exceeds DC limits when 500mA to 3.5A or 3.5A to 7A transient is switched.		10		μs
Ripple and Noise	500mA ≤ I$_{OUT}$ ≤ 7A, scope bandwidth at 20MHz		40	50	mV$_{P-P}$
Load Regulation (DC)	500mA ≤ I$_{OUT}$ ≤ 7A		11	20	mV
+5V Line Regulation	4.75V ≤ +5V ≤ 5.25V		2	15	mV
Efficiency	I(3.3V$_{OUT}$) = 7A		89		%
Current Limit	V$_{OUT}$ = 0V		10		A
2.8V Output					
DC Output Voltage	500mA ≤ I$_{OUT}$ ≤ 7A	2.74	2.80	2.86	V
AC Voltage Regulation	3.5A load step, scope bandwidth at 20 MHz		80		mV
Load Transient Response	I$_{SLEW}$ = 15A/μs, 100Hz TO 100kHz 3.5A load step, scope bandwidth at 20MHz Measure time 3.3V$_{OUT}$ exceeds DC limits when 500mA to 3.5A or 3.5A to 7A transient is switched.		10		μs
Ripple and Noise	500mA ≤ I$_{OUT}$ ≤ 7A, scope bandwidth at 20MHz		40	50	mV$_{P-P}$
Load Regulation (DC)	500mA ≤ I$_{OUT}$ ≤ 7A		11	20	mV
+5V Line Regulation	4.75V ≤ +5V ≤ 5.25V		2	15	mV
Efficiency	I(3.3V$_{OUT}$) = 7A		86		%
Current Limit	V$_{OUT}$ = 0V		10		A
+12V Input					
+12V Bias Current			22	30	mA
+12V Turn-on Voltage		7.4	8.4	9.4	V
+12V Turn-off Voltage		6.8	7.8	8.8	V
+12V Lockout Hysteresis			0.6		V
ENABLE Pin					
Channel 2 Duty Cycle	Enable pin grounded			0	%
	Enable pin tied to V$_{REF}$		55		%

Demonstration Board Schematic
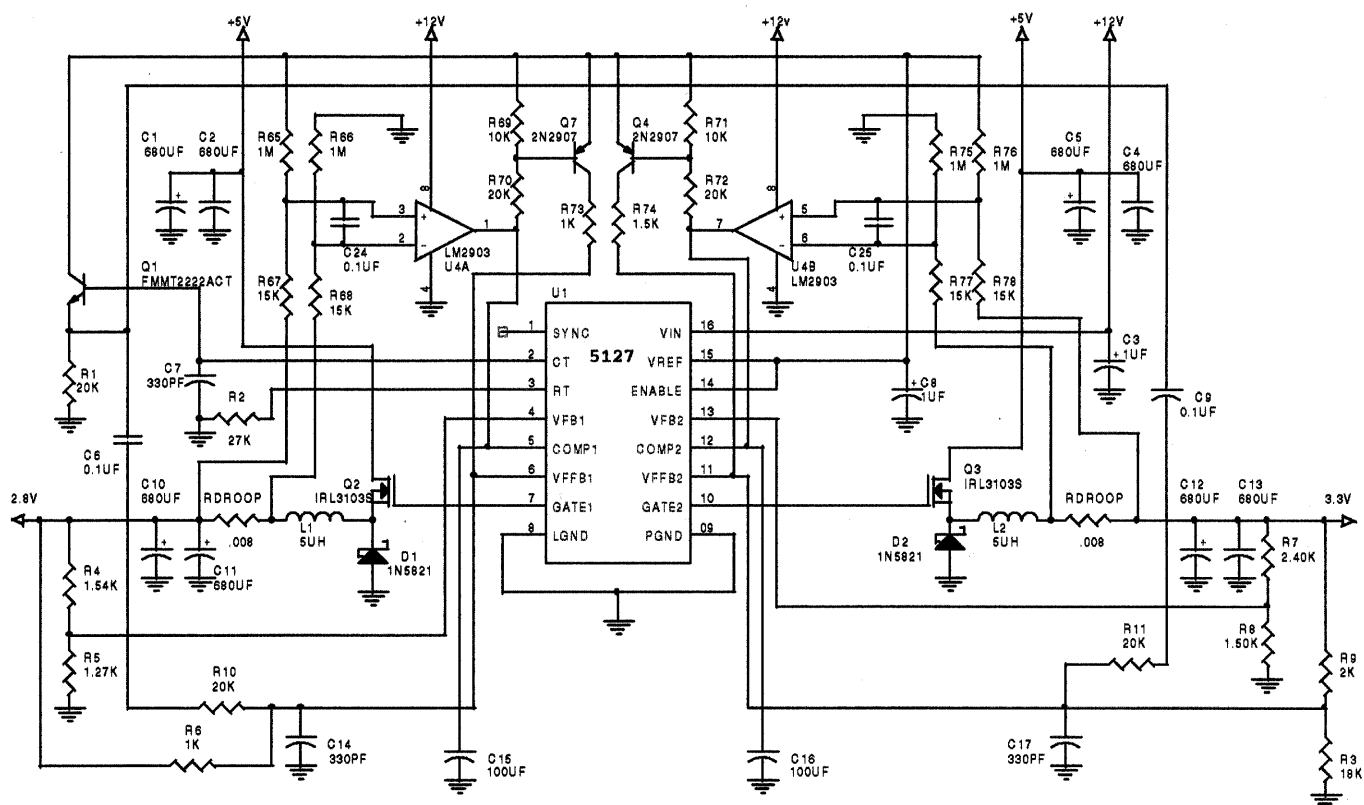
This is the application portion of the demonstration board. It shows the component reference designators corresponding to the printed circuit board layout and bills of materials that are included in this document.
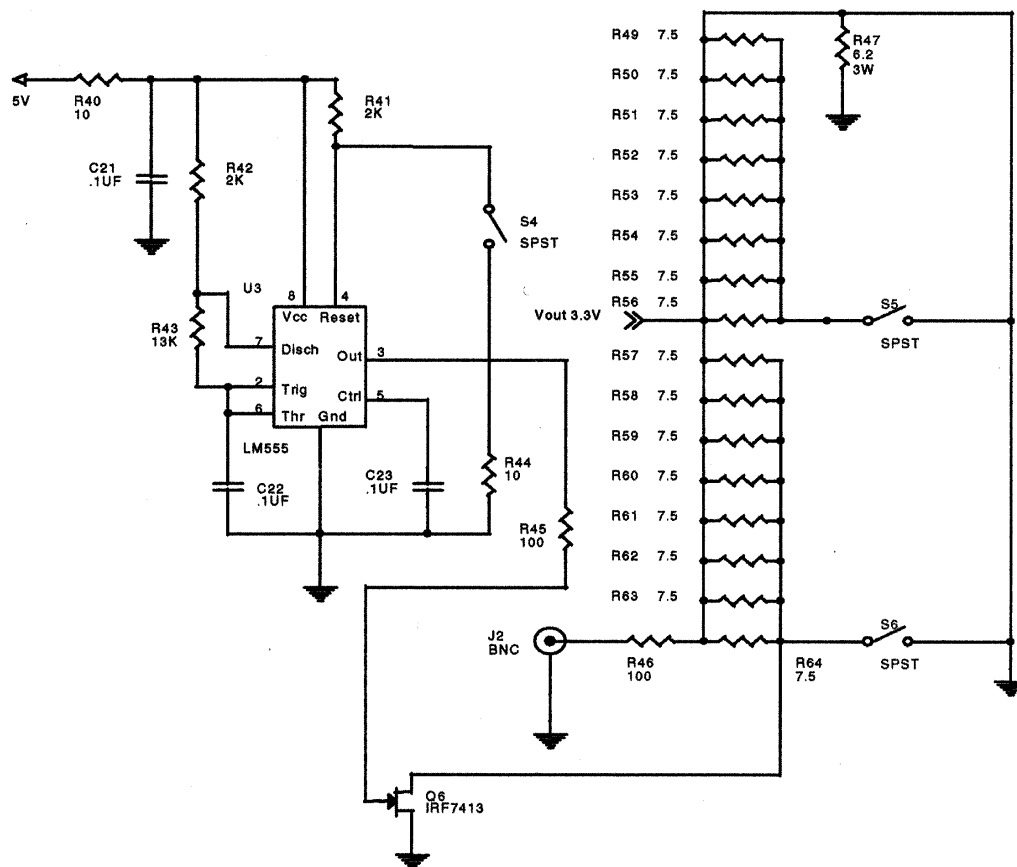
This schematic shows the test circuitry for the 3.3V output (channel 2). Reference designators correspond to the printed circuit board layout and the bill of materials.
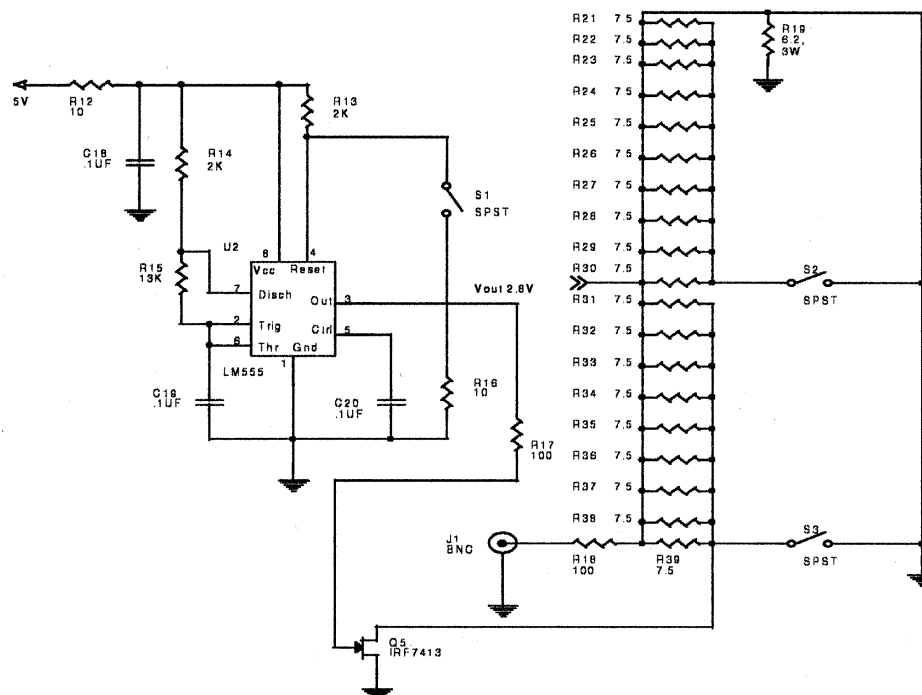
This schematic shows the test circuitry for the 2.8V output (channel 1). Reference designators correspond to the printed circuit board layout and the bill of materials.

Demonstration Board Operation Guidelines

No specialized equipment is required to exercise the CS5127 demonstration board. A "silver box" computer power supply and an oscilloscope with two BNC cable inputs are the only requirements.

Nine switches control the test modes for the CS5127 demonstration board. Switch S7 controls the ENABLE/DISABLE status of output channel 2 (3.3V output). Three switches for each output channel control DC current level and load transient testing. Switches S1, S2 and S3 control channel one, while switches S4, S5 and S6 control channel two testing. Switches S8 and S9 provide short circuit testing for channel 1 and channel 2, respectively. A list of test conditions and switch configurations is provided below. Testing of channel one is completely independent of testing of channel two, and both channels can be tested at full load simultaneously. An "X" in a column indicates a don't care condition.

Test Condition	S1	S2	S3	S4	S5	S6	S7	S8	S9
Output 1, 450mA DC	OFF	OFF	OFF	X	X	X	X	OFF	X
Output 1, 3.4A DC	OFF	ON	OFF	X	X	X	X	OFF	X
Output 1, 6.4A DC	OFF	ON	ON	X	X	X	X	OFF	X
Output 1, 450mA to 3.4A transient	ON	OFF	OFF	X	X	X	X	OFF	X
Output 1, 3.4A to 6.4A transient	ON	ON	OFF	X	X	X	X	OFF	X
Output 1 short circuited	X	X	X	X	X	X	X	ON	X
Output 2 disabled	X	X	X	X	X	X	DISABLE	X	OFF
Output 2, 530mA DC	X	X	X	OFF	OFF	OFF	ENABLE	X	OFF
Output 2, 4.05A DC	X	X	X	OFF	ON	OFF	ENABLE	X	OFF
Output 2, 7.57A DC	X	X	X	OFF	ON	ON	ENABLE	X	OFF
Output 2, 530mA to 4.05A transient	X	X	X	ON	OFF	OFF	ENABLE	X	OFF
Output 2, 4.05A to 7.57A transient	X	X	X	ON	ON	OFF	ENABLE	X	OFF
Output 2 short circuited	X	X	X	X	X	X	X	X	ON

As an example, if channel one was providing 3.4A DC while channel 2 was responding to a 530mA to 4.05A load step, switch settings would be:

	S1	S2	S3	S4	S5	S6	S7	S8	S9
	OFF	ON	OFF	ON	OFF	OFF	ENABLE	OFF	OFF

Design Procedure

Note: component reference designators contained in the Design Procedure refer to the Demonstration Board Schematic.

In order to begin designing a power supply using the CS5127, we must define the topology we wish to use, the supply voltages, the output voltage and current requirements and the switching frequency. Using the guidelines contained in the CS5127 data sheet, we chose to build a V^{2TM} controlled regulator. We chose to use a standard computer "silver box" power supply with both 12V and 5V outputs. The 12V supply provides the IC bias and the 5V supply provides the input power. Our regulator outputs were set at 3.3V and 2.8V, and both outputs can supply 7A to their loads. We chose a target switching frequency of 200kHz.

Choosing the Oscillator Components

We chose a switching frequency of 200kHz. We arbitrarily chose C7 = 470pF for small size and low cost. R2 can now be calculated:

$$R2 = \frac{1.88}{(200\text{kHz}) (470\text{pF})} = 20\text{k}\Omega$$

Choosing the Feedback Resistor Values

We first considered how to size R5 and R8. If each resistor is set to conduct 1mA, the V_{FB} pin bias current of 1mA will cause an error less than 0.1%. We chose a 1270W, 1%, 1/8W chip resistor. Thus, current in the divider is approximately

$$I_{V(FB)} = \frac{1.275}{1270} = 1.004 \text{ mA},$$

and expected error is

$$E = \frac{(1E - 6) (1270) (100\%)}{1.275} = 0.0996\%.$$

For the 2.8V output, we calculated the value of R4:

$$R4 = 1270 \times \left[\frac{2.8}{1.275} - 1 \right] = 1519\Omega.$$

Use a standard value of 1540Ω.

For the 3.3V output, we calculated the value of R7:

$$R7 = 1270 \times \left[\frac{3.4}{1.275} - 1 \right] = 2017\Omega.$$

Use a standard value of 2000Ω or 2050Ω.

Unfortunately, when we checked, we didn't have either value in stock. We looked for a good fit using values we did have, and found that setting R8 = 1500Ω gave a value of 2382Ω for R7. We used R7 = 2400Ω. The error from setting R8 = 1500Ω is

$$E = \frac{(1E - 6) (1500) (100\%)}{1.275} = 0.118\%.$$

Choosing the Inductors

We first solved for the 2.8V output minimum inductance value. We decided to set I_{MAX} = 10A as a limit for the inductor saturation current. This gave

$$L_{MIN} = \frac{(5V - 2.8V) (2.8V)}{(200\text{kHz}) (10A) (5V)} = 0.6\mu\text{H}.$$

For this inductor, ripple current was calculated as

$$I_{RIPPLE} = \frac{(5V - 2.8V) (2.8V)}{(200\text{kHz}) (0.6\mu\text{H}) (5V)} = 10.27\text{A}.$$

Increasing the inductance reduces the ripple current, so we tried 5μH:

$$I_{RIPPLE} = \frac{(5V - 2.8V) (2.8V)}{(200\text{kHz}) (5\mu\text{H}) (5V)} = 1.232\text{A}.$$

This is much more realistic.

We then calculated the maximum output current using the 5μH inductor.

$$I_{OUT(MAX)} = 10A - \frac{(5V - 2.8V) (2.8V)}{(2) (200\text{kHz}) (5\mu\text{H}) (5V)} = 9.38\text{A}.$$

This is adequate for our needs.

We then solved for the 3.3V output inductor:

$$L_{MIN} = \frac{(5V - 3.3V) (3.3V)}{(200\text{kHz}) (10A) (5V)} = 0.56\mu\text{H}.$$

For this inductor, ripple current was calculated as

$$I_{RIPPLE} = \frac{(5V - 2.8V) (2.8V)}{(200\text{kHz}) (056\mu\text{H}) (5V)} = 10.02\text{A}.$$

We tried 5μH again:

$$I_{RIPPLE} = \frac{(5V - 3.3V) (3.3V)}{(200\text{kHz}) (5\mu\text{H}) (5V)} = 1.122\text{A}.$$

$$I_{OUT(MAX)} = 10A - \frac{(5V - 3.3V) (3.3V)}{(2) (200\text{kHz}) (5\mu\text{H}) (5V)} = 9.44\text{A}.$$

Design Procedure continued

Thus, both inductors should be 5µH and rated for 10A. We chose the XF0066-VO2 from XFMRS, Inc. for both L1 and L2.

Choosing the Output FETs

We looked for an inexpensive logic level n-channel FET. Logic level is desirable in this application since there is only 7V of gate drive available, and 1.5V of that is used in the CS5127 output drivers. We wanted the FET to withstand a minimum of 15V and have current carrying capability of at least 10A. Additionally, low $R_{DS(ON)}$ and surface mount packaging were important. We chose the IRL3103S from International Rectifier for Q2 and Q3. The IRL3103S is a logic level n-channel FET capable of withstanding 30V, carrying 64A with $R_{DS(ON)}$ of 14mΩ, and the D^2 package features θ_{JA} of 40°C/W.

Choosing the Catch Diodes

These components are usually schottky diodes to minimize the forward voltage drop and improve system efficiency. The diodes are chosen based on reverse voltage, average current capability and turn-on voltage. In this application, the maximum reverse voltage that will be experienced by the catch diodes is V_{IN} plus some tolerance, or about 14V. The average current in the catch diode is given as

$$I_{D(AVE)} = I_{LOAD} \times \frac{V_{SUPPLY} - V_{OUT}}{V_{SUPPLY}}$$

This comes out to about 3.1A for the 2.8V output and 2.4A for the 3.3V output. We chose to use the 1N5821 from LiteOn Power Semiconductor for D1 and D2. This diode has a 3A average current rating, a withstand voltage of 30V and a turn-on voltage of 0.5V.

Choosing the Output Capacitors

We based our choice for output capacitors on four considerations: RMS ripple current rating, ESR, size and price. The capacitor network must be capable of handling the inductor ripple current of 1.2A. The ripple current flowing in the capacitor ESR will produce the output ripple voltage. Our demonstration board accepts its power through two standard J-connectors, so the capacitor height should be lower than the height of the connectors, and price should be as low as possible. We chose to use two Panasonic ECA-1AFQ681 capacitors in parallel for each output (C10, C11, C12, C13). These capacitors have a ripple current rating of

760mA and typical ESR of 90mΩ. Two capacitors in parallel give 1.5A of ripple current capability and ESR of 45mΩ. The ripple current into the ESR will produce about 55mV of output ripple voltage.

A load step will produce an instantaneous change in the output voltage defined by the magnitude of the load step and the output capacitor ESR. Our test setup produces a 3.5A load step. The worst case change in output voltage due to the load step will be

$$\Delta V_{OUT} = \Delta I_{OUT} \times ESR = (3.5A)\,(0.045\Omega) = 0.158V.$$

Choosing the Input Bypass Capacitors

We chose bypass capacitors for the FET drains with the same criteria used for the output capacitors. In this case, though, the ripple current during switch transitions is much larger:

$$I_{RIPPLE} = I_{OUT} \sqrt{\frac{(V_{IN} - V_{OUT})\,(V_{OUT})}{V_{IN}^2}} = 3.48A$$

However, the current "spikes" during the switch transitions are of very short duration. A voltage spike at the transition is defined as:

$$\Delta V = (ESR)\,(I_{RIPPLE}) = 0.157V$$

This momentary glitch introduces noise but does not otherwise impact system operation. The other component of ripple current in the input bypass capacitors is due to the inductor ripple current and has the same magnitude of about 1.2A. We chose to use the same capacitor type and value for the input bypass caps that we used for the output capacitors. We placed two Panasonic ECA-1AFQ681 capacitors (C1, C2, C4, C5) in parallel right at the drain of each FET. These capacitors help to minimize EMI and reduce ripple current in the 5V supply. We also chose to include bypass capacitors on the V_{IN} and V_{REF} lines of the IC (C3, C8). At 200kHz, a 1µF capacitor presents an impedance of 0.8Ω which should conduct any switching noise.

Choosing the COMP Pin Capacitors

We chose to impose a 0.1% tolerance on the DC level of the COMP pin voltage. At 200kHz, $T_{OSC} = 5µs$, and

$$C_{COMP(MIN)} = \frac{(0.016A)\,(5E - 6s)}{(2.8V)\,(0.001)} = 28.6µF$$

$$C_{COMP(MIN)} = \frac{(0.016A) \ (5E - 6s)}{(3.3V) \ (0.001)} = 24.2\mu F$$

We chose to use 100μF capacitors for C15 and C16 as recommended by the datasheet. Increasing the COMP pin capacitor value improves noise immunity.

Choosing the V$_{FFB}$ Pin Components

We started by determining how the DC bias would be provided. The 2.8V output is low enough to provide DC bias to the V$_{FFB1}$ pin, but the 3.3V output is very near the PWM comparator common mode maximum input voltage. We chose to use a resistor divider to provide the DC bias for the 3.3V output. We set the total divider resistance at 20kΩ between the 3.3V output and ground. This sets the divider current at 165μA. We chose to set the DC bias voltage at about 3V, so our divider resistors can be calculated:

$$R3 = 20k\Omega \times \frac{(3.0V)}{(3.3V)} = 18k\Omega, \text{ and}$$

$$R9 = 20k\Omega - 18k\Omega = 2k\Omega.$$

This ratio keeps 90% of the output voltage ripple as input to the V$_{FFB}$ pin so that V^{2TM} control will function properly. R9 also serves as the filter resistor for the 3.3V output.

We chose to use identical 330pF capacitors for V$_{FFB}$ filter capacitors C14 and C17, and we set R6 equal to 1K. This gives cutoff frequencies of 3MHz for the 2.8V output and of 1.5MHz for the 3.3V output. This effectively removes switching noise from the V$_{FFB}$ bias levels.

To provide the artificial ramp signal, we chose a SOT-23 packaged NPN transistor for Q1. We used Zetex's FMMT2222A transistor. This transistor can provide as much as 600mA of current and has a forward current gain (H$_{FE}$) between 100 and 300. It is important to have a fairly high gain so that the transistor does not load down the CT pin capacitor. Such loading will decrease the switching frequency.

The CS5127 datasheet provides the CT pin peak and valley thresholds for the oscillator. We used the peak threshold of 3.6V to help us determine the maximum bias current for Q1. Assuming V$_{BE(ON)}$ for Q1 is 700mV, the maximum emitter voltage for the transistor will be 3.6V − 0.7V = 2.9V. We arbitrarily chose to use a 20K resistor for R1. This sets the maximum quiescent current for Q1 at 145μA. If forward current gain is 100, the

current load on the CT pin due to Q1 is about 1.5μA. The error introduced by this loading can be approximately calculated as

$$E_{FREQ} = \frac{R2}{(R1) \ (H_{FE})} \ ,$$

where H$_{FE}$ is the forward current gain of the transistor at the DC bias current level.

For our circuit, E$_{FREQ}$ is less than 1%.

We use 2 capacitors to couple the artificial ramp signal into the V$_{FFB}$ pins. Ideally, these capacitors present as low a resistance as possible at the switching frequency so that the full amplitude of the voltage signal at Q1's emitter is present on the V$_{FFB}$ side of the capacitor. We chose C6 and C9 at 0.1μF. At 200kHz, this value represents a resistance of about 8Ω.

We now need to calculate the amount of artificial ramp needed to stabilize our system. For the 2.8V output,

$$V_{RAMP} = \frac{(0.045\Omega) \ (2.8V)}{(2000) \ (5\mu H)} = 12.6mV \text{ per period.}$$

However, we must add the output voltage ripple to this value to calculate the value of R10:

$$R_{RAMP} = (1k\Omega) \left[\frac{2.1V}{57.6mV} - 1 \right] = 35k\Omega.$$

Use a standard value of 33kΩ.

When we tried this resistor value, we observed some minor pulse skipping. Decreasing R10 to 27K eliminated the pulse skipping, and further decreasing R10 to 20K did not affect transient response. We chose 20kΩ for a final value.

For the 3.3V output,

$$V_{RAMP} = \frac{(0.045\Omega) \ (3.3V) \ (18K)}{(2000) \ (5\mu H) \ (20K)} = 13.4mV \text{ per period.}$$

$$R_{RAMP} = (2k\Omega) \left[\frac{2.1V}{59.9mV} - 1 \right] = 68k\Omega.$$

This resistor value for R11 also resulted in some pulse skipping. Decreasing the resistor value to 27kΩ again eliminated the problem, and decreasing the value to 20kΩ did not affect transient response. We chose 20kΩ as the final value.

With this calculation, our converter design was complete. As noted above, some optimization was required

Design Procedure continued

for the values of R10 and R11, but system performance is otherwise good.

Design of the Current Limit Circuit

Several factors must be considered in designing a current limit circuit for the CS5127. First, a measurement of the inductor current must be provided. Second, this measurement must be compared against a reference, and a decision made on whether or not to terminate conduction in the switch. Finally, the actual turn-off of the switch must occur.

Our design uses a resistor to measure the inductor current. This resistor may be implemented in several ways, but two primary methods are use of a high-precision current sense resistor and use of an embedded PC board trace. The precision current sense resistor is a fairly expensive component, but it is accurate, will dissipate large amounts of power and is usually available in a surface mount package. It uses very little PC board area. The embedded PC board trace, on the other hand, costs nothing for components, but uses a large amount of board area and is usually only accurate to about ± 30%. We chose to use an embedded trace. The sheet resistance of the copper in the PC board can be obtained from the PC board manufacturer. The embedded trace resistance is then calculated by

$$R_{TRACE} = (L/W)\,(R_{SHEET})$$

where L is the length of the trace (any unit of length), W is the width of the trace (in the same unit as L) and L/W provides the number of squares of metal in the trace. R_{SHEET} is given in ohms per square, and the product of R_{SHEET} and the number of squares yields an answer in ohms. If the embedded trace cannot be made from a single straight segment of metal, the corners at which the embedded trace turns have the effect of providing approximately one half square of resistance.
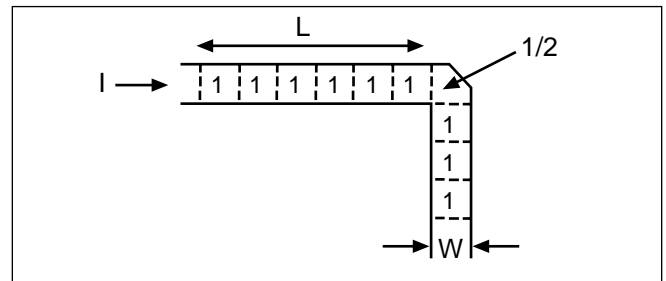
Figure 1: Calculating resistance by number of squares: L/W gives the number of squares. Corners give $1/2$ square to total.

The comparison is done by means of a comparator with open collector output. Two conditions must be applied to the IC to turn the output switch off. The COMP pin must be pulled low at the same time as the V_{FFB} pin is pulled high. This can be accomplished by using the open collector output of the comparator to pull down on the COMP pin, and on a resistor divider that will turn a PNP transistor on. The PNP transistor then can pull up the V_{FFB} pin to complete the turn off process. The comparator output must be capable of sinking in excess of 3mA to completely sink the COMP pin source current while driving the PNP transistor hard enough to pull up the V_{FFB} pin.
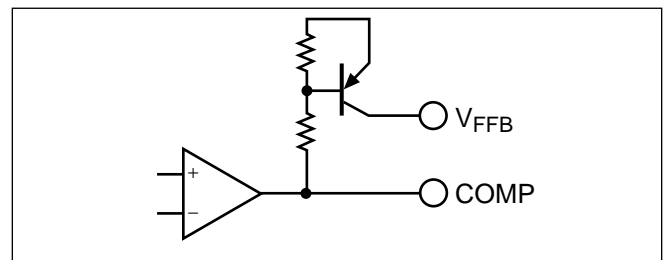
Figure 2: Comparator configuration to pull COMP pin low while pulling V_{FFB} pin high simultaneously.

Finally, some means of providing the reference and the measured current to the circuit for comparison must be devised. A simple resistor divider can accomplish this goal.
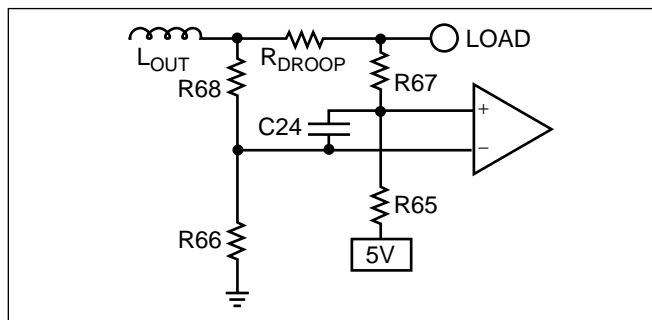
Figure 3: Current comparator schematic valid for output voltages less than 5V.

When the load is shorted to ground, a DC voltage will exist across the droop resistor. At the same time, the resistor divider from 5V establishes a reference voltage on the non-inverting input. When the current in the droop resistor becomes large enough, the comparator will change states, and the output will sink current. This pulls the COMP pin down, drives the V_{FFB} high and terminates conduction in the switch. As current begins to decrease, the comparator will return to its original off-state, and the switch FET will turn on at the next oscillator cycle. If the load is still shorted, current will rise until the shutdown sequence occurs again. The result is that an average current slightly lower than the programmed current limit will flow in the inductor.

For our design, we chose to use R67 = R68 = 15kΩ and R66 = R65 = 1MΩ. The equation for the current limit trip point is

$$I_{LIMIT} = \frac{0.074V}{(0.985)\ (R_{DROOP})}$$

Thus, the current limit may be modified by using different values of R_{DROOP}. Alternatively, the values of resistors R20–R23 may be modified to change the DC reference and the portion of the current sense voltage presented to the comparator. Finally, a 0.1μF capacitor was placed across the inputs of the comparator to reduce the chance of tripping the current limit circuit due to noise. Note that the component numbers in the figure above reference the 2.8V output in the demonstration schematic.

Two notes are useful at this point. First, the selection of schottky diodes should be made based on the average current during short circuit if a shorted output is a likely event. Since the current limit results in a low duty cycle, the schottky diode carries nearly the entire short circuit current. Second, the value of the capacitor placed across the comparator inputs may need to be increased due to variation in PC board layout and component selection.

Thermal Performance Data

Component	2.8V @ 0.5A	2.8V @ 7A	3.3V @ 0.5A	2.8V @ 7A	2.8V Short	3.3V Short
Input Capacitors	25°C	26°C	25°C	26°C	38°C	40°C
Output Capacitors	25°C	30°C	25°C	32°C	38°C	39°C
FET Switches	27°C	43°C	27°C	43°C	78°C	79°C
Schottky Diodes	27°C	47°C	27°C	47°C	106°C	106°C
Inductors	31°C	48°C	31°C	48°C	78°C	95°C
Controller IC	41°C	50°C	41°C	50°C	62°C	62°C

Note: measurements made in still air with a separate current source to avoid heating of components due to conduction of thermal energy from power dissipated in resistive loads. Ambient room temperature was 23°C. Measurements were made with both output channels operating.

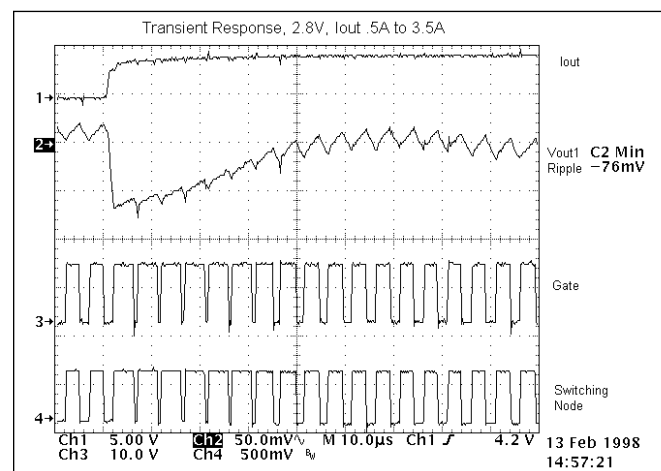# Typical Performance Characteristics
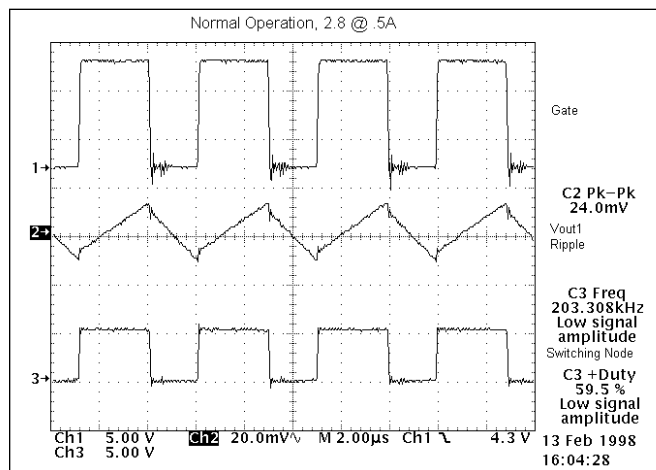
Figure 4.
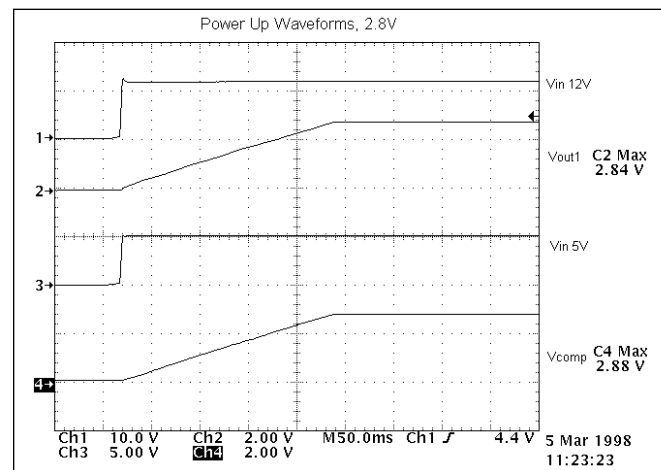
Figure 5.
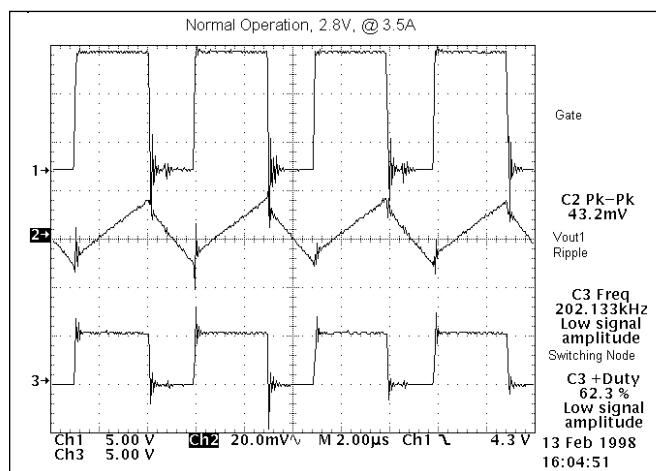
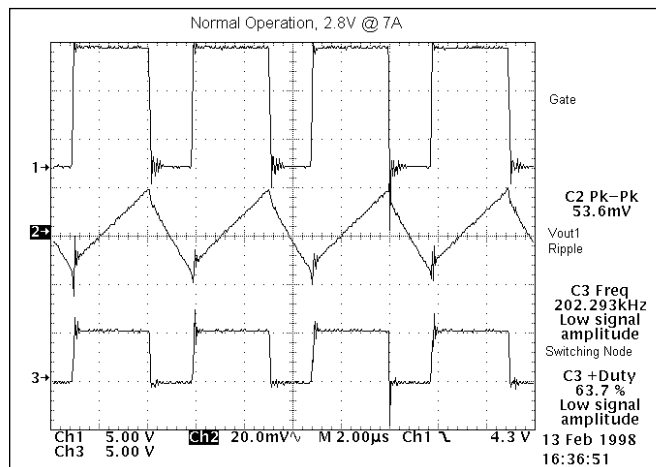

Figure 6.

Figure 7.

Figure 8.

Figure 9.

Typical Performance Characteristics continued

Figure 10.

Figure 13.

Figure 11.
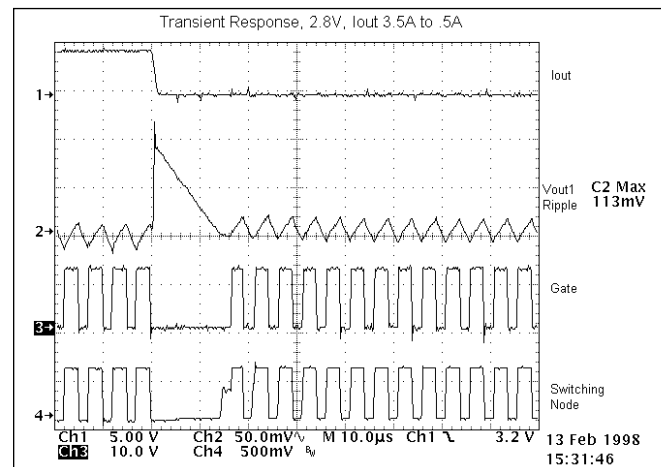

Figure 14.

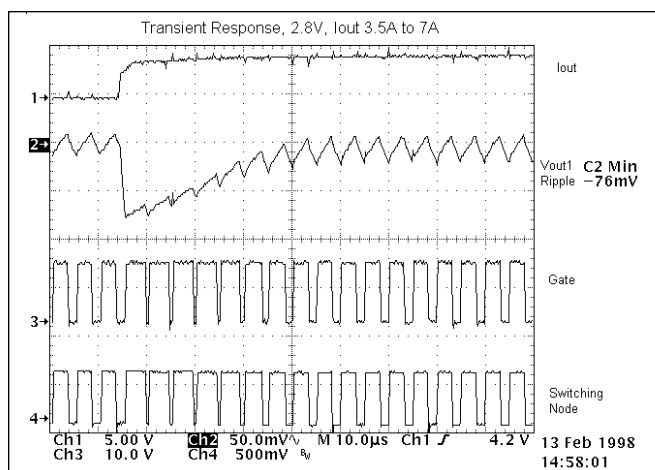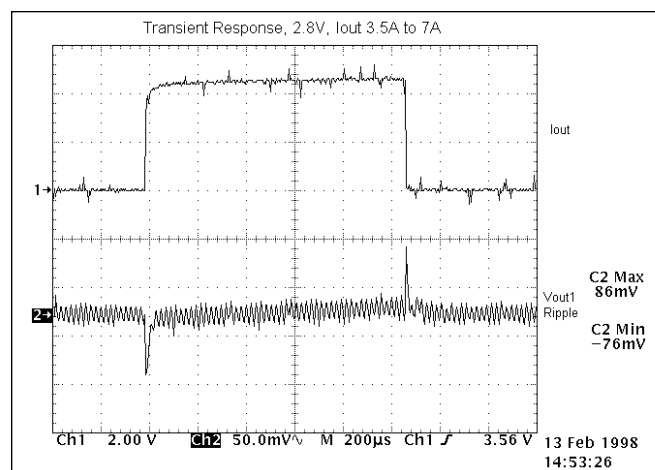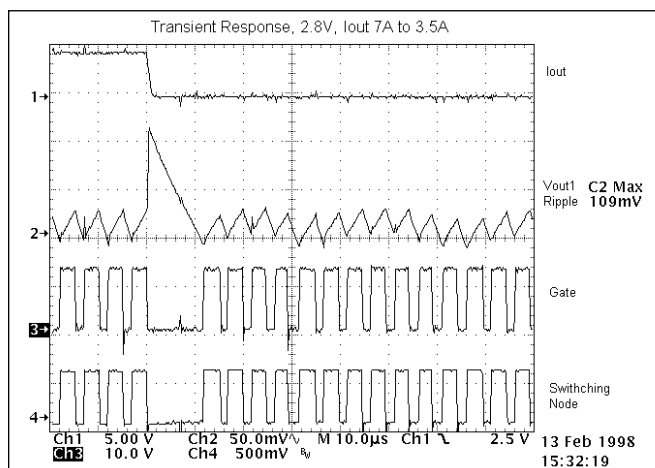**Figure 12.**

Figure 15.

Typical Performance Characteristics continued
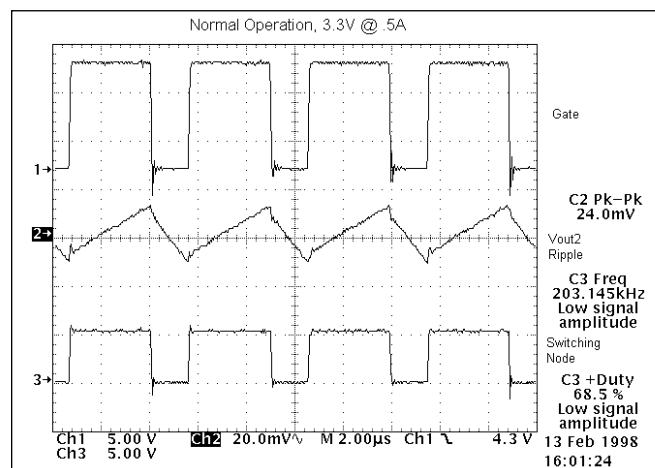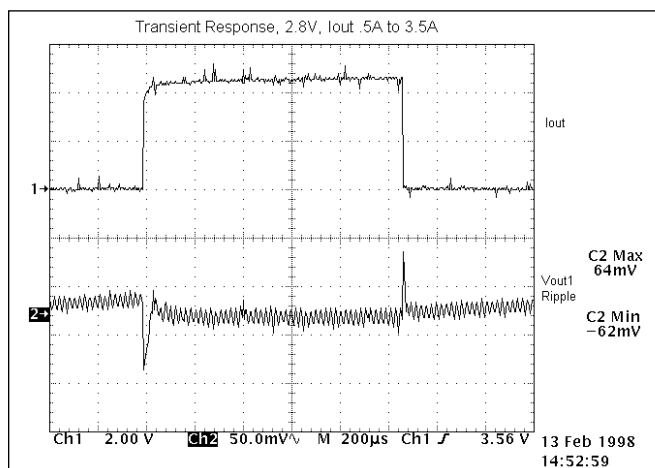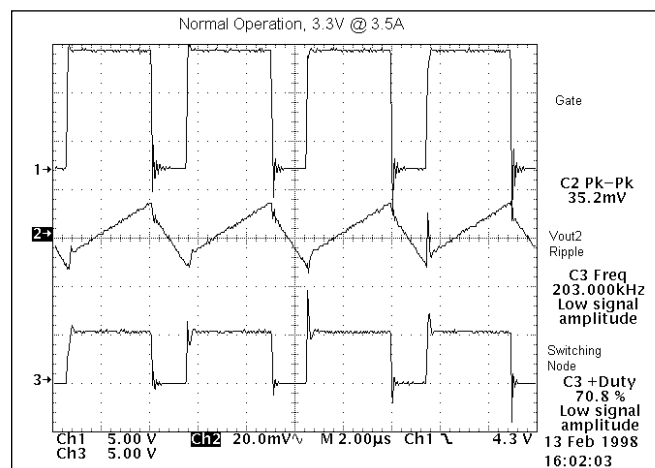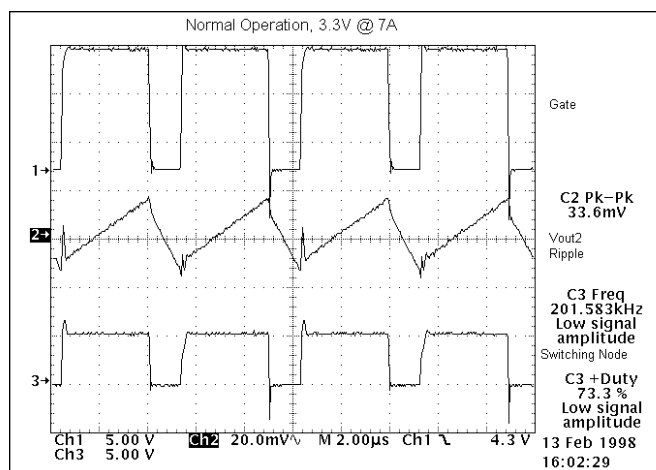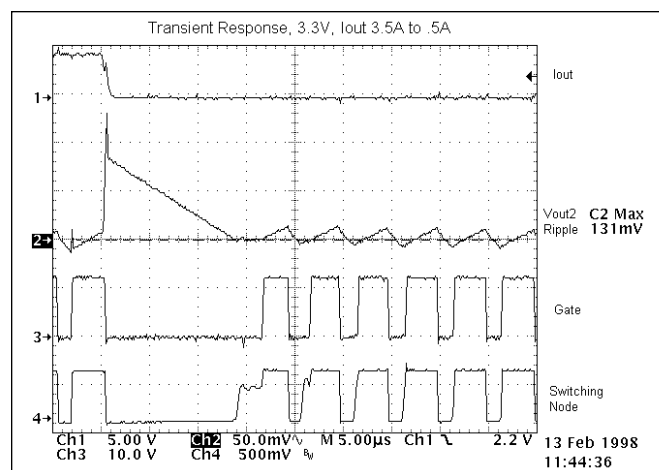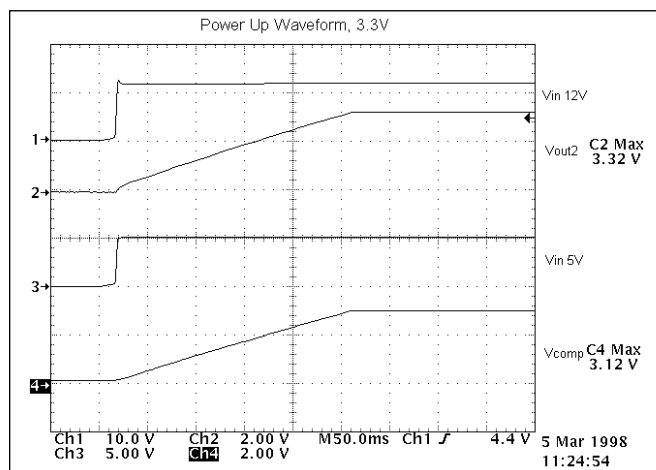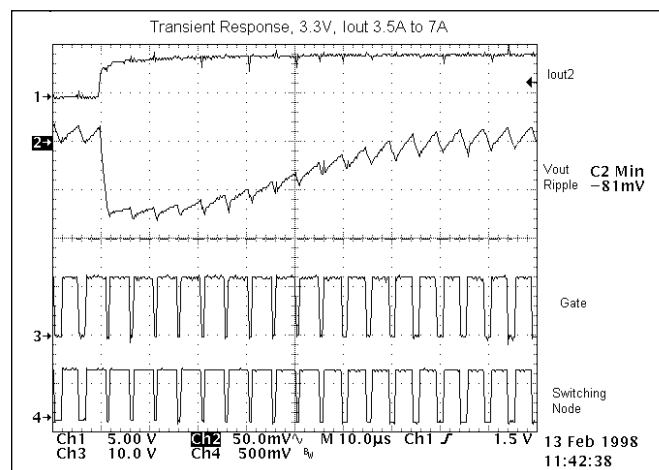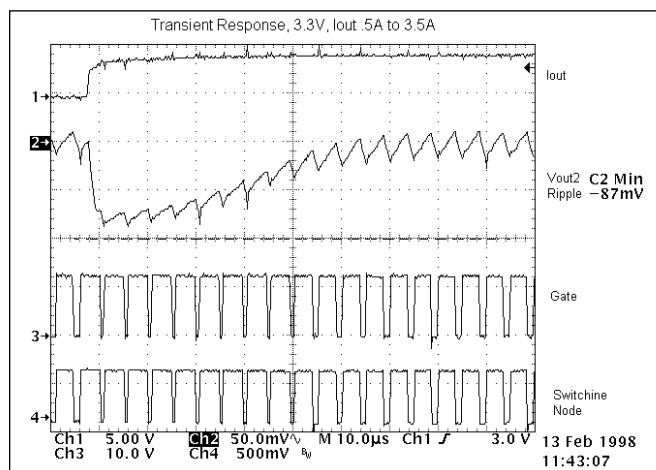

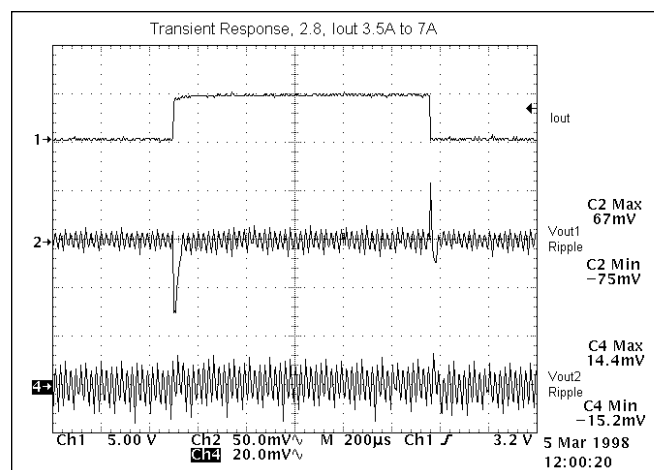Figure 16.

Figure 19.

Figure 17.

Figure 20.

Figure 18.
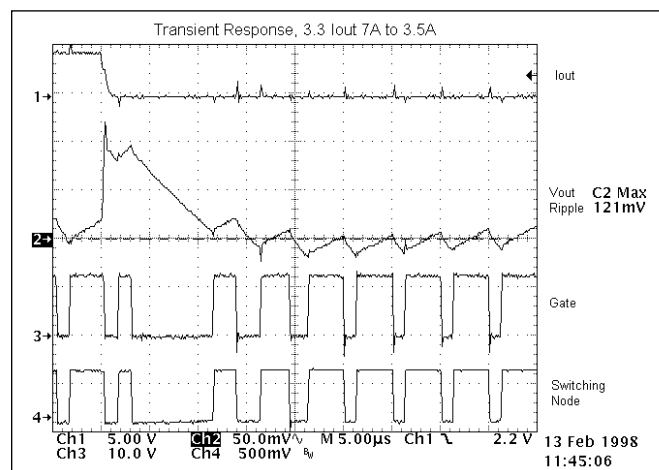
Figure 21.

Typical Performance Characteristics continued
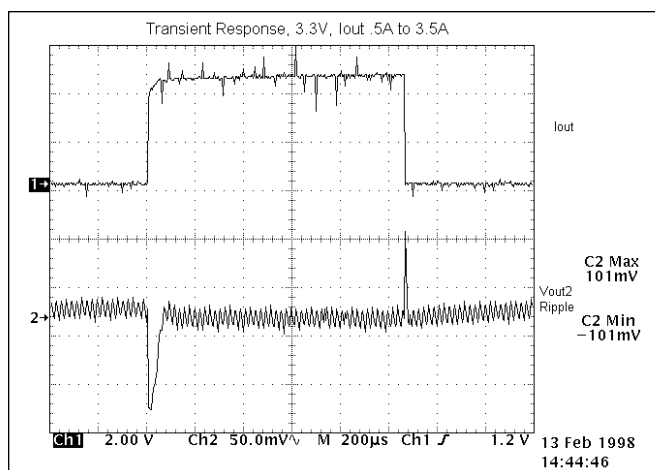
Figure 22.

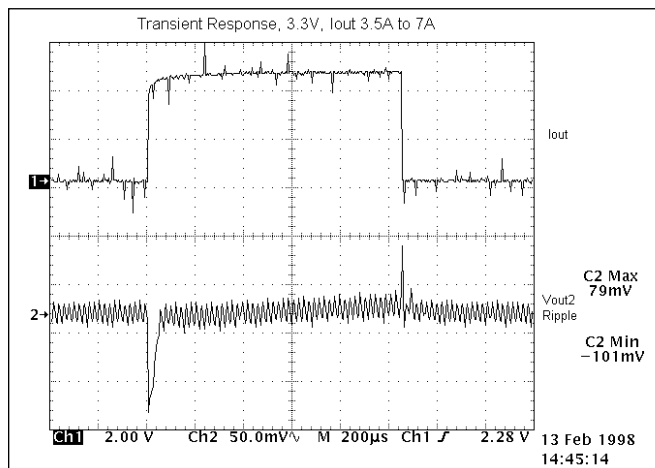Figure 25: Effect of Channel 1 Transient Response on Channel 2 DC Regulation (I_{LOAD} = 500mA).
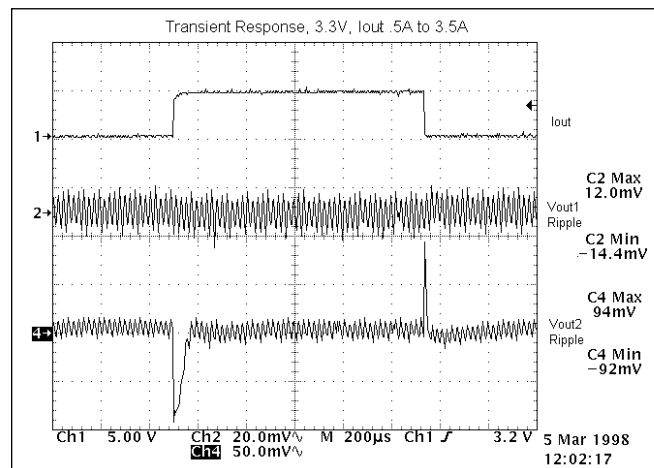

Figure 23.

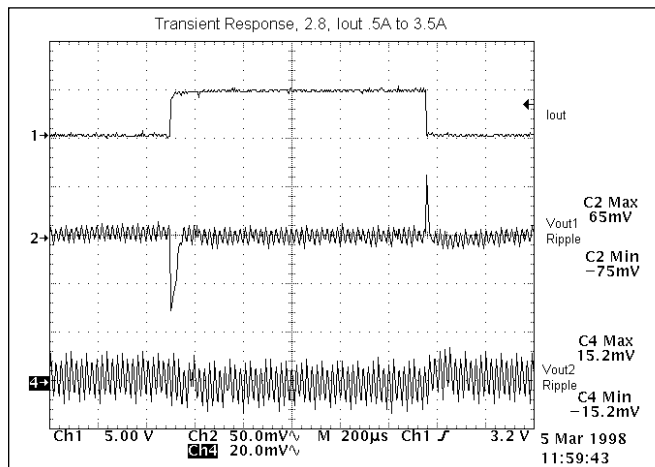Figure 26: Effect of Channel 2 Transient Response on Channel 1 DC Regulation (I_{LOAD} = 500mA).

Figure 24: Effect of Channel 1 Transient Response on Channel 2 DC Regulation (I_{LOAD} = 500mA).
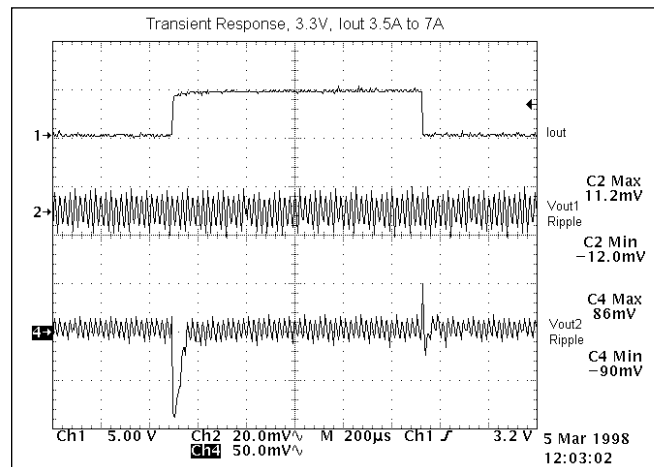

Figure 27: Effect of Channel 2 Transient Response on Channel 1 DC Regulation (I_{LOAD} = 500mA).

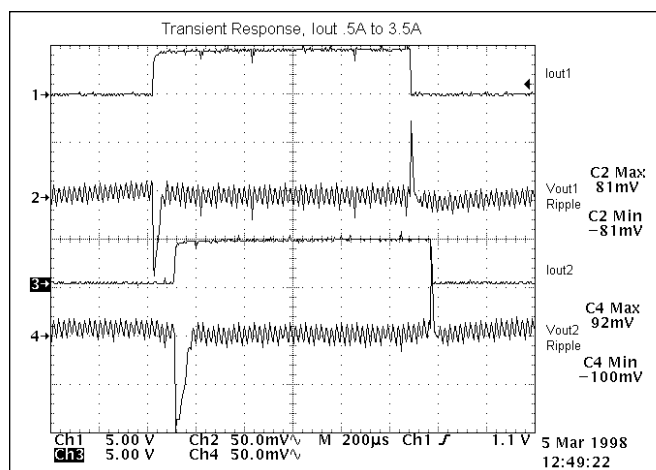# Typical Performance Characteristics continued

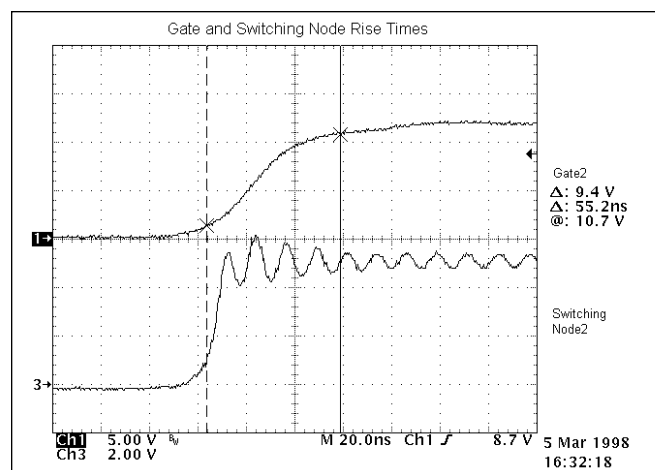Figure 28: Effect of both channels' transient responses (0.5 to 3.5A load step).

Figure 31.
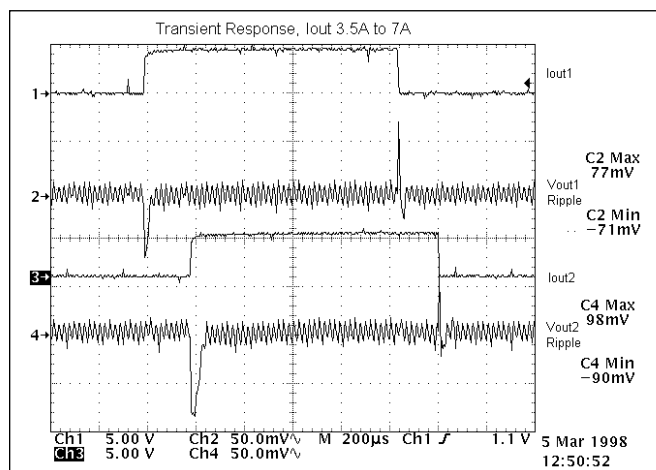

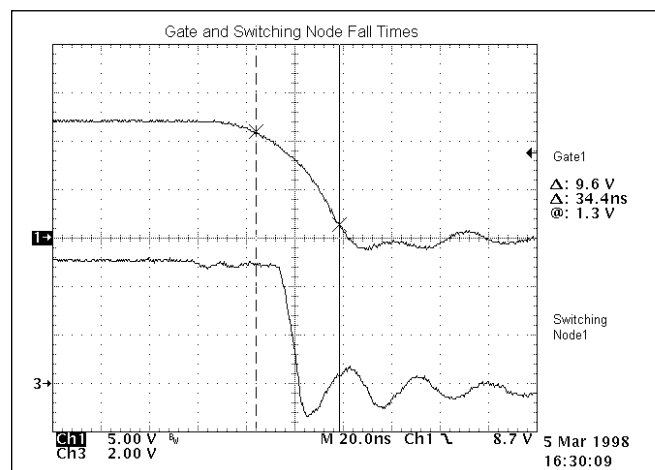Figure 29: Effect of both channels' transient responses (3.5A to 7A load step).
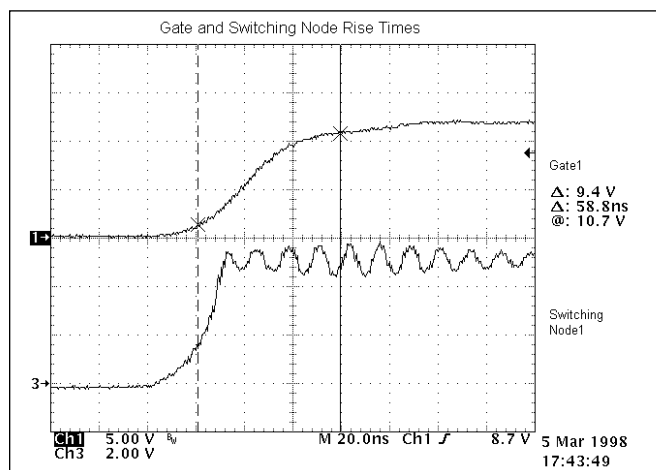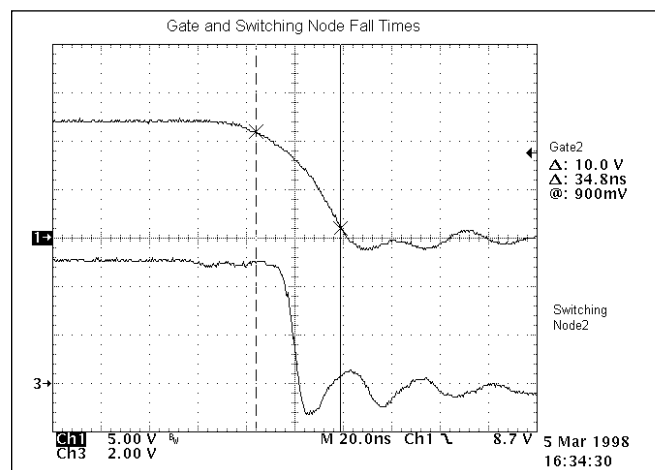

Figure 32.

Figure 30.

Figure 33.

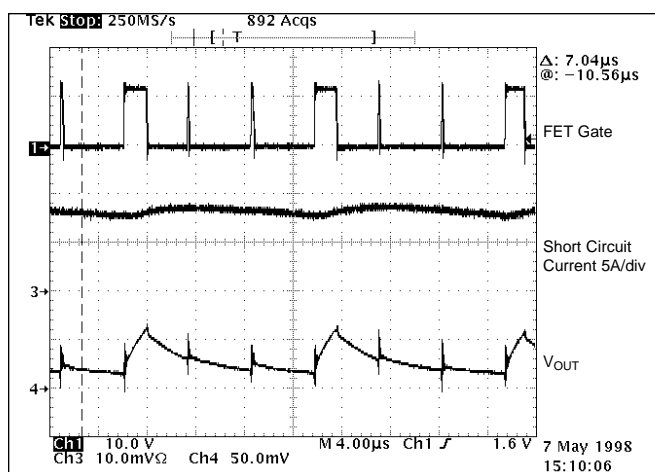# Typical Performance Characteristics continued

Figure 34: 2.8V Current Limit Waveforms.

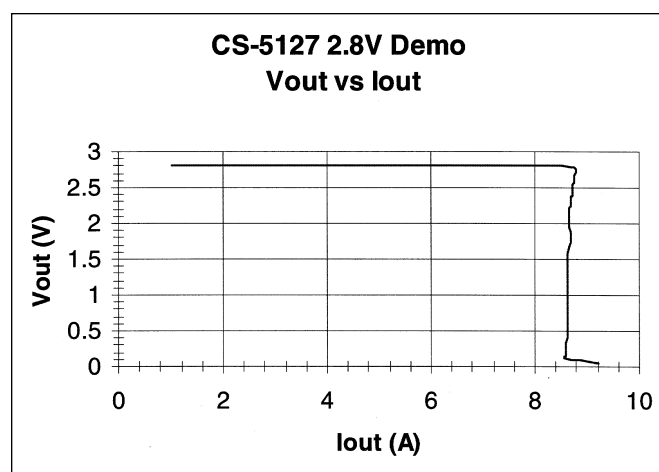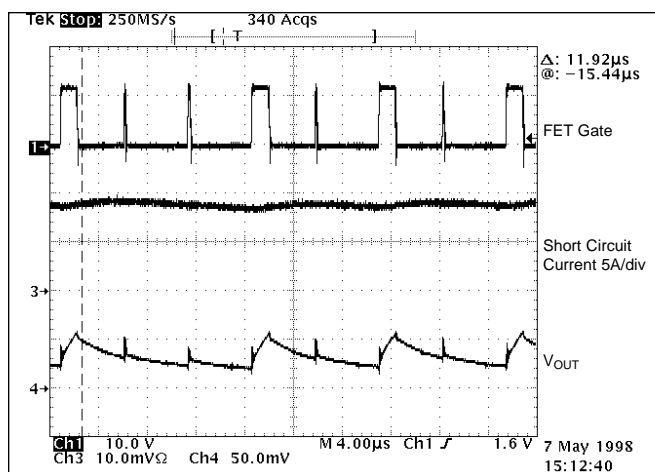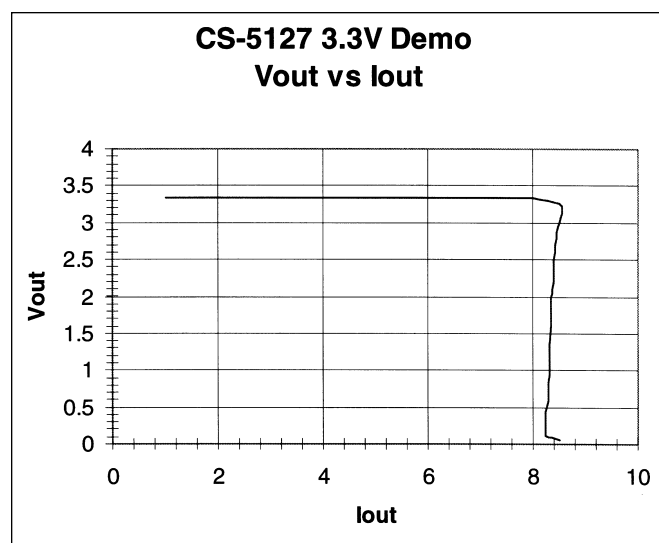Figure 36.

Figure 35: 3.3V Current Limit Waveforms.


Figure 37.

CS5127 Demonstration Board Bill of Materials

Ref. Designator	Manufacturer	Part Number	Value/Desc.	Qty	Website	Telephone
DC/DC Converter						
U1	ON Semiconductor	CS5127DW16*01	Dual Channel V^{2TM} Buck Controller IC	1	www.cherry-semi.com	(800)-272-3601
U4	Texas Instruments	LM2903	Dual Comparator	1	www.ti.com/sc/question	varies, available on website
C1,C2,C4,C5, C10-C13	Panasonic	ECA-1AFQ681	680μF 10V,Radial lead Electrolytic	8	www.panasonic.com	(800)-344-2112
C3,C8	Panasonic	ECS-T1CY105R	1μF 16V Tantalum Electrolytic chip	2	www.panasonic.com	(800)-344-2112
C6,C9,C24,C25	Panasonic	ECH-V1H104KBW	0.1μF 50V Film Chip	4	www.panasonic.com	(800)-344-2112
C14, C17	Panasonic	ECH-V1H331KBW	330pF 50V Film Chip	2	www.panasonic.com	(800)-344-2112
C7	Panasonic	ECH-U1H471JB5	470pF 50V Film Chip	1	www.panasonic.com	(800)-344-2112
C15,C16	Panasonic	ECE-V1AA101UP	100μF 10V Electrolytic	2	www.panasonic.com	(803)-344-2112
R1,R2,R10, R11,R70,R72	Panasonic	ERJ-8GEYJ204	20K 1/8W 5%	6	www.panasonic.com	(800)-344-2112
R3	Panasonic	ERJ-8GEJ184	18K, 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R4	Panasonic	ERJ-8ENF1543	1.54K 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R5	Panasonic	ERJ-8ENF1273	1.27K 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R6, R73, R74	Panasonic	ERJ-8GEJ103	1K 1/8W 5%	3	www.panasonic.com	(800)-344-2112
R7	Panasonic	ERJ-8ENF2403	2.40K 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R8	Panasonic	ERJ-8ENF1503	1.50K 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R9	Panasonic	ERJ-8GEYJ203	2K 1/8W 5%	1	www.panasonic.com	(800)-344-2112
R65,R66,R75, R76	Panasonic	ERJ-8GEYJ106	1MEG 1/8W 5%	4	www.panasonic.com	(800)-344-2112
R67,R68,R77, R78	Panasonic	ERJ-8GEYJ154	15K 1/8W 5%	4	www.panasonic.com	(800)-344-2112
R69, R71	Panasonic	ERJ-8GEYJ104	10K 1/8W 5%	2	www.panasonic.com	(800)-344-2112
R70, R72	Panasonic	ERJ-8GEYJ204	20K 1/8W 5%	2	www.panasonic.com	(800)-344-2112
D1,D2	Lite-On	1N5821	Schottky Diode	2	www.vishay-liteon.com	(602)-302-8056
Q1	ZETEX	MMTB2222A	SOT-23 NPN Transistor	1	www.zetex.com	(516)-543-7100
Q2,Q3	International Rectifier	IRL3103S	N Channel FET	2	www.irf.com	(310)-252-7032
Q4, Q7	Lite-On	MMTB2907A	SOT-23 PNP Transistor	2	www.vishay-liteon.com	(602)-302-8056
L1,L2	Xformers, Inc	XF0066-VO2	5μH Inductor	2	www.xfmrs.com	(800)-344-4539

Note: R$_{DROOP}$ represents the DC resistance of an embedded trace on the PC board. A dedicated resistor may be purchased to reduce board area usage if the cost of the necessary resistor is of lesser importance.

| Ref. Designator	Manufacturer	Part Number	Value/Desc.	Qty	Website	Telephone
Test Circuitry						
C18-C23	Panasonic	ECU-V1H104KBW	0.1μF 50V Film Chip	6	www.panasonic.com	(800)-344-2112
R13,R14,R41,R42	Panasonic	ERJ-8GEYJ203	2K, 1/8 W, 5%	4	www.panasonic.com	(800)-344-2112
R15, R43	Panasonic	ERJ-8GEYJ134	13K, 1/8 W, 5%	2	www.panasonic.com	(800)-344-2112
R19, R47	Panasonic		Film, 6.2Ω, 3W 5%	2	www.panasonic.com	(800)-344-2112

CS5127 Demonstration Board Bill of Materials continued

| Ref. Designator	Manufacturer	Part Number	Value/Desc.	Qty	Website	Telephone
Test Circuitry						
R17,R18,R45,R46	Panasonic	ERJ-8GEYJ102	100Ω, 1/8 W, 5%	4	www.panasonic.com	(800)-344-2112
R12,R16,R40,R44	Panasonic	ERJ-8GEYJ101	10Ω 1/8 W, 5%	4	www.panasonic.com	(800)-344-2112
R21-R39,R49-R64	Panasonic		Film 7.5Ω, 3W 5%	35	www.panasonic.com	(803)-344-2112
Q5,Q6	International Rectifier	IRF7413	N Channel FET	2	www.irf.com	(310)-252-7032
TP1–TP6	Cambion (distributed by Newark Electronics)	40F6023 (Newark stock number)	Turret Pin	6	www.newark.com	(800)-463-9275
J1, J2	Farnell (distributed by Newark Electronics)	583-558 (Newark stock number)	BNC Connector	2	www.newark.com	(800)-463-9275
S1-S6, S8, S9	C & K Components	7101MDRBE	SPDT Switch	8	www.ckcomponents.com	(800)-635-5936
U2, U3	International Rectifier	LM555	Timer IC	2	www.irf.com	(310)-252-7032
J3, J4	Molex	26-48-1065	Straight Friction Lock Connector	2	www.molex.com	(800)-786-6539
S7	C&K Components	T101SHCQE	Switch SPDT	1	www.ckcomponents.com	(800)-635-5936

Printed Circuit Board Layout Information
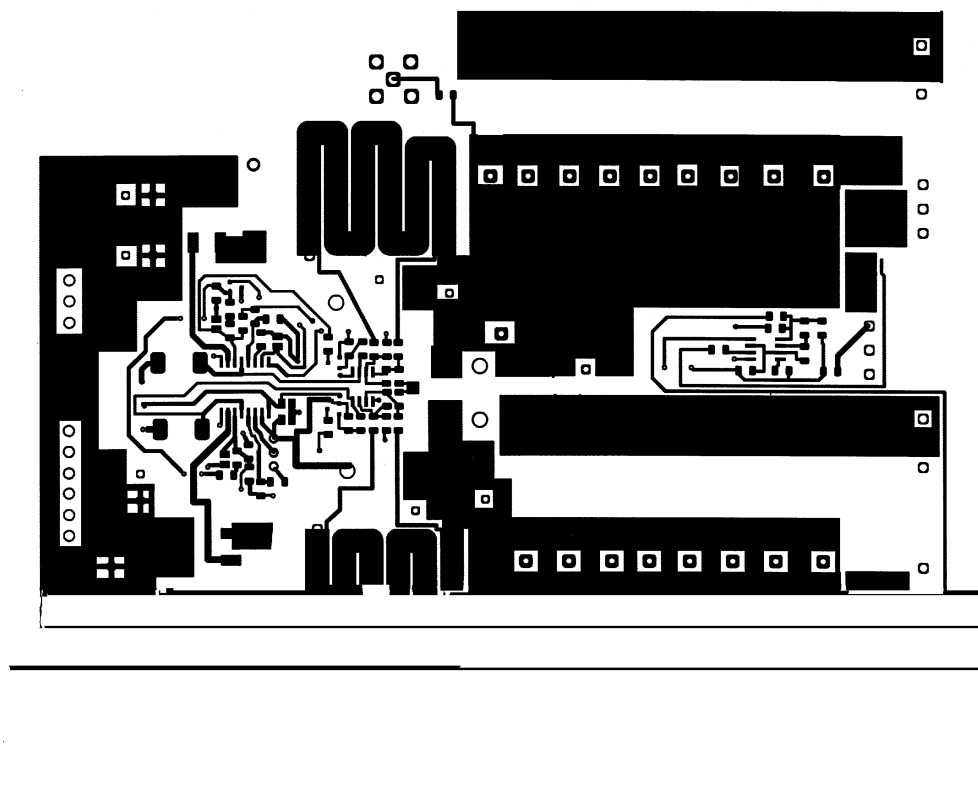
This is the layout pattern for the top layer metal of the printed circuit board for the demonstration.
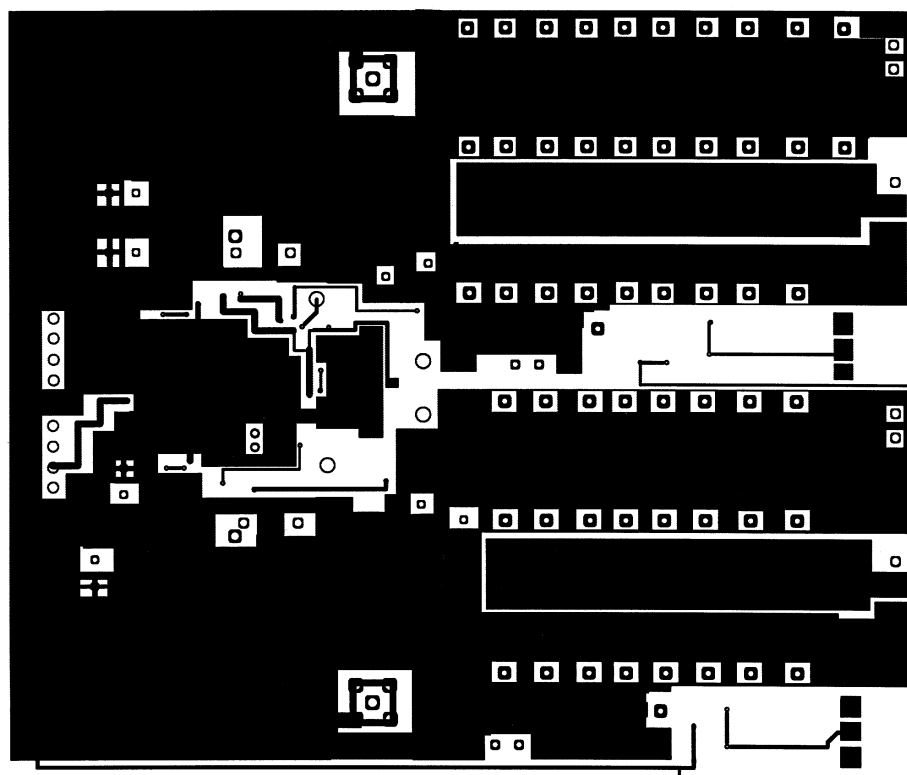
This is the layout pattern for the bottom layer metal of the printed circuit board for the demonstration.

Printed Circuit Board Layout Information continued
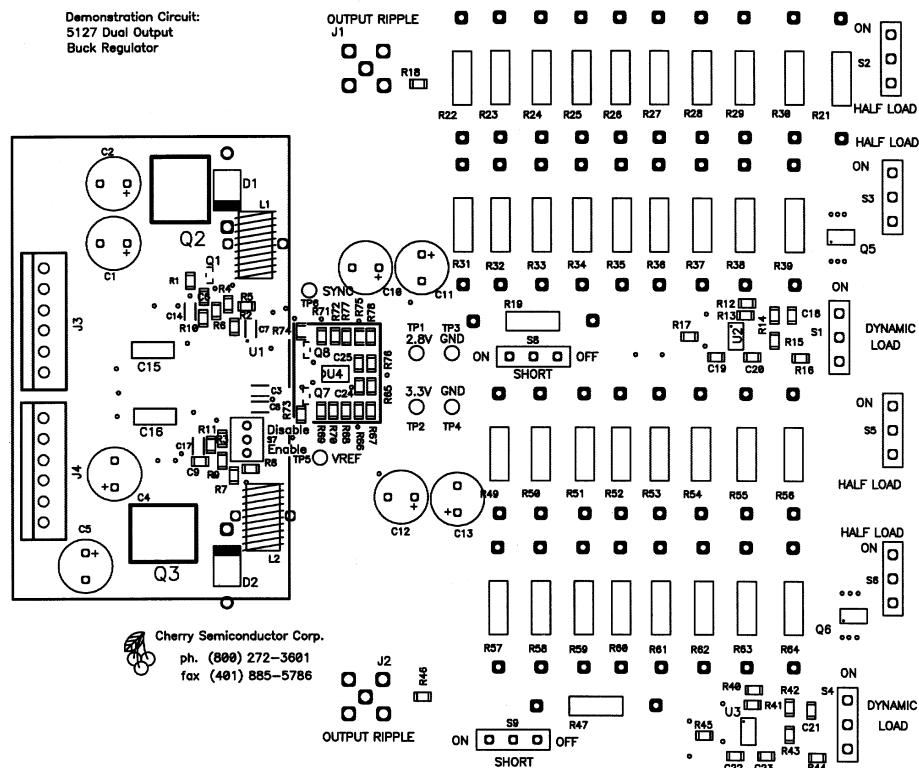
This is the layout pattern for the silkscreen layer of the printed circuit board for the demonstration.

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Notes