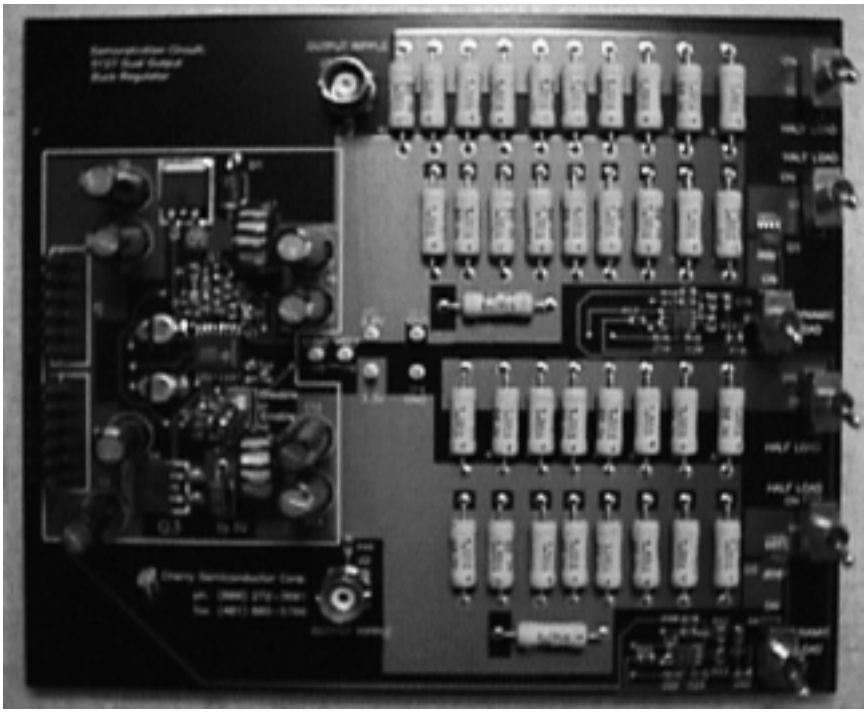
2.8V, 7A and 3.3V, 7A Dual Output Buck Mode Power Supply for V_{CORE} and V_{IO} Motherboard Applications

a CS5127 Demonstration Manual
05/08/98



November, 1998 - Rev. 0
CS5127DM

ON Semiconductor

Description

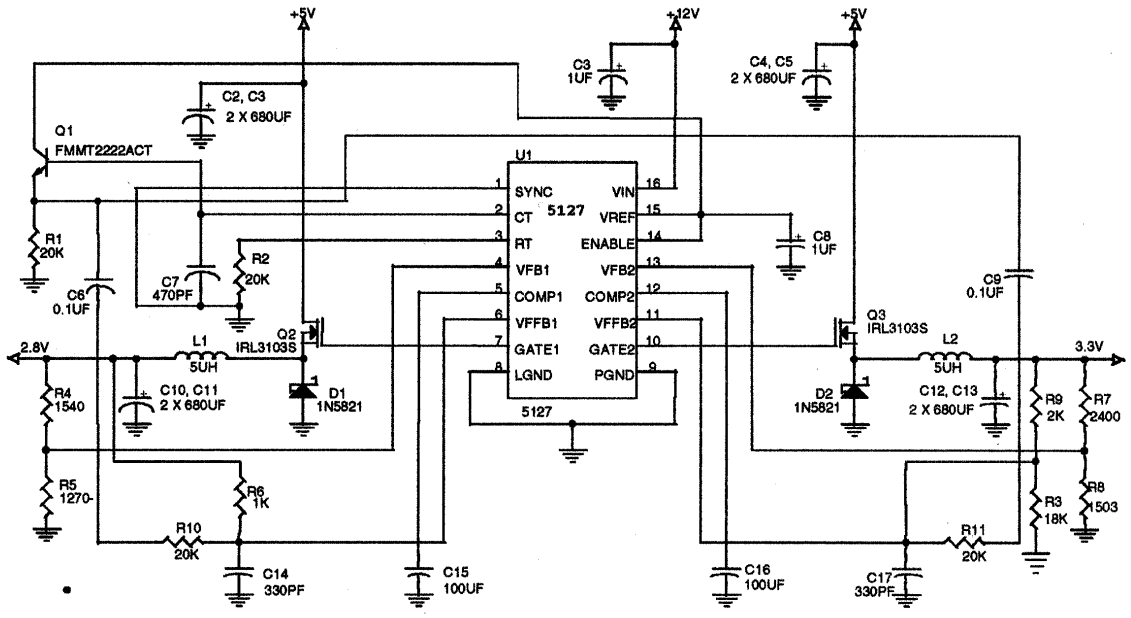
This demonstration circuit showcases a dual output switching power supply. Using a 12V/5V input, two non-synchronous buck controller channels are used to provide separate 3.3V and 2.8V outputs, each capable of supplying 7A. The CS5127 controller IC features the proprietary V^{2TM} control architecture, and provides the fastest transient response available to date in a switch-mode power supply. Use of a single controller IC reduces component count. Additionally, the fixed frequency architecture makes noise minimization easier, since both outputs have the same switching frequency.

Design of the CS5127 was completed with the goal of putting performance and value in the hands of every power supply designer. The external components and printed circuit board layout contained in this demonstration note are optimized for computer motherboard applications. This dual controller is a cost-effective solution for providing V_{CORE} and V_{IO} power solutions in computing applications using a single controller.

Features

- Nonsynchronous buck design
- V^{2TM} control topology
- 100ns transient loop response
- Programmable oscillator frequency
- 55ns typical gate rise and 38ns typical gate fall times
- ENABLE input controls channel 2 gate driver

Application Diagram



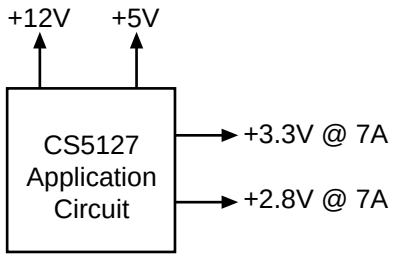
12V, 5V Input to Dual Output 3.3V @ 7A and 2.8V @ 7A for 233MHz Pentium MMX V_{IO} and V_{CORE}

V^2 is a trademark of Switch Power, Inc.

Demonstration Board Description

The CS5127 Demonstration Board is a 7" by 6", two-layer printed circuit board holding both the dual supply and the test circuitry for the supply. The dual supply occupies an area about 2.5" by 3.5", and the test circuitry fills the rest of the board. The test circuitry is capable of exercising the dual supply in a number of ways. Each output channel can be run at minimum load (70mA) DC, half load (3.5A) DC or full load (7.0A) DC. A transient test is also possible, where the load current steps from minimum load to half load or from half load to full load. BNC connectors allow the output waveforms to be viewed with minimum noise pick-up. Standard oscilloscope probes are used to measure all other waveforms.

Application Interface Diagram



Absolute Maximum Ratings

Pin Name	Maximum Voltage	Maximum Current
+5V	+6V / –0.3V	20A (DC)
+12V	+15V / –0.3V	100mA (DC)
$3.3V_{OUT}$	+5V / –0.3V	10A (DC)
$2.8V_{OUT}$	+5V / –0.3V	10A (DC)

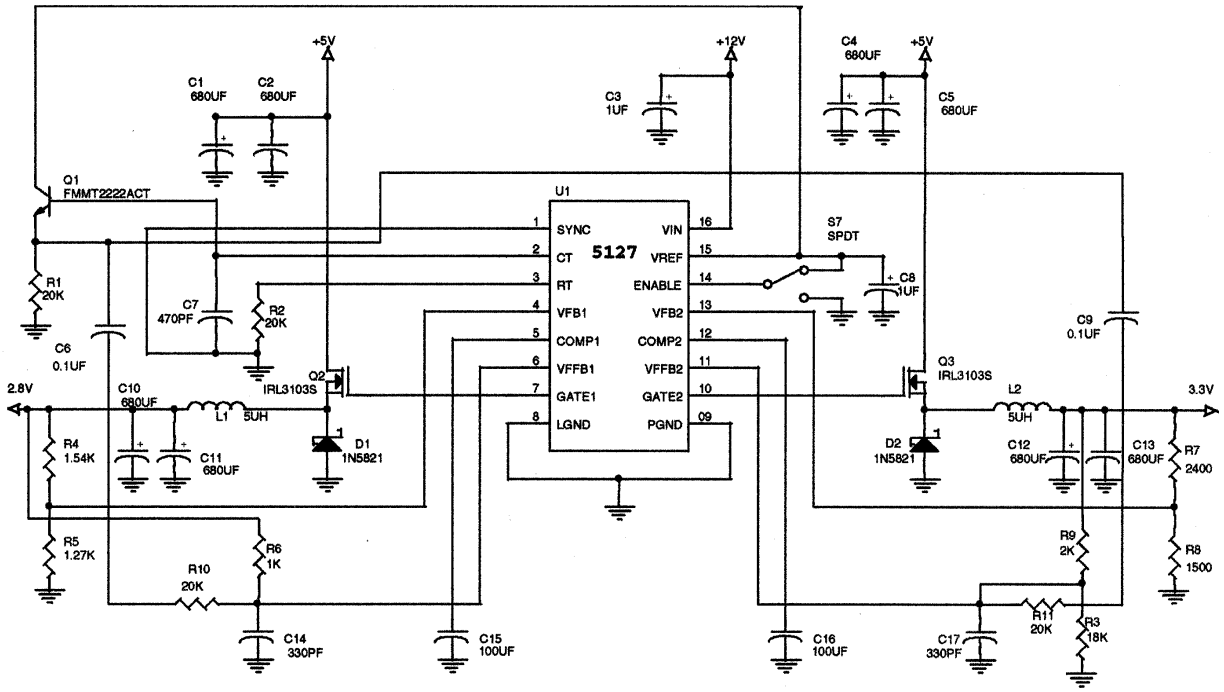
Electrical Characteristics: $0°C \le T_A \le 50°C$, $4.75V \le +5V \le 5.25V$, $11.8V \le +12V \le 13.2V$, I(+5V) = 1A (both channels at minimum load), Unless Otherwise Specified

Parameter	Test Condition	MIN	TYP	MAX	UNITS
3.3V Output					
DC Output Voltage	$500mA \le I_{OUT} \le 7A$	3.23	3.30	3.37	V
AC Voltage Regulation	3.5A load step, scope bandwidth at 20MHz		80		mV
Load Transient Response	I_{SLEW} = 15A / µs, 100Hz TO 100kHz 3.5A load step, scope bandwidth at 20MHz Measure time $3.3V_{OUT}$ exceeds DC limits when 500mA to 3.5A or 3.5A to 7A transient is switched.		10		µs
Ripple and Noise	$500mA \le I_{OUT} \le 7A$, scope bandwidth at 20MHz		40	50	mV_{P-P}
Load Regulation (DC)	$500mA \le I_{OUT} \le 7A$		11	20	mV
+5V Line Regulation	$4.75V \le +5V \le 5.25V$		2	15	mV
Efficiency	$I(3.3V_{OUT})$ = 7A		89		%
2.8V Output					
DC Output Voltage	$500mA \le I_{OUT} \le 7A$	2.74	2.80	2.86	V
AC Voltage Regulation	3.5A load step, scope bandwidth at 20 MHz		80		mV

Absolute Maximum Ratings continued

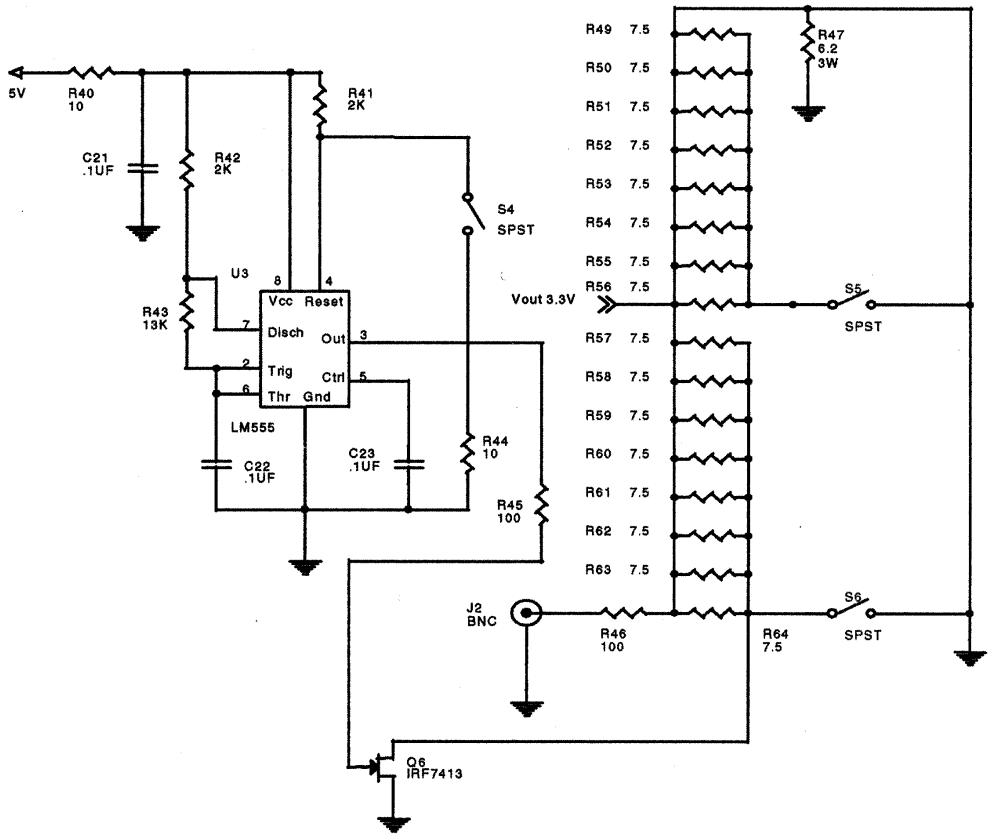
Electrical Characteristics: 0°C ≤ T_A ≤ 50°C, 4.75V ≤ +5V ≤ 5.25V, 11.8V ≤ +12V ≤ 13.2V, I(+5V) = 1A (both channels at minimum load), Unless Otherwise Specified					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**UNITS**
2.8V Output continued					
Load Transient Response	I_{SLEW} = 15A / µs, 100Hz TO 100kHz		10		µs
	3.5A load step, scope bandwidth at 20MHz Measure time $3.3V_{OUT}$ exceeds DC limits when 500mA to 3.5A or 3.5A to 7A transient is switched.				
Ripple and Noise	500mA ≤ I_{OUT} ≤ 7A, scope bandwidth at 20MHz		40	50	mV_{P-P}
Load Regulation (DC)	500mA ≤ I_{OUT} ≤ 7A		11	20	mV
+5V Line Regulation	4.75V ≤ +5V ≤ 5.25V		2	15	mV
Efficiency	I($3.3V_{OUT}$) = 7A		86		%
+12V Input					
+12V Bias Current			22	30	mA
+12V Turn-on Voltage		7.4	8.4	9.4	V
+12V Turn-off Voltage		6.8	7.8	8.8	V
+12V Lockout Hysteresis			0.6		V
ENABLE Pin					
Channel 2 Duty Cycle	Enable pin grounded			0	%
	Enable pin tied to V_{REF}		55		%

Demonstration Board Schematic

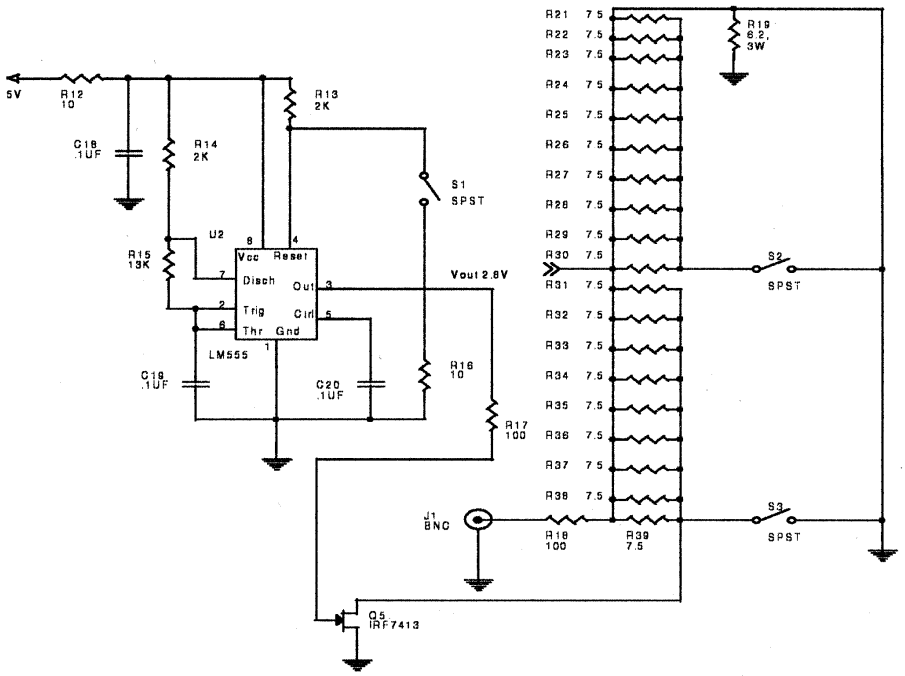


This is the application portion of the demonstration board. It shows the component reference designators corresponding to the printed circuit board layout and bills of materials that are included in this document.

Demonstration Board Schematic continued



This schematic shows the test circuitry for the 3.3V output (channel 2). Reference designators correspond to the printed circuit board layout and the bill of materials.



This schematic shows the test circuitry for the 2.8V output (channel 1). Reference designators correspond to the printed circuit board layout and the bill of materials.

Demonstration Board Operation Guidelines

No specialized equipment is required to exercise the CS5127 demonstration board. A “silver box” computer power supply and an oscilloscope with two BNC cable inputs are the only requirements.

Seven switches control the test modes for the CS5127 demonstration board. Switch S7 controls the ENABLE/DISABLE status of output channel 2 (3.3V output). Three switches for each output channel control DC current level and load transient testing. Switches S1, S2 and S3 control channel one, while switches S4, S5 and S6 control channel two testing. A list of test conditions and switch configurations is provided below. Testing of channel one is completely independent of testing of channel two, and both channels can be tested at full load simultaneously. An “X” in a column indicates a don’t care condition.

Test Condition	S1	S2	S3	S4	S5	S6	S7
Output 1, 450mA DC	OFF	OFF	OFF	X	X	X	X
Output 1, 3.4A DC	OFF	ON	OFF	X	X	X	X
Output 1, 6.4A DC	OFF	ON	ON	X	X	X	X
Output 1, 450mA to 3.4A transient	ON	OFF	OFF	X	X	X	X
Output 1, 3.4A to 6.4A transient	ON	ON	OFF	X	X	X	X
Output 2 disabled	X	X	X	X	X	X	DISABLE
Output 2, 530mA DC	X	X	X	OFF	OFF	OFF	ENABLE
Output 2, 4.05A DC	X	X	X	OFF	ON	OFF	ENABLE
Output 2, 7.57A DC	X	X	X	OFF	ON	ON	ENABLE
Output 2, 530mA to 4.05A transient	X	X	X	ON	OFF	OFF	ENABLE
Output 2, 4.05A to 7.57A transient	X	X	X	ON	ON	OFF	ENABLE

As an example, if channel one was providing 3.4A DC while channel 2 was responding to a 530mA to 4.05A load step, switch settings would be:

	OFF	ON	OFF	ON	OFF	OFF	ENABLE

Design Procedure

Note: component reference designators contained in the Design Procedure refer to the Demonstration Board Schematic.

In order to begin designing a power supply using the CS5127, we must define the topology we wish to use, the supply voltages, the output voltage and current requirements and the switching frequency. Using the guidelines contained in the CS5127 data sheet, we chose to build a V^{2TM} controlled regulator. We chose to use a standard computer "silver box" power supply with both 12V and 5V outputs. The 12V supply provides the IC bias and the 5V supply provides the input power. Our regulator outputs were set at 3.3V and 2.8V, and both outputs can supply 7A to their loads. We chose a target switching frequency of 200kHz.

Choosing the Oscillator Components

We chose a switching frequency of 200kHz. We arbitrarily chose C7 = 470pF for small size and low cost. R2 can now be calculated:

$$R2 = \frac{1.88}{(200kHz)\ (470pF)} = 20k\Omega$$

Choosing the Feedback Resistor Values

We first considered how to size R5 and R8. If each resistor is set to conduct 1mA, the V_{FB} pin bias current of 1mA will cause an error less than 0.1%. We chose a 1270W, 1%, 1/8W chip resistor. Thus, current in the divider is approximately

$$I_{V(FB)} = \frac{1.275}{1270} = 1.004\ mA,$$

and expected error is

$$E = \frac{(1E-6)\ (1270)\ (100\%)}{1.275} = 0.0996\%.$$

For the 2.8V output, we calculated the value of R4:

$$R4 = 1270 \times \left[\frac{2.8}{1.275} - 1\right] = 1519\Omega.$$

Use a standard value of 1540Ω.

For the 3.3V output, we calculated the value of R7:

$$R7 = 1270 \times \left[\frac{3.4}{1.275} - 1\right] = 2017\Omega.$$

Use a standard value of 2000Ω or 2050Ω.

Unfortunately, when we checked, we didn't have either value in stock. We looked for a good fit using values we did have, and found that setting R8 = 1500Ω gave a value of 2382Ω for R7. We used R7 = 2400Ω. The error from setting R8 = 1500Ω is

$$E = \frac{(1E-6)\ (1500)\ (100\%)}{1.275} = 0.118\%.$$

Choosing the Inductors

We first solved for the 2.8V output minimum inductance value. We decided to set I_{MAX} = 10A as a limit for the inductor saturation current. This gave

$$L_{MIN} = \frac{(5V-2.8V)\ (2.8V)}{(200kHz)\ (10A)\ (5V)} = 0.6\mu H.$$

For this inductor, ripple current was calculated as

$$I_{RIPPLE} = \frac{(5V-2.8V)\ (2.8V)}{(200kHz)\ (0.6\mu H)\ (5V)} = 10.27A.$$

Increasing the inductance reduces the ripple current, so we tried 5µH:

$$I_{RIPPLE} = \frac{(5V-2.8V)\ (2.8V)}{(200kHz)\ (5\mu H)\ (5V)} = 1.232A.$$

This is much more realistic.

We then calculated the maximum output current using the 5µH inductor.

$$I_{OUT(MAX)} = 10A - \frac{(5V-2.8V)\ (2.8V)}{(2)\ (200kHz)\ (5\mu H)\ (5V)} = 9.38A.$$

This is adequate for our needs.

We then solved for the 3.3V output inductor:

$$L_{MIN} = \frac{(5V-3.3V)\ (3.3V)}{(200kHz)\ (10A)\ (5V)} = 0.56\mu H.$$

For this inductor, ripple current was calculated as

$$I_{RIPPLE} = \frac{(5V-2.8V)\ (2.8V)}{(200kHz)\ (056\mu H)\ (5V)} = 10.02A.$$

We tried 5µH again:

$$I_{RIPPLE} = \frac{(5V-3.3V)\ (3.3V)}{(200kHz)\ (5\mu H)\ (5V)} = 1.122A.$$

$$I_{OUT(MAX)} = 10A - \frac{(5V-3.3V)\ (3.3V)}{(2)\ (200kHz)\ (5\mu H)\ (5V)} = 9.44A.$$

Design Procedure continued

Thus, both inductors should be 5µH and rated for 10A. We chose the XF0066-VO2 from XFMRS, Inc. for both L1 and L2.

Choosing the Output FETs

We looked for an inexpensive logic level n-channel FET. Logic level is desirable in this application since there is only 7V of gate drive available, and 1.5V of that is used in the CS5127 output drivers. We wanted the FET to withstand a minimum of 15V and have current carrying capability of at least 10A. Additionally, low $R_{DS(ON)}$ and surface mount packaging were important. We chose the IRL3103S from International Rectifier for Q2 and Q3. The IRL3103S is a logic level n-channel FET capable of withstanding 30V, carrying 64A with $R_{DS(ON)}$ of 14mΩ, and the D^2 package features θ_{JA} of 40°C / W.

Choosing the Catch Diodes

These components are usually schottky diodes to minimize the forward voltage drop and improve system efficiency. The diodes are chosen based on reverse voltage, average current capability and turn-on voltage. In this application, the maximum reverse voltage that will be experienced by the catch diodes is V_{IN} plus some tolerance, or about 14V. The average current in the catch diode is given as

$$I_{D(AVE)} = I_{LOAD} \times \frac{V_{SUPPLY} - V_{OUT}}{V_{SUPPLY}}$$

This comes out to about 3.1A for the 2.8V output and 2.4A for the 3.3V output. We chose to use the 1N5821 from LiteOn Power Semiconductor for D1 and D2. This diode has a 3A average current rating, a withstand voltage of 30V and a turn-on voltage of 0.5V.

Choosing the Output Capacitors

We based our choice for output capacitors on four considerations: RMS ripple current rating, ESR, size and price. The capacitor network must be capable of handling the inductor ripple current of 1.2A. The ripple current flowing in the capacitor ESR will produce the output ripple voltage. Our demonstration board accepts its power through two standard J-connectors, so the capacitor height should be lower than the height of the connectors, and price should be as low as possible. We chose to use two Panasonic ECA-1AFQ681 capacitors in parallel for each output (C10, C11, C12, C13). These capacitors have a ripple current rating of 760mA and typical ESR of 90mΩ. Two capacitors in parallel give 1.5A of ripple current capability and ESR of 45mΩ. The ripple current into the ESR will produce about 55mV of output ripple voltage.

A load step will produce an instantaneous change in the output voltage defined by the magnitude of the load step and the output capacitor ESR. Our test setup produces a 3.5A load step. The worst case change in output voltage due to the load step will be

$$\Delta V_{OUT} = \Delta I_{OUT} \times ESR = (3.5A)\ (0.045\Omega) = 0.158V.$$

Choosing the Input Bypass Capacitors

We chose bypass capacitors for the FET drains with the same criteria used for the output capacitors. In this case, though, the ripple current during switch transitions is much larger:

$$I_{RIPPLE} = I_{OUT}\sqrt{\frac{(V_{IN} - V_{OUT})\ (V_{OUT})}{V_{IN}^2}} = 3.48A$$

However, the current “spikes” during the switch transitions are of very short duration. A voltage spike at the transition is defined as:

$$\Delta V = (ESR)\ (I_{RIPPLE}) = 0.157V$$

This momentary glitch introduces noise but does not otherwise impact system operation. The other component of ripple current in the input bypass capacitors is due to the inductor ripple current and has the same magnitude of about 1.2A. We chose to use the same capacitor type and value for the input bypass caps that we used for the output capacitors. We placed two Panasonic ECA-1AFQ681 capacitors (C1, C2, C4, C5) in parallel right at the drain of each FET. These capacitors help to minimize EMI and reduce ripple current in the 5V supply. We also chose to include bypass capacitors on the V_{IN} and V_{REF} lines of the IC (C3, C8). At 200kHz, a 1µF capacitor presents an impedance of 0.8Ω which should conduct any switching noise.

Choosing the COMP Pin Capacitors

We chose to impose a 0.1% tolerance on the DC level of the COMP pin voltage. At 200kHz, T_{OSC} = 5µs, and

$$C_{COMP(MIN)} = \frac{(0.016A)\ (5E-6s)}{(2.8V)\ (0.001)} = 28.6\mu F$$

$$C_{COMP(MIN)} = \frac{(0.016A)\ (5E-6s)}{(3.3V)\ (0.001)} = 24.2\mu F$$

We chose to use 100µF capacitors for C15 and C16 as recommended by the datasheet. Increasing the COMP pin capacitor value improves noise immunity.

Choosing the V_{FFB} Pin Components

We started by determining how the DC bias would be provided. The 2.8V output is low enough to provide DC bias to the V_{FFB1} pin, but the 3.3V output is very near the PWM comparator common mode maximum input voltage. We chose to use a resistor divider to provide the DC bias for the 3.3V output. We set the total divider resistance at 20kΩ between the 3.3V output and ground. This sets the divider current at 165µA. We chose to set the DC bias voltage at about 3V, so our divider resistors can be calculated:

$$R3 = 20k\Omega \times \frac{(3.0V)}{(3.3V)} = 18k\Omega, \text{ and}$$

$$R9 = 20k\Omega - 18k\Omega = 2k\Omega.$$

This ratio keeps 90% of the output voltage ripple as input to the V_{FFB} pin so that V^2 control will function properly. R9 also serves as the filter resistor for the 3.3V output.

We chose to use identical 330pF capacitors for V_{FFB} filter capacitors C14 and C17, and we set R6 equal to 1K. This gives cutoff frequencies of 3MHz for the 2.8V output and of 1.5MHz for the 3.3V output. This effectively removes switching noise from the V_{FFB} bias levels.

To provide the artificial ramp signal, we chose a SOT-23 packaged NPN transistor for Q1. We used Zetex's FMMT2222A transistor. This transistor can provide as much as 600mA of current and has a forward current gain (H_{FE}) between 100 and 300. It is important to have a fairly high gain so that the transistor does not load down the CT pin capacitor. Such loading will decrease the switching frequency.

The CS5127 datasheet provides the CT pin peak and valley thresholds for the oscillator. We used the peak threshold of 3.6V to help us determine the maximum bias current for Q1. Assuming $V_{BE(ON)}$ for Q1 is 700mV, the maximum emitter voltage for the transistor will be 3.6V – 0.7V = 2.9V. We arbitrarily chose to use a 20K resistor for R1. This sets the maximum quiescent current for Q1 at 145µA. If forward current gain is 100, the current load on the CT pin due to Q1 is about 1.5µA. The error introduced by this loading can be approximately calculated as

$$E_{FREQ} = \frac{R2}{(R1)\ (H_{FE})},$$

where H_{FE} is the forward current gain of the transistor at the DC bias current level.

For our circuit, E_{FREQ} is less than 1%.

We use 2 capacitors to couple the artificial ramp signal into the V_{FFB} pins. Ideally, these capacitors present as low a resistance as possible at the switching frequency so that the full amplitude of the voltage signal at Q1's emitter is present on the V_{FFB} side of the capacitor. We chose C6 and C9 at 0.1µF. At 200kHz, this value represents a resistance of about 8Ω.

We now need to calculate the amount of artificial ramp needed to stabilize our system. For the 2.8V output,

$$V_{RAMP} = \frac{(0.045\Omega)\ (2.8V)}{(2000)\ (5\mu H)} = 12.6mV \text{ per period.}$$

However, we must add the output voltage ripple to this value to calculate the value of R10:

$$R_{RAMP} = (1k\Omega)\left[\frac{2.1V}{57.6mV} - 1\right] = 35k\Omega.$$

Use a standard value of 33kΩ.

When we tried this resistor value, we observed some minor pulse skipping. Decreasing R10 to 27K eliminated the pulse skipping, and further decreasing R10 to 20K did not affect transient response. We chose 20kΩ for a final value.

For the 3.3V output,

$$V_{RAMP} = \frac{(0.045\Omega)\ (3.3V)\ (18K)}{(2000)\ (5\mu H)\ (20K)} = 13.4mV \text{ per period.}$$

$$R_{RAMP} = (2k\Omega)\left[\frac{2.1V}{59.9mV} - 1\right] = 68k\Omega.$$

This resistor value for R11 also resulted in some pulse skipping. Decreasing the resistor value to 27kΩ again eliminated the problem, and decreasing the value to 20kΩ did not affect transient response. We chose 20kΩ as the final value.

With this calculation, our converter design was complete. As noted above, some optimization was required for the values of R10 and R11, but system performance is otherwise good.

Thermal Performance Data

Component	2.8V @ 0.5A	2.8V @ 7A	3.3V @ 0.5A	2.8V @ 7A
Input Capacitors	25°C	26°C	25°C	26°C
Output Capacitors	25°C	30°C	25°C	32°C
FET Switches	27°C	43°C	27°C	43°C
Schottky Diodes	27°C	47°C	27°C	47°C
Inductors	31°C	48°C	31°C	48°C
Controller IC	41°C	50°C	41°C	50°C

Note: measurements made in still air with a separate current source to avoid heating of components due to conduction of thermal energy from power dissipated in resistive loads. Ambient room temperature was 23°C. Measurements were made with both output channels operating.

Typical Performance Characteristics

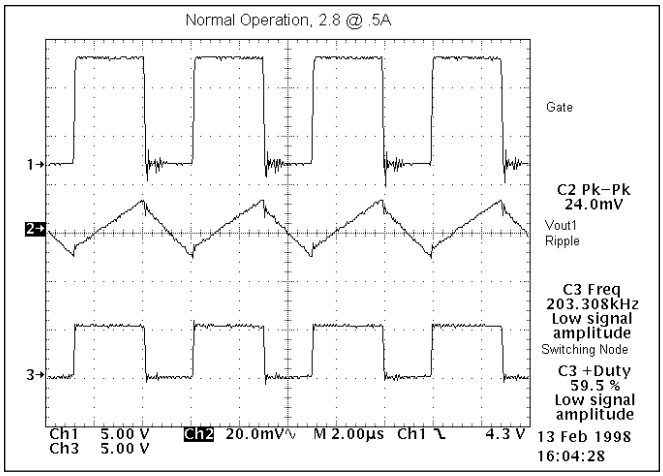


Figure 1.

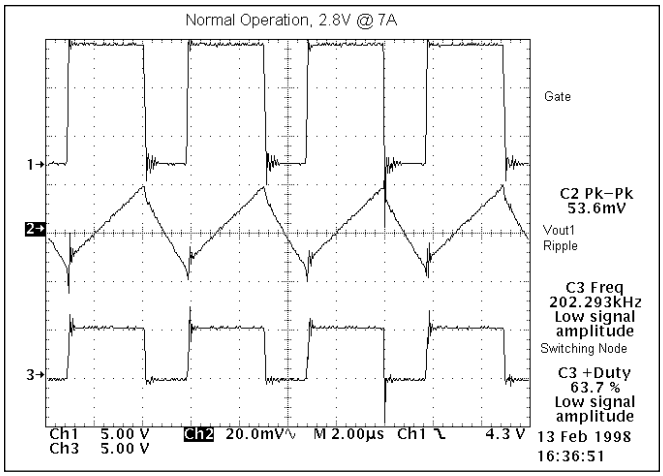


Figure 3.

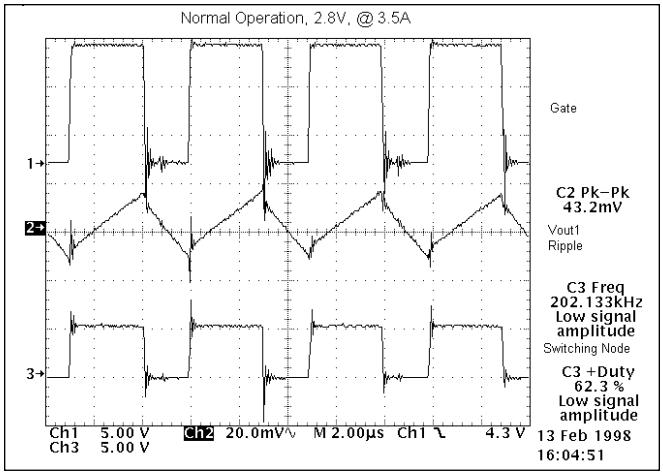


Figure 2.

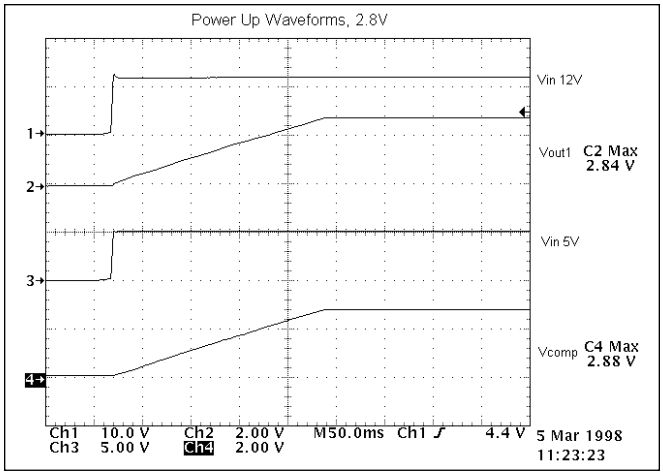


Figure 4.

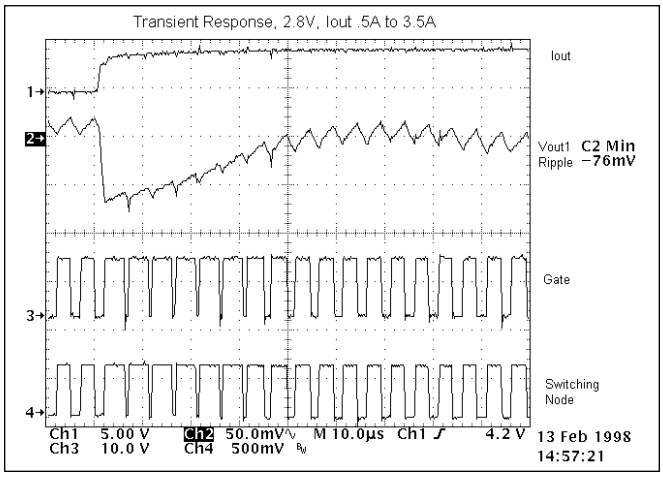


Figure 5.

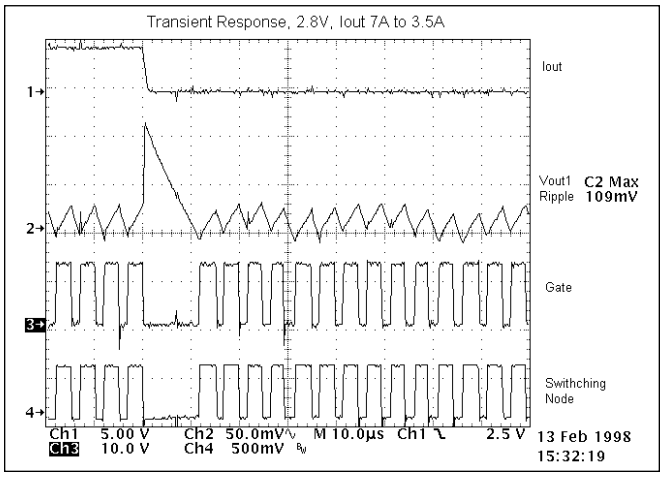


Figure 8.

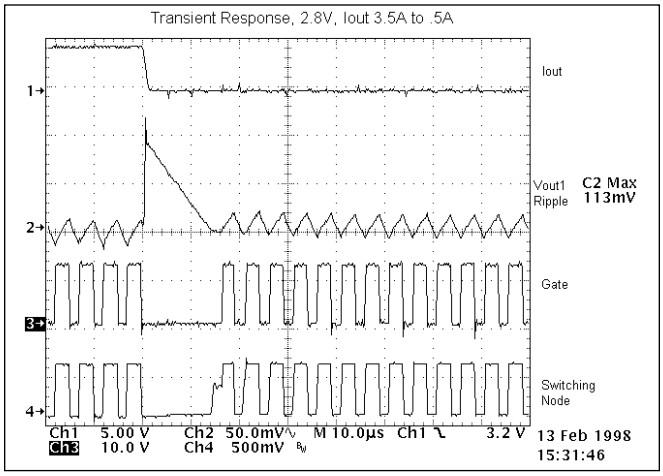


Figure 6.

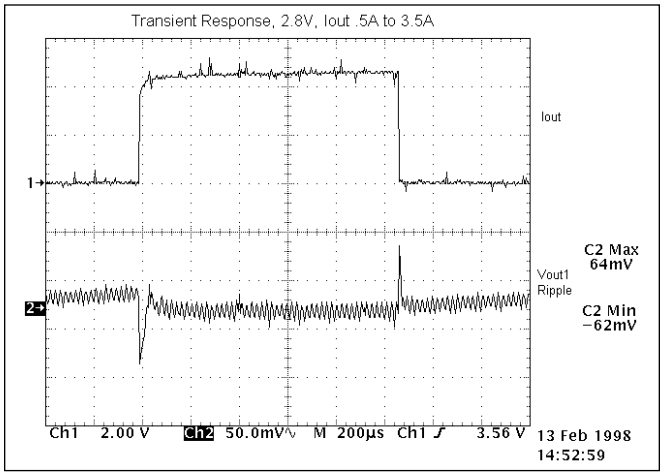


Figure 9.

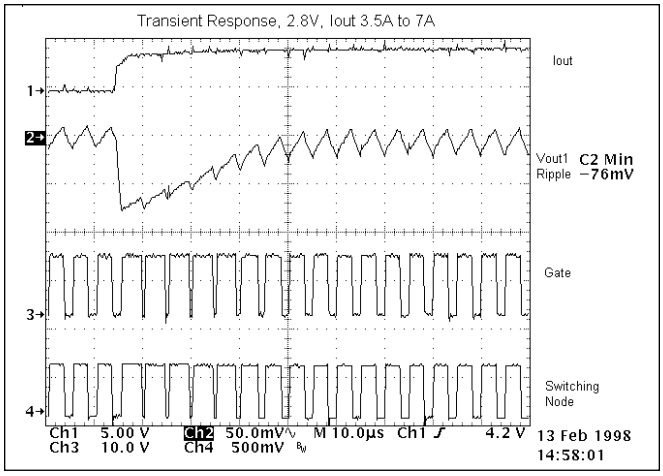


Figure 7.

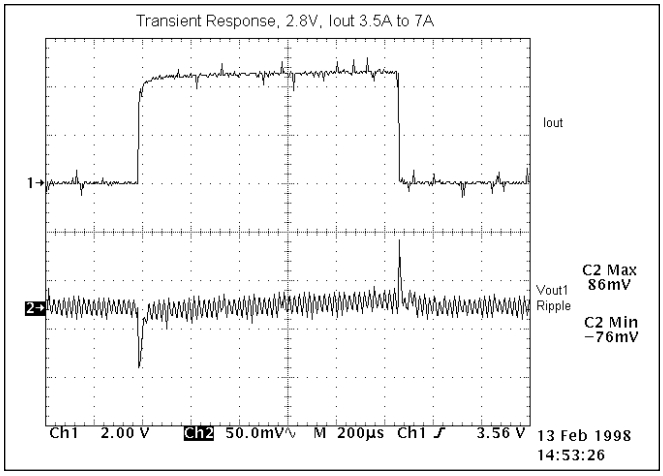


Figure 10.

Typical Performance Characteristics continued

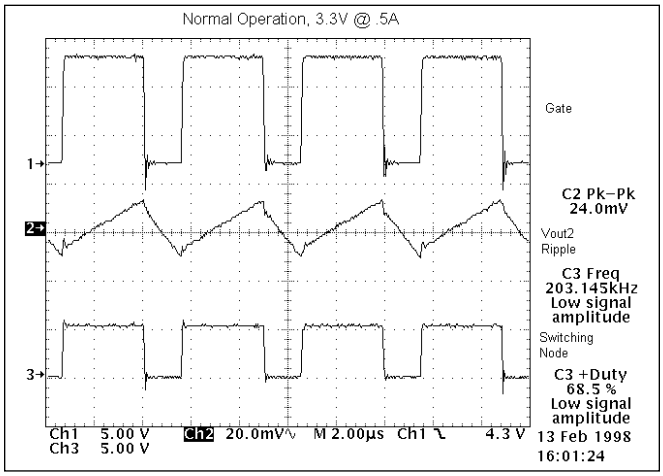
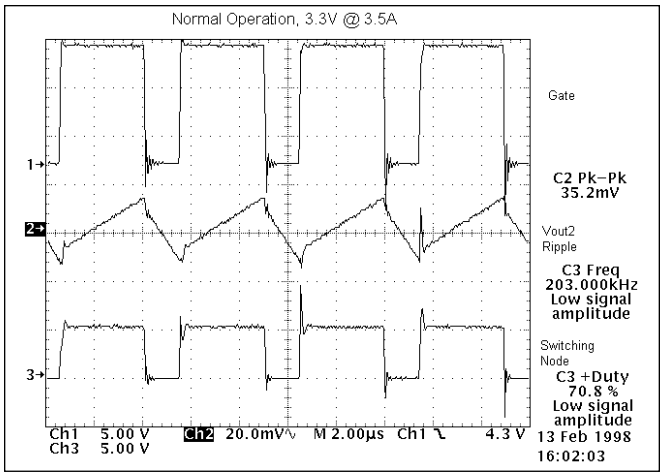


Figure 11.



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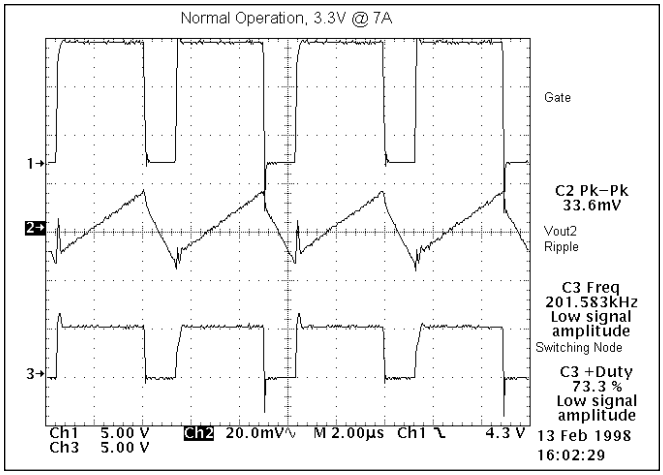
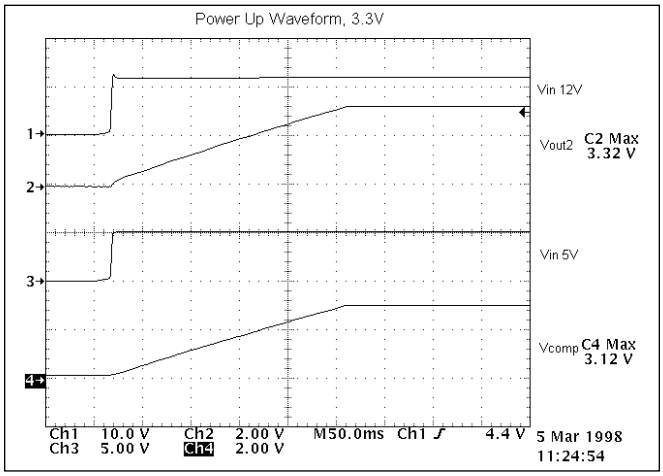


Figure 13.



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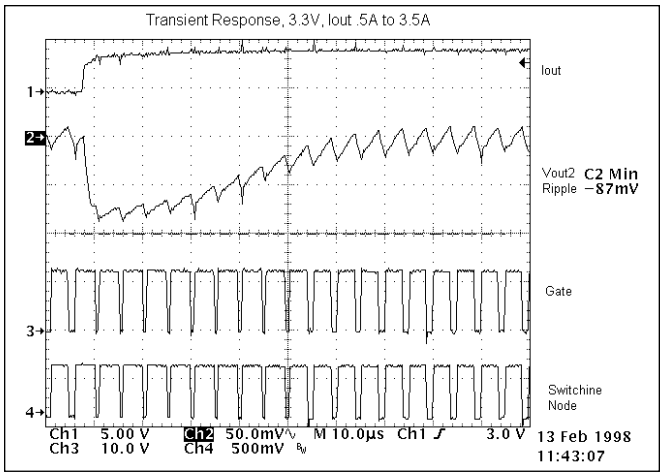


Figure 15.

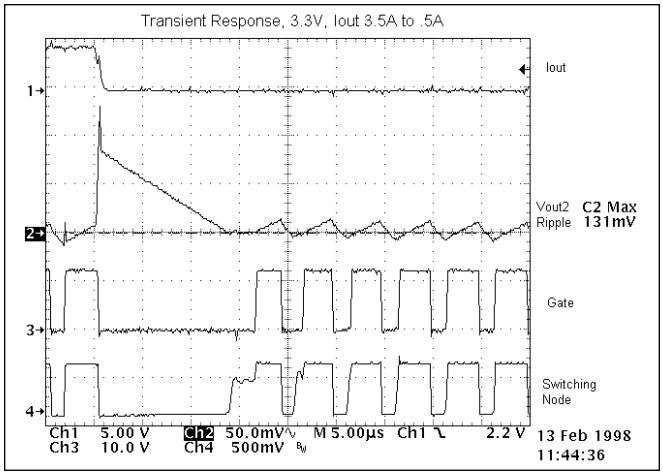


Figure 16.

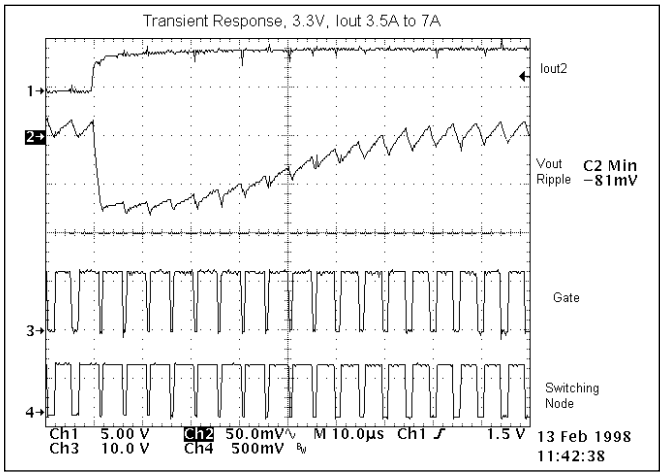


Figure 17.

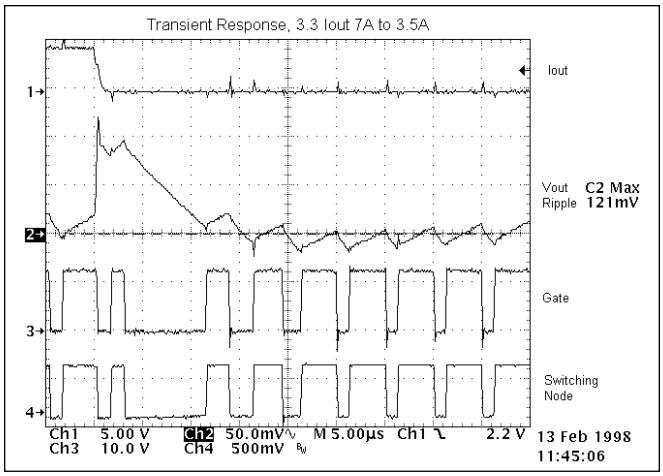
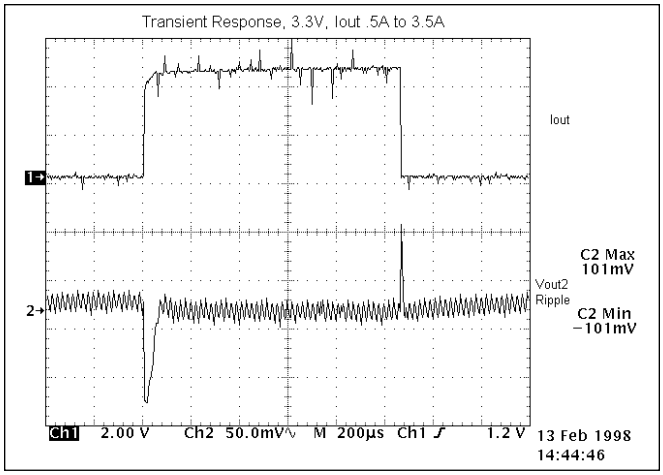


Figure 18.



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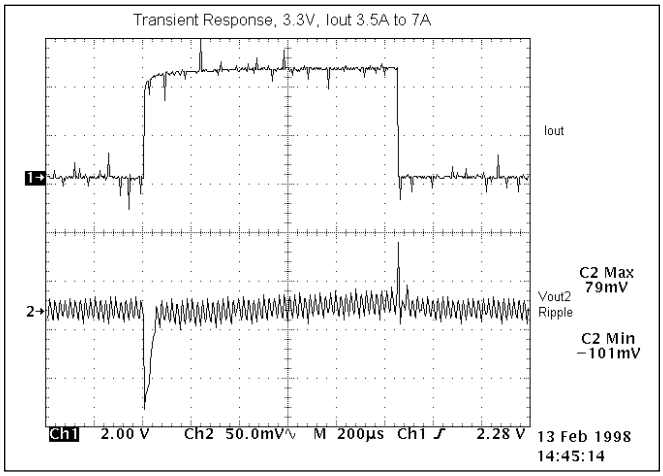

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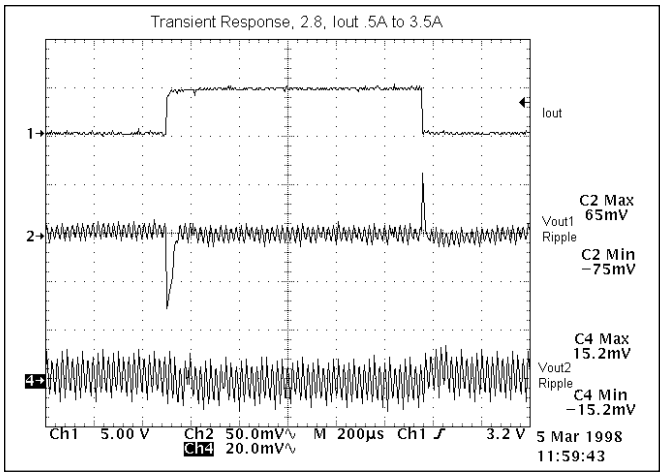


Figure 21: Effect of Channel 1 Transient Response on Channel 2 DC Regulation (I_{LOAD} = 500mA).

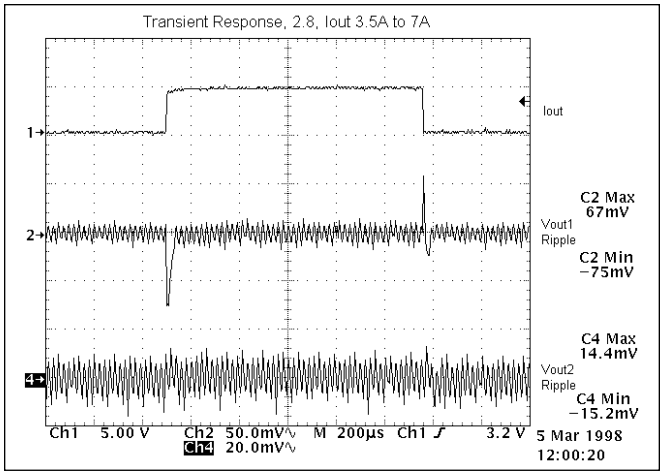


Figure 22: Effect of Channel 1 Transient Response on Channel 2 DC Regulation (I_{LOAD} = 500mA).

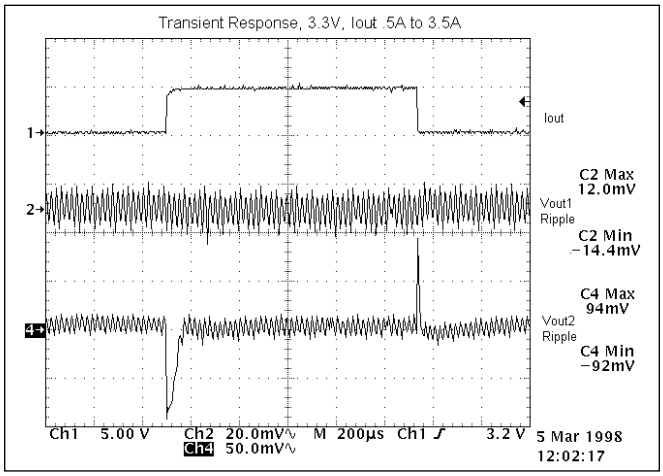


Figure 23: Effect of Channel 2 Transient Response on Channel 1 DC Regulation (I_{LOAD} = 500mA).

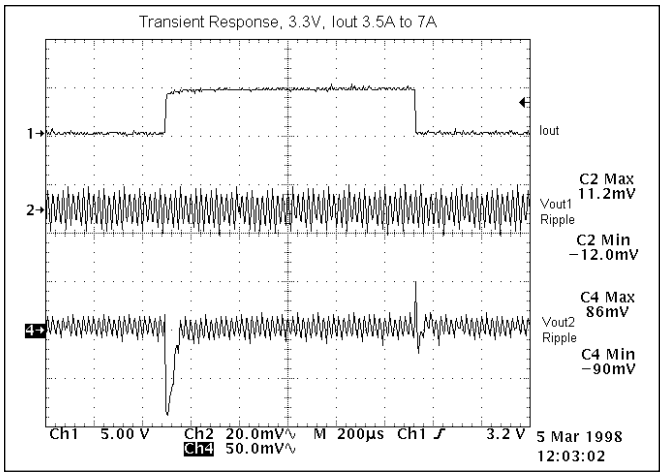


Figure 24: Effect of Channel 2 Transient Response on Channel 1 DC Regulation (I_{LOAD} = 500mA).

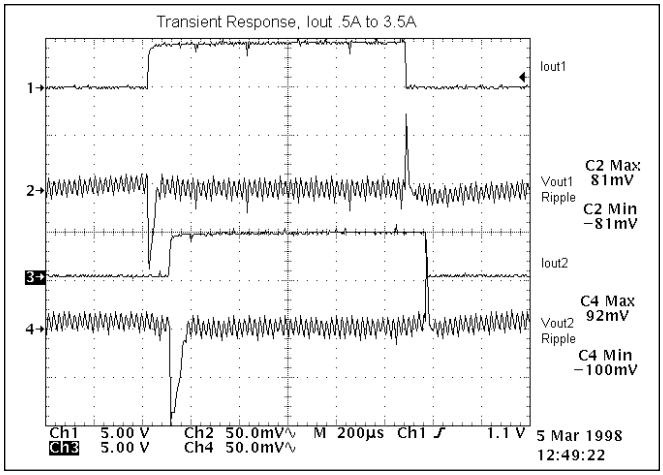


Figure 25: Effect of both channels' transient responses (0.5 to 3.5A load step).

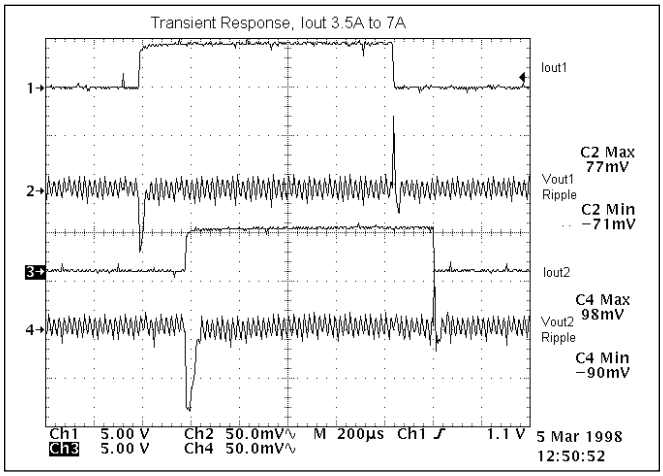


Figure 26: Effect of both channels' transient responses (3.5A to 7A load step).

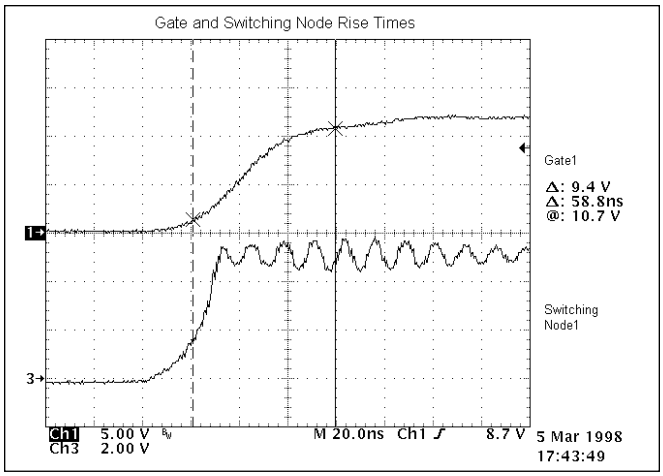


Figure 27.

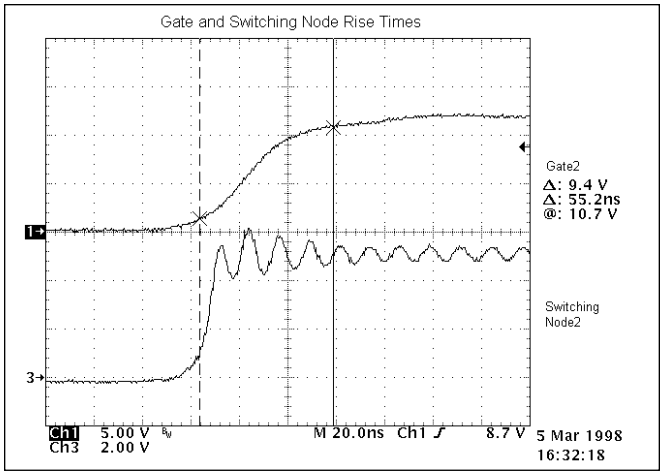


Figure 28.

Typical Performance Characteristics continued

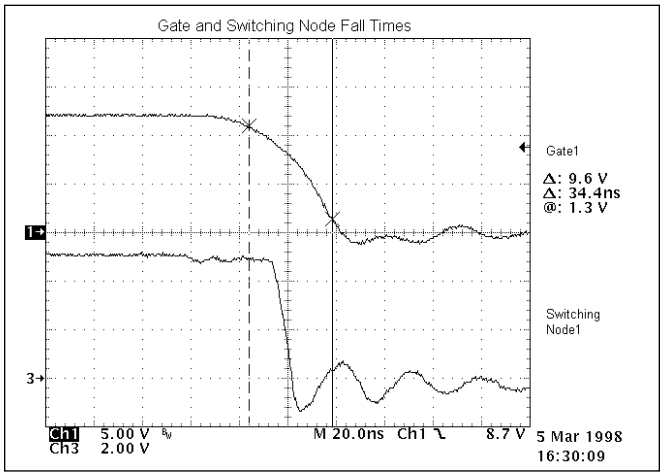


Figure 29.

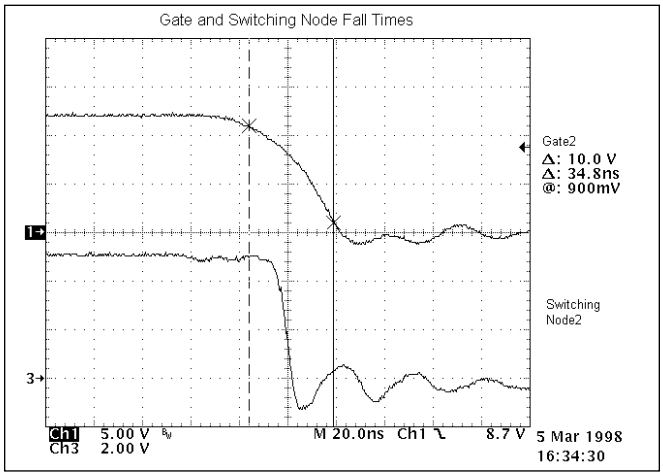


Figure 30.

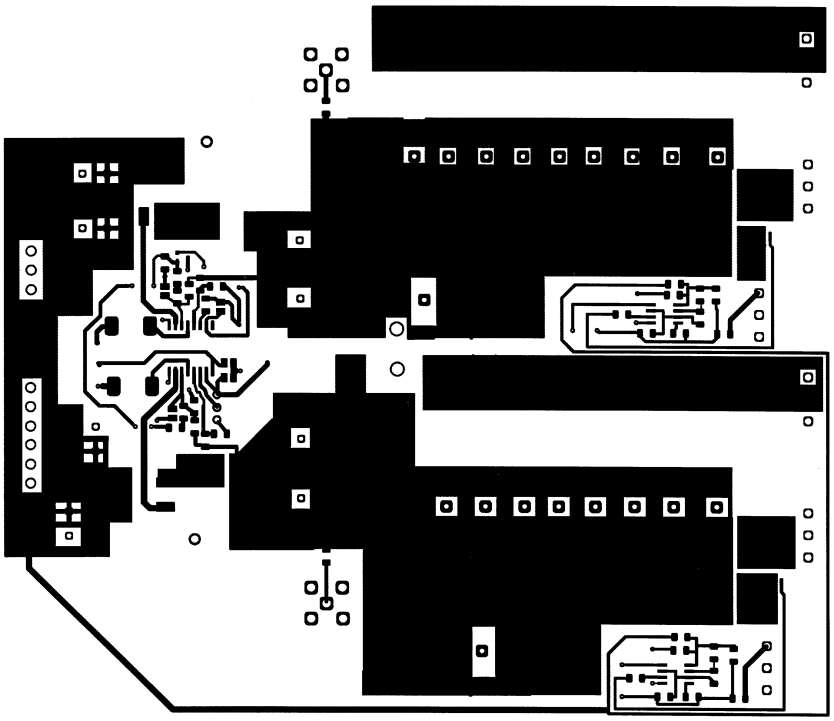
CS5127 Demonstration Board Bill of Materials

Ref. Designator	Manufacturer	Part Number	Value/Desc.	Qty	Website	Telephone
DC/DC Converter						
U1	ON Semiconductor	CS5127DW16*01	Dual Channel V^{2TM} Buck Controller IC	1	www. cherry-semi.com	(800)-272-3601
C1,C2,C4,C5, C10-C13	Panasonic	ECA-1AFQ681	680µF 10V,Radial lead Electrolytic	8	www.panasonic.com	(800)-344-2112 Ext. 200
C3,C8	Panasonic	ECS-T1CY105R	1µF 16V Tantalum Electrolytic chip	2	www.panasonic.com	(800)-344-2112
C6,C9	Panasonic	ECH-V1H104KBW	0.1µF 50V Film Chip	2	www.panasonic.com	(800)-344-2112
C14, C17	Panasonic	ECH-V1H331KBW	330pF 50V Film Chip	2	www.panasonic.com	(800)-344-2112
C7	Panasonic	ECH-U1H471JB5	470pF 50V Film Chip	1	www.panasonic.com	(800)-344-2112
C15,C16	Panasonic	ECE-V1AA101UP	100µF 10V Electrolytic	2	www.panasonic.com	(803)-448-9411
R1,R2,R10,R11	Panasonic	ERJ-8GEYJ204	20K 1/8W 5%	4	www.panasonic.com	(800)-344-2112
R3	Panasonic	ERJ-8GEJ184	18K, 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R4	Panasonic	ERJ-8ENF1543	1.54K 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R5	Panasonic	ERJ-8ENF1273	1.27K 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R6	Panasonic	ERJ-8GEJ103	1K 1/8W 5%	1	www.panasonic.com	(800)-344-2112
R7	Panasonic	ERJ-8ENF2403	2.40K 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R8	Panasonic	ERJ-8ENF1503	1.50K 1/8W 1%	1	www.panasonic.com	(800)-344-2112
R9	Panasonic	ERJ-8GEYJ203	2K 1/8W 5%	2	www.panasonic.com	(800)-344-2112
D1,D2	Lite-On	1N5821	Schottky Diode	2	www.vishay-liteon.com	(602)-302-8056
Q1	ZETEX	FMMT2222A	SOT-23 NPN Transistor	1	www.zetex.com	(516)-543-7100
Q2,Q3	International Rectifier	IRL3103S	N Channel FET	2	www.irf.com	(310)-252-7032
L1,L2	Xformers, Inc	XF0066-VO2	5µH Inductor	2	www.xfmrs.com	(800)-344-4539

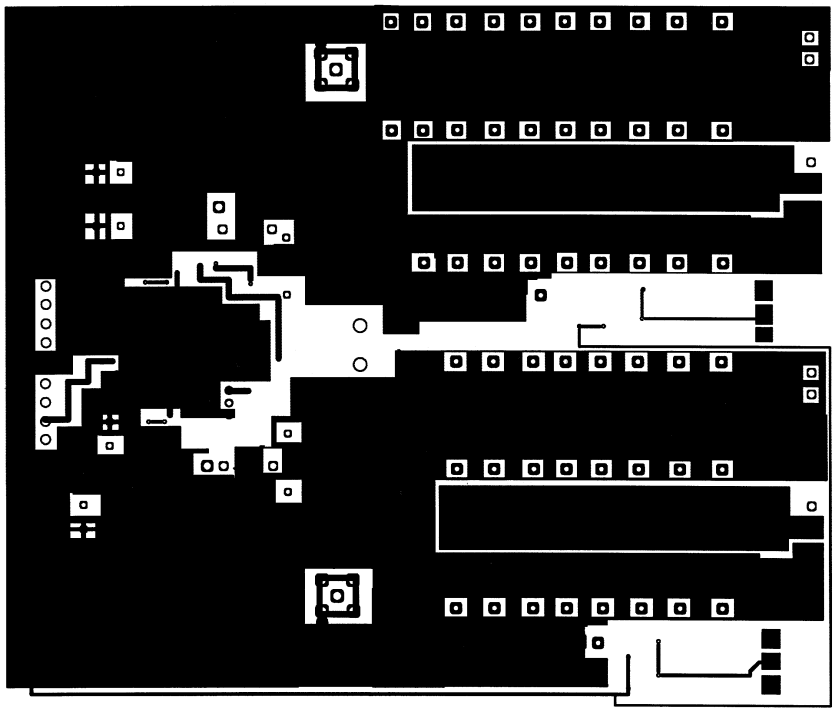
CS5127 Demonstration Board Bill of Materials continued

Ref. Designator	Manufacturer	Part Number	Value/Desc.	Qty	Website	Telephone
Test Circuitry						
C18-C23	Panasonic	ECU-V1H104KBW	0.1µF 50V Film Chip	6	www.panasonic.com	(800)-344-2112
R13,R14,R41,R42	Panasonic	ERJ-8GEYJ203	2K, 1/8 W, 5%	4	www.panasonic.com	(800)-344-2112
R15, R43	Panasonic	ERJ-8GEYJ134	13K, 1/8 W, 5%	2	www.panasonic.com	(800)-344-2112
R17,R18,R45,R46	Panasonic	ERJ-8GEYJ102	100Ω, 1/8 W, 5%	4	www.panasonic.com	(800)-344-2112
R12,R16,R40,R44	Panasonic	ERJ-8GEYJ101	10Ω 1/8 W, 5%	4	www.panasonic.com	(800)-344-2112
R21-R39,R49-R64	Panasonic		Film 7.5Ω, 3W 5%	35	www.panasonic.com	(803)-344-2112
Q5,Q6	International Rectifier	IRF7413	N Channel FET	2	www.irf.com	(310)-252-7032
TP1–TP4	Cambion (distributed by Newark Electronics)	40F6023 (Newark stock number)	Turret Pin	4	www.newark.com	(800)-463-9275
J1, J2	Farnell (distributed by Newark Electronics)	583-558 (Newark stock number)	BNC Connector	2	www.newark.com	(800)-463-9275
S1-S6	C & K Components	7101MDRBE	SPDT Switch	6	www.ckcomponents.com	(800)-635-5936
U2, U3	International Rectifier	LM555	Timer IC	2	www.irf.com	(310)-252-7032
J3, J4	Molex	26-48-1065	Straight Friction Lock Connector	2	www.molex.com	(800)-786-6539
S7	C&K Components	T101SHCQE	Switch SPDT	1	www.ckcomponents.com	(800)-635-5936

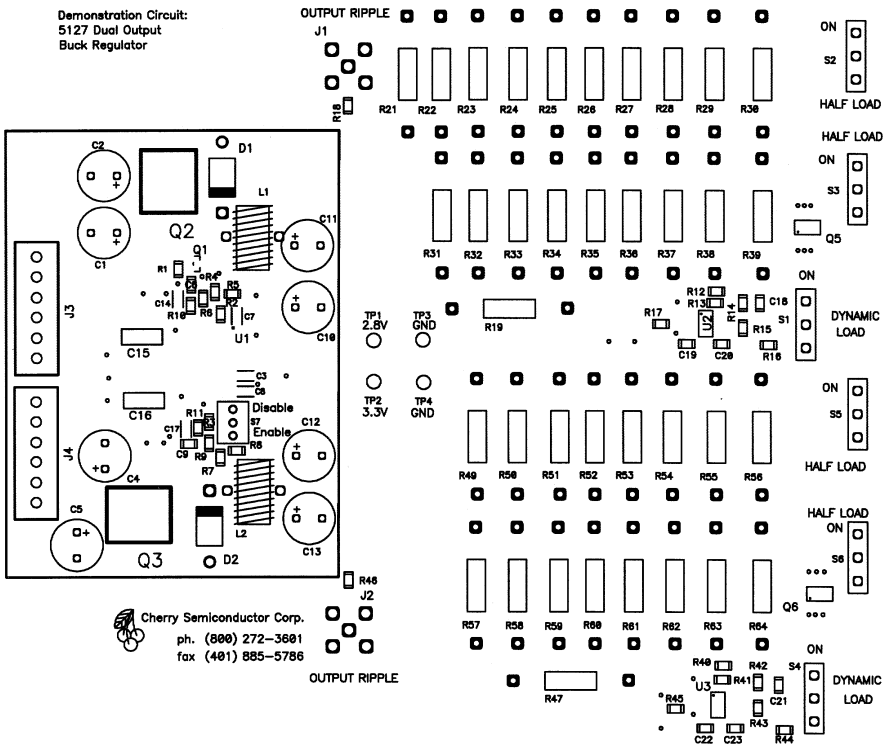
Printed Circuit Board Layout Information



This is the layout pattern for the top layer metal of the printed circuit board for the demonstration.



This is the layout pattern for the bottom layer metal of the printed circuit board for the demonstration.



This is the layout pattern for the silkscreen layer of the printed circuit board for the demonstration.

Notes

Notes