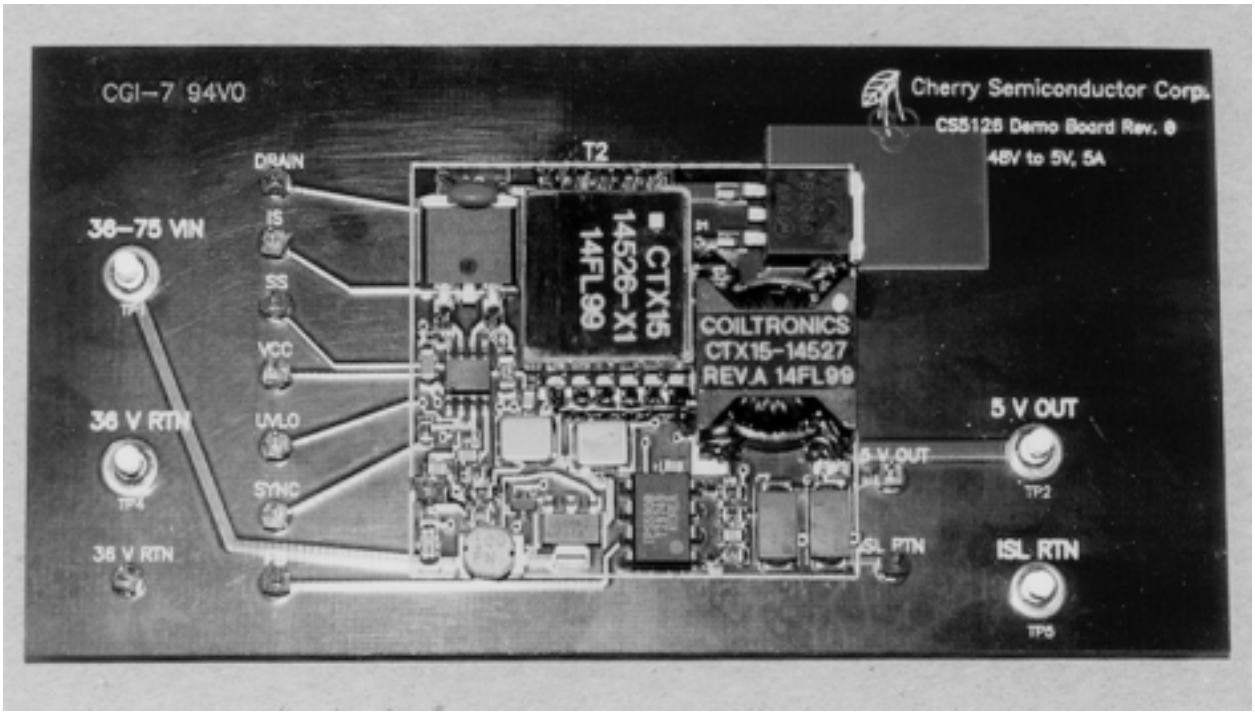
48V to 5V,
5A Forward Converter

a CS5126 Demonstration Manual



ON Semiconductor

January, 2000 - Rev. 1
CS5126DM

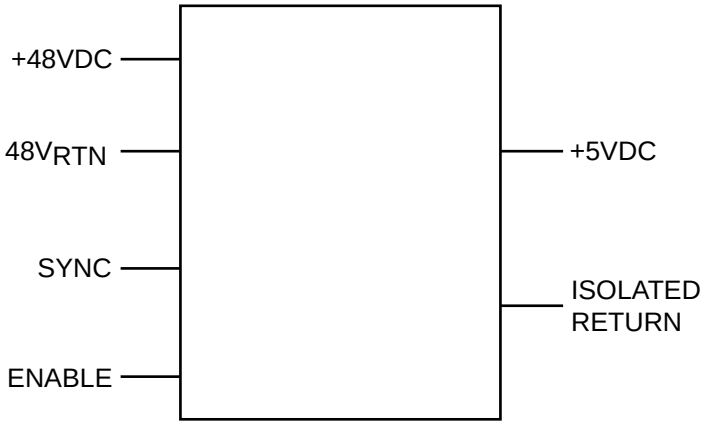
Description

The CS5126 demonstration board is a fixed frequency, isolated, 48VDC to 5VDC forward converter. High efficiency over a wide input voltage range is accomplished by powering the CS5126 controller from a flyback winding on the forward inductor. Blanking, short circuit, overload, and input undervoltage protection are all accomplished by integrated CS5126 circuitry.

Features

- 36 to 75VDC Input Voltage Range
- 5V, 5A Isolated Output
- 1.62" × 1.95" Footprint
- 82% Typical Efficiency
- External Synchronization 170kHz to 450kHz
- Input Undervoltage Shutdown and Sleep Mode
- Remote Enable Input
- Overcurrent Protection
- Thermal Shutdown

Application Diagram



Pin Description

Pin Symbol	Function
+48VDC	36 to 75VDC Input.
$48V_{RTN}$	Return for +48VDC Input.
SYNC	Clock synchronization pin. A positive edge will terminate the current PWM cycle. Ground this pin if it is not used.
ENABLE	This pin is internally pulled up and performs the UVLO function if left open. Pull this pin to between 2.3V and 2.6V to stop the converter from switching. Pull this pin to below 1.5V to put the converter in sleep mode.
+5VDC	+5VDC Isolated Output.
ISOLATED RETURN	Return for +5VDC Output.

Absolute Maximum Ratings

T_A = 25°C			
Input/Output Name	**Minimum**	**Maximum**	**Unit**
+48VDC	–0.3	80.0	Volts
Output Current		Internally Limited	Amps
SYNC	–1	40	Volts
ENABLE	–0.3	6.0	Volts
Isolated Return	–500	+500	VDC

Electrical Characteristics

T_A = 25°C, 36 to 75V, 200kHz, Unless Otherwise Specified					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	0.25A < I_{OUT} < 5A	4.85	5.00	5.15	V
Load Reg.	0.25A < I_{OUT} < 5A		0.1		%
Line Reg.	0.25A < I_{OUT} < 5A		0.02		%
Transient Regulation & Recovery Time to within 2%	Step Between 50% and 75% of Maximum Load.		180 75		mV µs
Output Ripple and Noise	75V_{IN} @ Full Load(20MHz BW)		60		mV_{P-P}
Input Current Ripple	75V_{IN} @ Full Load, 200kHz		35		mA_{rms}
Efficiency	0.5A Out, 5A Out		60% 82%		% %
Enable / S.S. Time	Full Load		4		ms
Enable (Turn-on) Threshold		2.30	2.45	2.60	V
Enable Hysteresis		170	185	200	mV
Sleep Mode (Turn-off) Threshold		1.50	1.83	2.30	V
Sleep Mode Hysteresis		35.0	85.0	1.5	mV
Enable Pin Source Current	Enable Pin = 0V			1	mA
Sleep Mode Input Current	75V_{IN}		2	3	mA
Undervoltage Lockout (Turn-off)		28	31	33	Volts
Undervoltage Lockout (Turn-on)		31	33	35	V
Undervoltage Lockout Hysteresis			2		V
SYNC Threshold		2	4	6	V
SYNC Frequency Range	V_{IN} > 48V for frequencies above 250kHz	170		450	kHz
Overcurrent Limit Threshold	V_{IN} = 36V V_{IN} = 75V		5.7 6.0		A
Oscillator Freq.	Free running	170	200	230	kHz

Demonstration Board Operation Guidelines

Input Power

The converter is designed to run with an input voltage between 36VDC to 75VDC. Approximately 0.87A of current is required for full load with a 36V input.

Output Load

An external load is required for the demo board to run normally at fixed frequency. If the demo board is run with a load less than 150mA the output will be regulated at 5V in hiccup mode.

SYNC

The Sync threshold is scaled to allow the converter to be synchronized to a typical MOSFET gate drive levels. When the converter is not being synchronized to an external source this pin should be tied low.

Demonstration Board Schematic

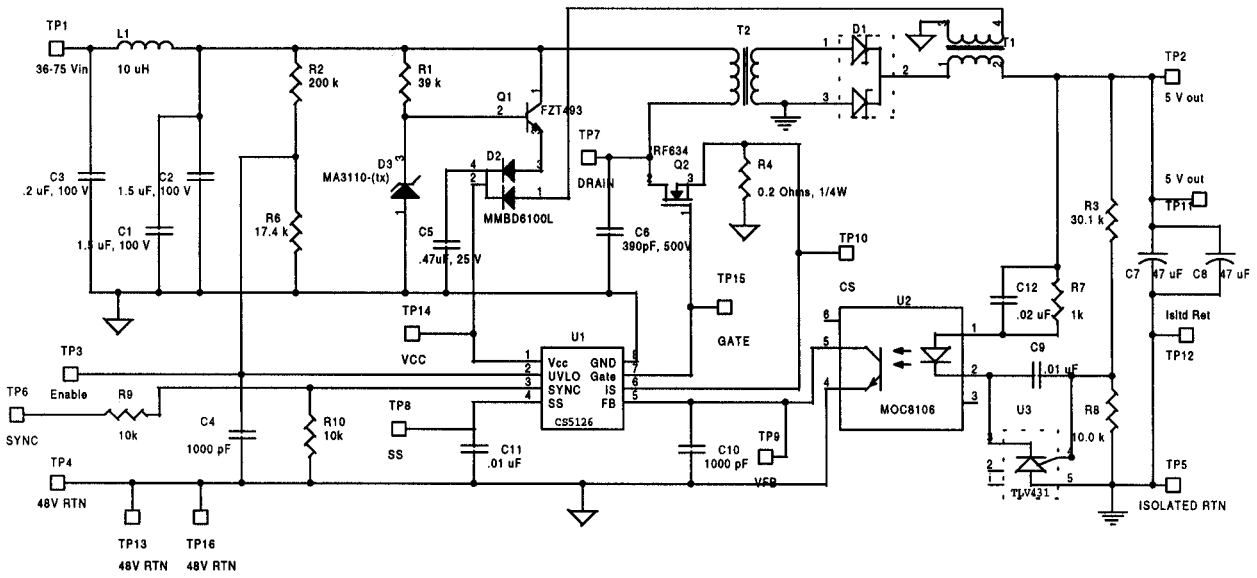


Figure 1. Circuit Schematic

Theory of Operation

Enable/UVLO

R2 and R6 form a divider for the UVLO function. If the ENABLE pin of the supply is left open it will operate in one of three modes depending on the input voltage. For V_{IN} less than 18V the supply will be in sleep mode. For V_{IN} between 18V and 31V the PWM section is disabled. If V_{IN} exceeds 35V the supply operate normally.

The ENABLE pin can also be controlled by open collector logic to perform an ENABLE function. Any time the ENABLE pin is below 1.5V the supply will be in sleep mode and input current will be less than 3mA.

V_{CC} Bias

R1 and D3 provide a reference for Q1 high to regulate Vcc at about 9V when the converter is not running. When the converter is running normally, the flyback winding of T1 is clamped at 12V (in proportion to the output voltage), the base of Q1 is reverse biased and Vcc is powered from T1.

Current Sensing

R4 is the current sense resistor. The turn-on spikes, shown in Figures 11-13, are blanked internally by the CS5126. During heavy load conditions the primary current is pulse by pulse limited as shown in Figures 14 and 15. Under conditions with high currents and fast rise-times, the converter will enter a low duty cycle hiccup mode as shown in Figure 16.

Soft Start & Hiccup Mode

Soft Start capacitor C11 determines the Soft Start time during turn-on, and the dead time when the supply is operating in hiccup mode. During Soft Start there will be a dead time of about 1.6ms while C8 charges to 1.6 V. The ramp-up time of the output voltage will last about 1-2ms depending on output load.

During hiccup mode the dead time will be about 1.4ms while C8 charges from 0.25V to 1.6V as shown in Figure 16.

Feedback

R3 and R8 divide the 5V output to the 1.24V reference of optoisolator U2. C9 and the Thevenin resistance of R3 and R8 set the low frequency roll-off of U2. R7 sets the maximum current through U2's photodiode and adjusts gain. C12 provides a phase boost near the crossover frequency. C10 is primarily intended to improve high frequency noise reduction.

Design Guidelines

Transformer Design and Resonant Reset

This design uses resonant reset for the transformer. Energy stored in the transformer magnetizing inductance during the on time is transferred back to the input through the resonating capacitance and transformer primary. In order to provide adequate reset time the transformer ratio was chosen for a 60% duty cycle at low supply line voltage using Formula 1.

$$\text{Transformer Ratio} = \frac{N_P}{N_S} \times \frac{1}{\text{Duty}} \qquad (1)$$

$$= \frac{5.4}{36} \times \frac{1}{0.6} = \frac{1}{4}$$

Using standard transformer design equations the transformer design is: EFD-17 core with a 20 turns of #26AWG on the primary and 5×5 turns of #26AWG on the secondary. The nominal primary inductance is 344µH.

The resonating capacitance was chosen to meet two constraints: reset time less than the minimum off time (2µs) and the maximum peak primary voltage less than the rating of the MOSFET (250V). An approximate resonating capacitance for the required reset time at light load can be chosen from Formula 2. (Reset time will typically be slowest with light loads.)

$$C_{RESONANT} = \frac{\text{Reset Period}^2}{\pi^2 \times L_{PRIMARY}} \qquad (2)$$

$$= \frac{(1.5\mu s)^2}{9.9 \times 344\mu H} \times 660pF$$

$C_{RESONANT}$ is made up of all capacitances associated with the transformer including the MOSFET drain capacitance, transformer internal capacitance and the Schottky diode capacitance. The effective IRF634 capacitance was estimated at 150pF from the data sheet. The value for the Schottky capacitance was estimated at 160pF from curves on a MBRB20200CT data sheet and contributes 10pF when reflected to the primary. The internal transformer primary capacitance is estimated to be 100pF based on transformer dimensions and the insulation thickness of #26 single build wire. These calculations leave 390pF to be added externally to the transformer primary.

If the actual reset time is too long the capacitor value can be reduced. If the overshoot is too high and the reset period too long the transformer ratio can be adjusted for a lower duty cycle. An estimate of the peak primary voltage can be made by calculating the energy stored in the transformer during each cycle (Formula 3) and then by calculating the peak primary voltage based on transferring the stored energy to the resonating capacitance (Formula 4).

$$E_{STORED} = \frac{V^2 \times D^2}{2 \times L_{PRI} \times F_2} - \frac{\text{Core Loss}}{F} - \frac{\text{Switching Loss}}{F} \quad (3)$$

$$= \frac{(48 - 1.5)^2 \times .46^2}{2 \times 344\mu H \times 200k^2} - \frac{.5W}{200k} - \frac{.68W}{200k}$$

$$= 10.7\mu J$$

(V is the input voltage minus the voltage drops in the sense resistor, power MOSFET and transformer primary.)

$$V_{PEAK} = (2 \times E_{STORED} \ / \ C_{RESONANT})^{1/2} + V_{IN} \quad (4)$$

$$= (2 \times 10.7\mu J \ / \ 660pF)^{1/2} + 48V = 228V$$

The results of the above formulas are only approximate. Neither equation includes effects of leakage inductance or MOSFET capacitance change with drain voltage. The final values for the resonant reset circuit can be chosen empirically. The typical peak voltage measured on the circuit ranged from 160V to 210V.

The value of the resonating capacitor is related to the operating frequency. An external 390pF capacitor was chosen as the optimum value for the converter at 200kHz. At frequencies above 200kHz, this capacitor is larger than optimum. At higher frequencies, a smaller value will raise efficiency and reduce reset time. At higher frequencies with input voltages less than 48V, subharmonic oscillation may occur when a new PWM cycle begins before the transformer is reset as shown in Figure 23.

Output Inductor and Current Sense Resistor Selection

The values of the current sense resistor (R4) and the output inductor are related by the slope compensation ramp. The current sense resistor value is also constrained by the converter current limit threshold. Several iterations of the procedure below might be required to choose compatible values.

1. Choose (estimate) a value for the output inductor – 10µH.

2. Calculate output filter ripple at high supply line voltage in continuous conduction mode.

$$I_{PK-PK} = \frac{V_{OUT} \times T_{OFF}}{L} = \frac{5.3V \times 3.5\mu s}{10\mu H} = 1.85A_{PK-PK}$$

3. Calculate peak secondary current at high line and current limit threshold.

$$I_{SEC(PK)} = I_{MAX} + I_{P-P}/2 = 6A + 0.93A = 6.93A$$

4. Calculate peak primary current at high line and current limit threshold.

$$I_{PRI(PK)} = I_{SEC(PK)} \times \frac{N_S}{N_P} + \frac{V_{IN} \times T_{ON}}{L_{PRI}} = 6.93A \times \frac{1}{4} + \frac{75V \times 1.5\mu s}{344\mu H} = 2A$$

5. Calculate 1st current sense threshold (using formula in CS5126 datasheet).

Design Guidelines continued

$$1^{st}\ \text{Threshold} = \frac{2.65V - 85mV/\mu s \times T_{ON}}{5} - 0.13$$

$$= \frac{2.65 - .085 \times 1.5}{5} - 0.13 = 0.375V$$

6. Choose current sense resistor value.

$$R_{SENSE} = \frac{1^{st}\ \text{Threshold}}{I_{PRIpk}} = \frac{0.375V}{2A} = 0.19\Omega$$

7. Recalculate inductor value for slope compensation factor of 1. (See data sheet.)

$$\text{Inductor Value (H)} = \frac{1}{\text{Internal Ramp}} \times V_{OUT} + V_{RECTIFIER}$$

$$\times \frac{N_{SECONDARY}}{N_{PRIMARY}} \times R_{SENSE} \times \text{Slope Value Factor}$$

$$= \frac{1}{20mV\ /\ \mu s} \times \left(5V + 0.3V\right) \times \frac{1}{4} \times 0.19\Omega \times 1$$

$$= 12.6\mu H$$

8. If required, recalculate with the new inductor value starting at step 2. The actual values for this design were 0.2Ω and 12.3µH.

Typical Performance Characteristics

The figures below show typical performance of the CS5126 Demo Board. All waveforms were taken with the 20MHz filter option selected on the oscilloscope.

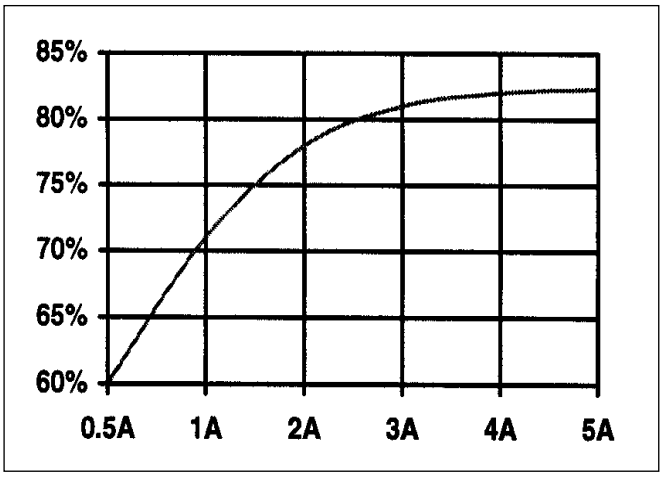


Figure 2: Typical Output Efficiency at $48V_{IN}$, 200kHz.

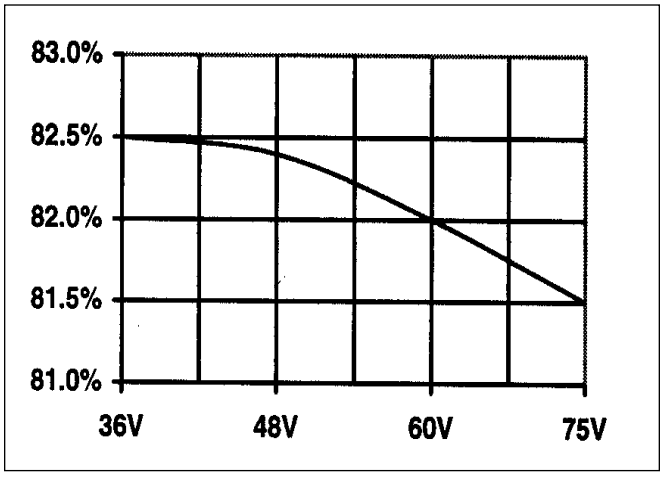


Figure 3: Typical Output Efficiency at 5A Out 200kHz.

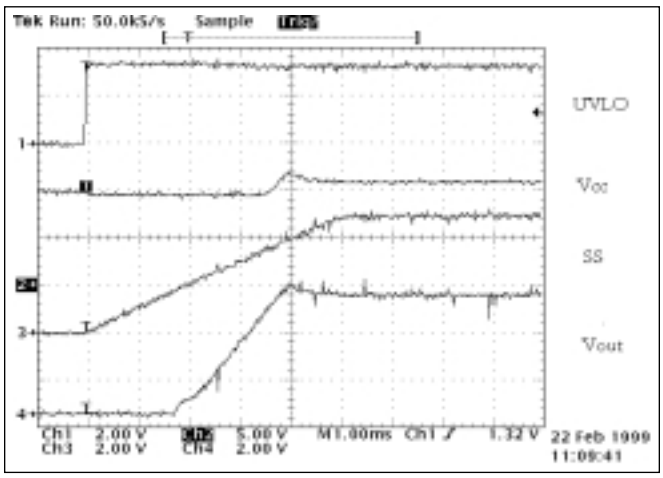


Figure 4: Startup Waveforms @ 48 V_{IN} 5A (1Ω) Load.

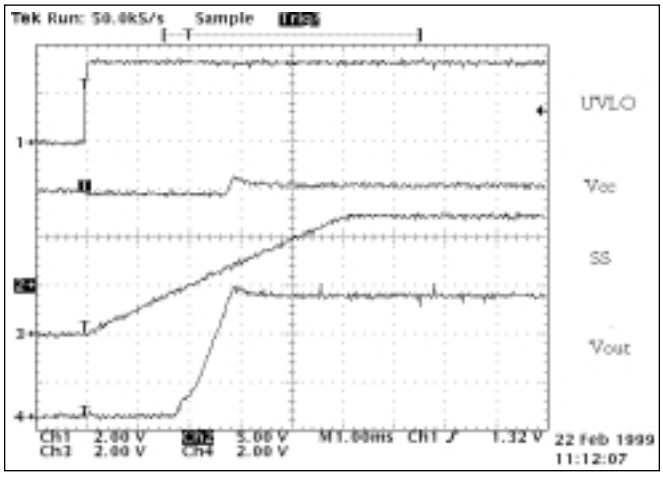


Figure 5: Startup Waveforms @ 48 V_{IN} with 1A (5Ω) Load.

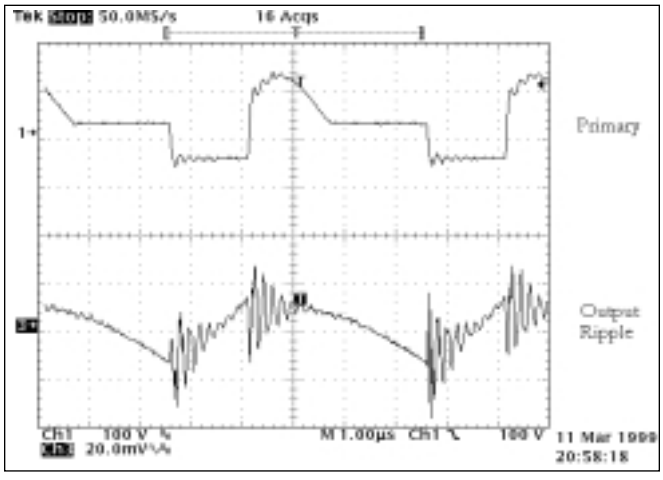


Figure 6: Primary Voltage and Output Ripple at 75V_{IN}, 5A Out. (Primary side floating. Output grounded directly to body of Ch3 scope probe.)

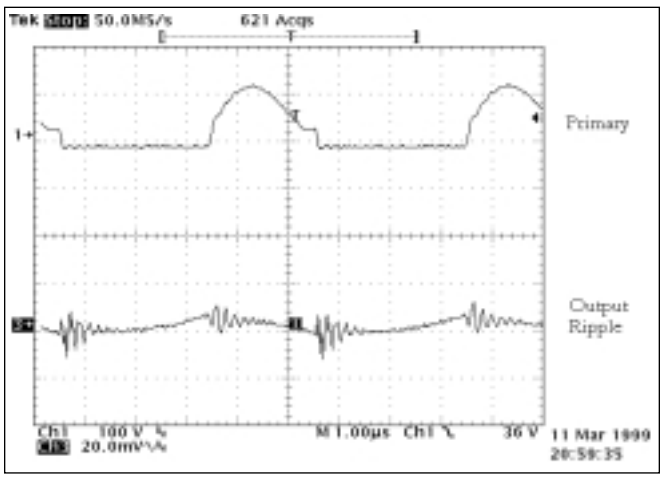


Figure 7: Primary Voltage and Output Ripple at 36V_{IN}, 1A Out. (Primary side floating. Output grounded directly to body of Ch3 scope probe.)

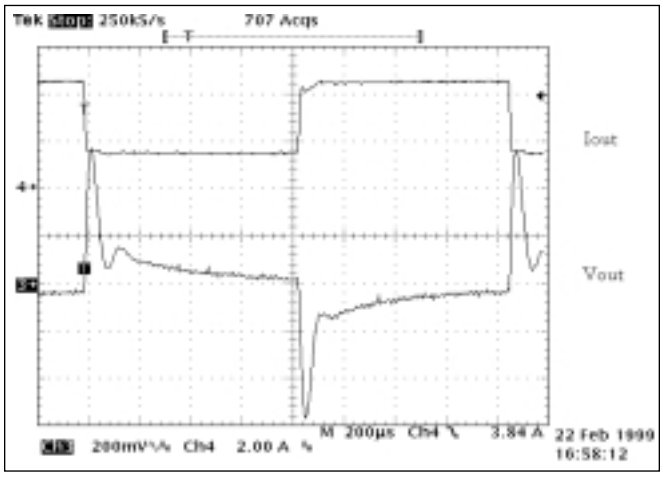


Figure 8: Transient Response 1.5A to 4.6A Step.

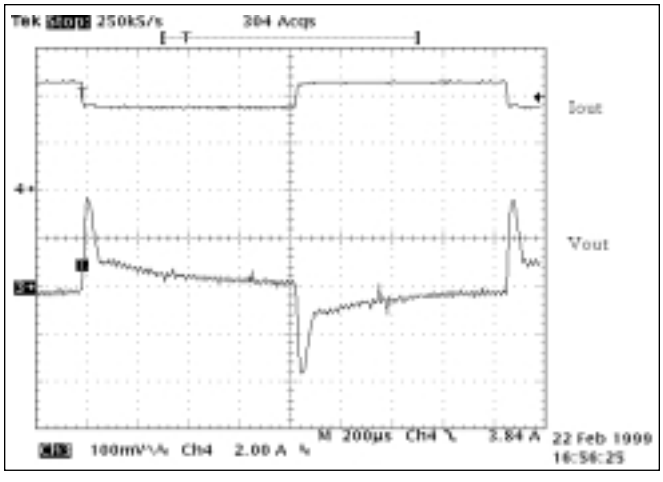


Figure 9: Transient Response 3.5A to 4.6 Step.

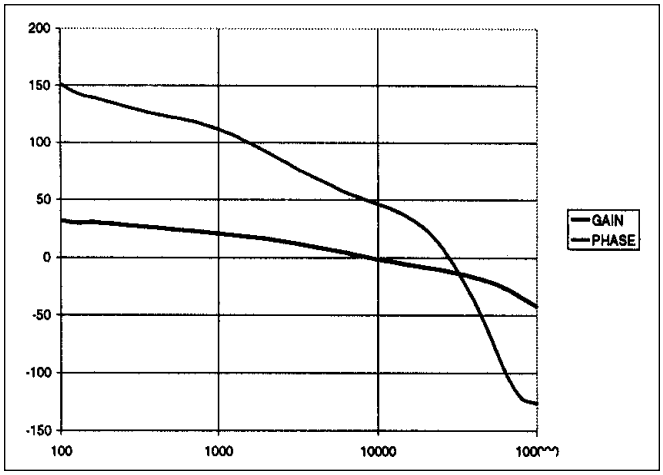


Figure 10: Control Loop @ 48V_{IN}, 2.5A Out. Crossover = 9kHz. PM = 50°. GM = 11dB.

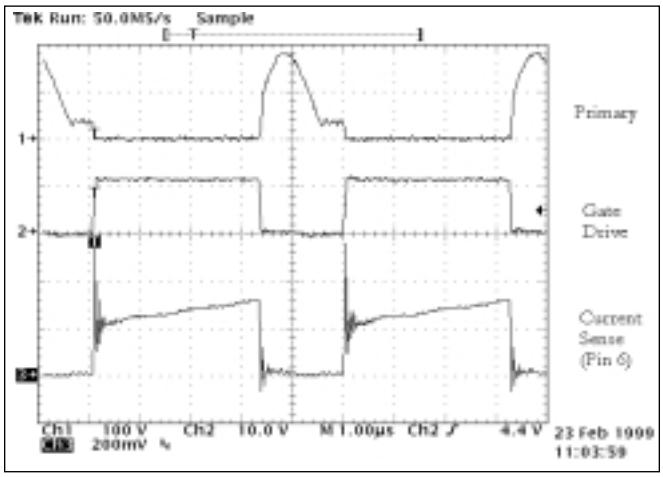


Figure 11: Current Sense 36V_{IN}, 5A Out.

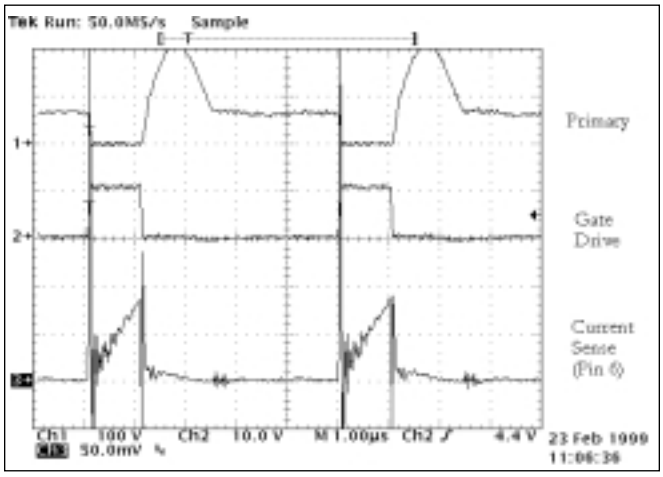


Figure 12: Current Sense 75V_{IN}, 0.5A Out.

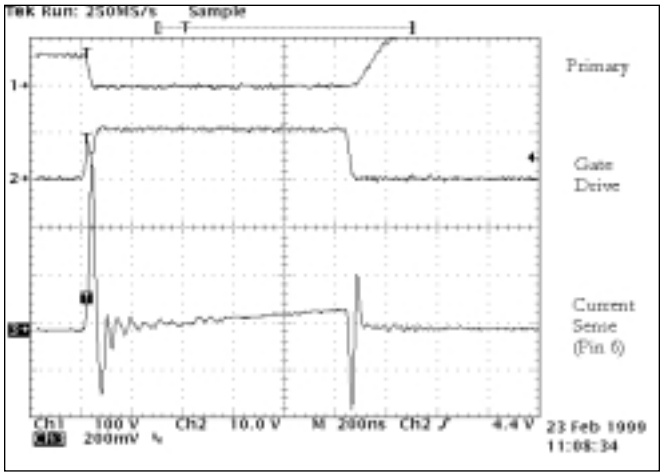


Figure 13: Current Sense 75V_{IN}, 5A Out Expanded.

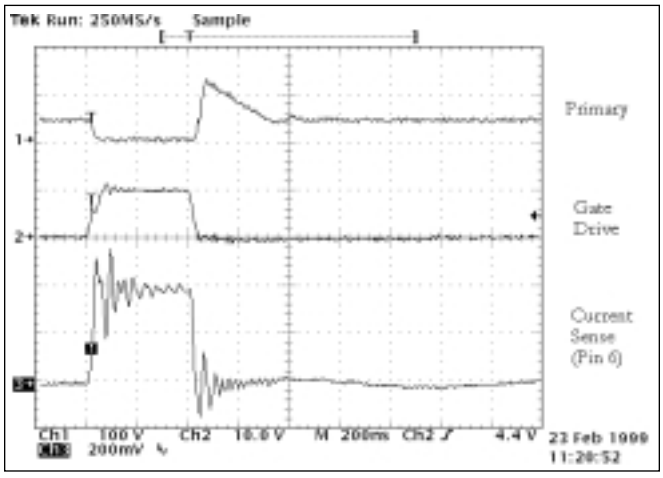


Figure 14: Current Sense 36V_{IN}, Output Shorted.

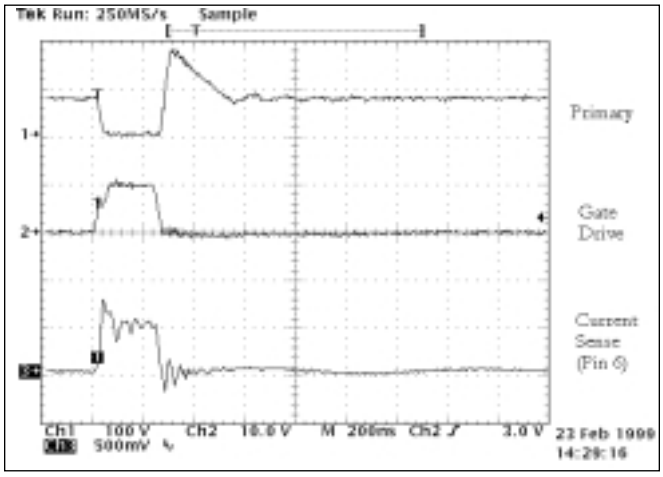


Figure 15: Current Sense 75 V_{IN}, Output Shorted.

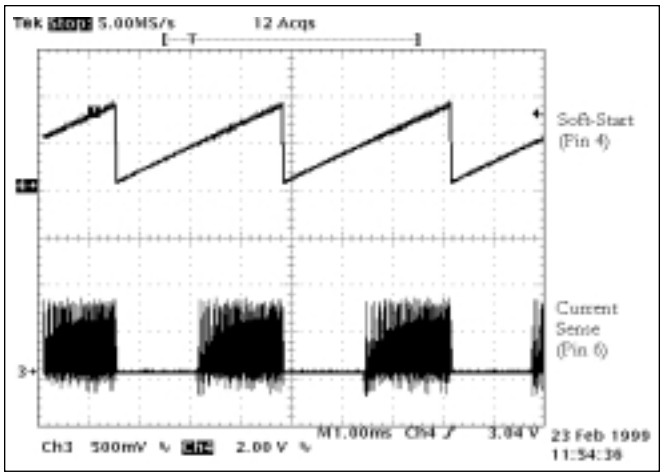


Figure 16: Second Threshold Operation. 85V_{IN}, Output shorted. (A low impedance connection is required to reach second threshold.)

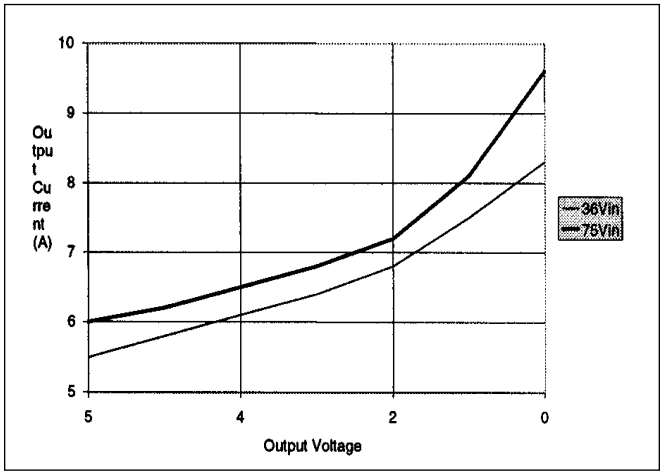


Figure 17: V-I Curves during High Output Currents.

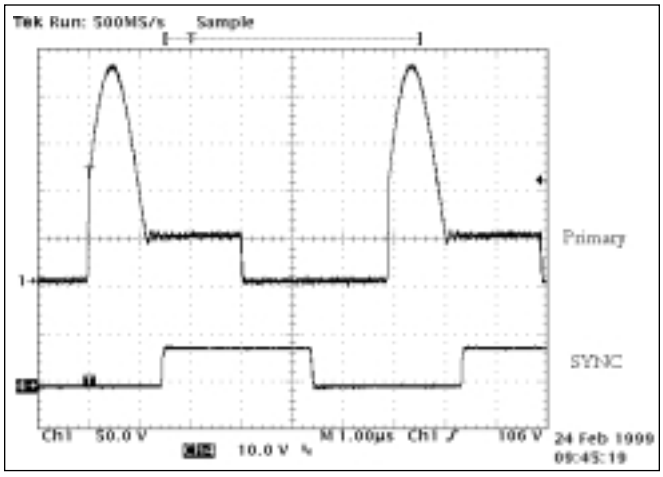


Figure 18: Synchronized Operation, 48V_{IN}, 5A Out, 170kHz.

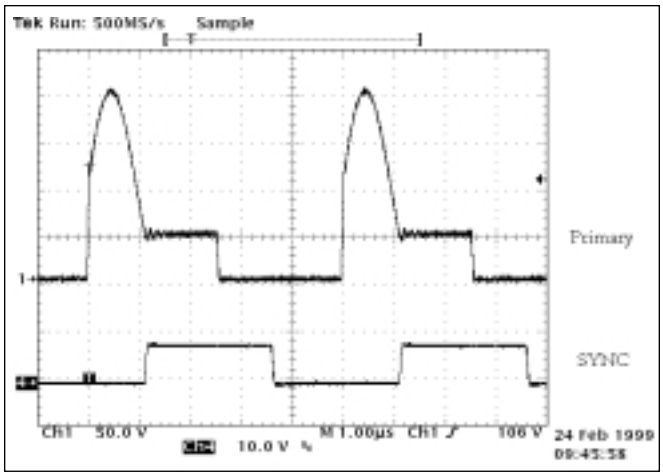


Figure 19: Synchronized Operation, 48V_{IN}, 5A Out, 200kHz.

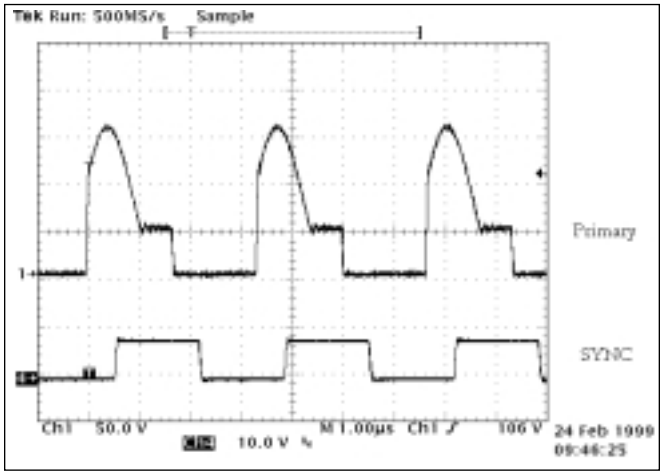


Figure 20: Synchronized Operation, 48V_{IN}, 5A Out, 300kHz.

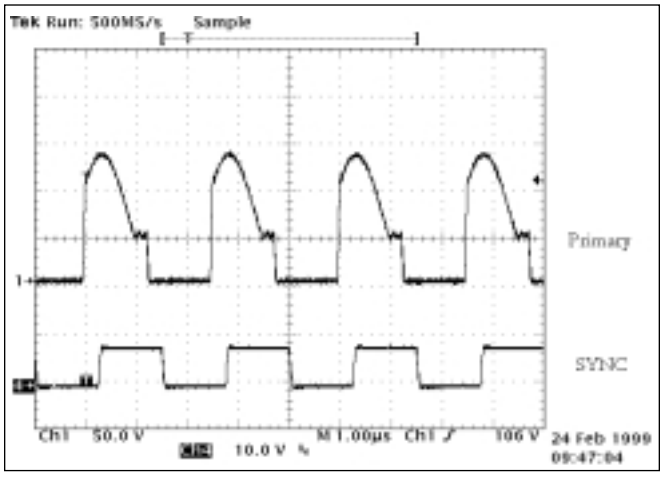


Figure 21: Synchronized Operation, 48V_{IN}, 5A Out, 400kHz.

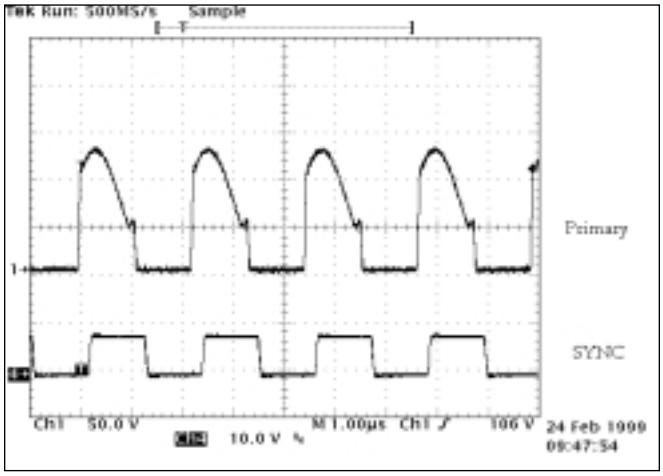


Figure 22: Synchronized Operation, 48V_{IN}, 5A Out, 450kHz.

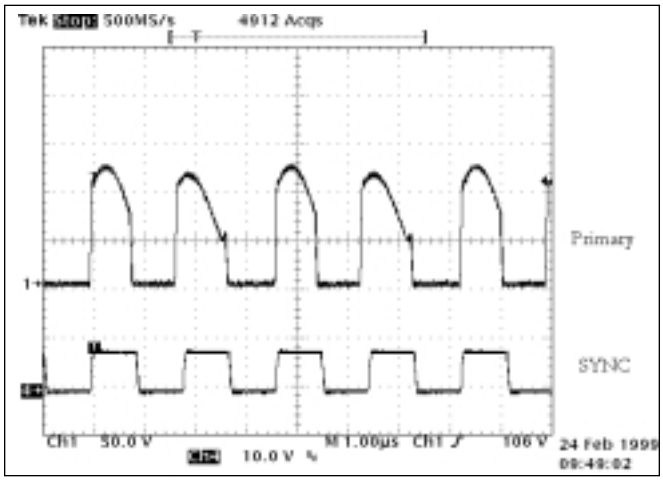


Figure 23: Synchronized Operation, 48V_{IN}, 5A Out, 550kHz. (Note the subharmonic oscillation when a new PWM cycle starts during the high dv/dt portion transformer reset.)

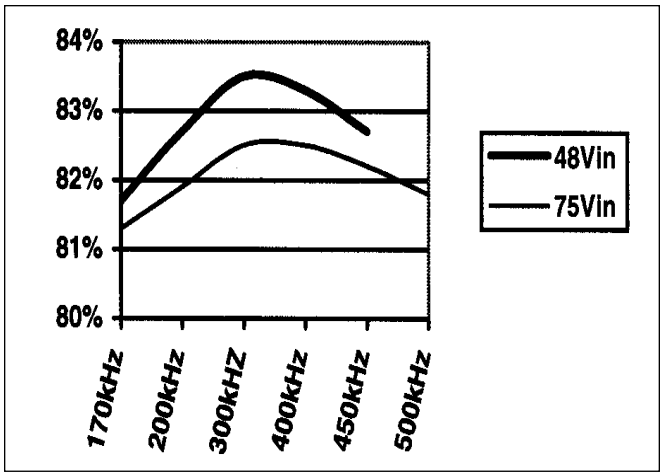


Figure 24: Efficiency During Synchronized Operation at Full Load.

Location	1A Output	5A Output	Shorted Output (~7.6A)
Ambient	25°C	26°C	28°C
PCB (near the V_{CC} TP)	35°C	45°C	50°C
U1	48°C	60°C	66°C
U2	33°C	47°C	60°C
Q2	45°C	63°C	65°C
T1	35°C	70°C	95°C
T2	50°C	73°C	70°C
D1	39°C	83°C	111°C

Figure 25: Component Temperature vs. Load at 75V_{IN}.

Location	200kHz	300kHz	450kHz
Ambient	27°C	27°C	28°C
PCB (near the V_{CC} TP)	46°C	46°C	49°C
U1	60°C	65°C	71°C
U2	46°C	46°C	47°C
Q2	62°C	64°C	73°C
T1	69°C	67°C	67°C
T2	73°C	67°C	70°C
D1	83°C	83°C	83°C

Figure 26: Component Temperature vs. Frequency at 48 V_{IN}, 5A Out.

Bill of Materials

Converter Bill of Material					
Item	**Qty.**	**Reference**	**Part**	**Mfg. & P/N**	**Distributor**
1	2	C1, 2	cer, 1.5µF, 100V	TDK C5750XR72A155K	TDK 603-886-6600
2	1	C3	cer, 0.22µF, 100V, 1206	Kemet C1206C224M5UAC	Newark 800-463-9275
3	2	C4, 10	cer, 1000pF, 50V, 0805	Panasonic ECU-V1H102KBN	Digi-Key
4	1	C5	0.47µF, 25V, 1206	Panasonic ECJ-3YB1E474K	Digi-Key
5	1	C6	cer, 390pF, 500V	Novacap 1206X391M501N	Novacap 661-295-5920
6	2	C7, 8	47µF, 6.3V	Panasonic EEFCDOJ470R	Digi-Key
7	2	C9, 11	cer, .01µF, 50V, 0805	Panasonic ECU-V1H103KBG	Digi-Key
8	1	C12	cer, .022µF, 50V, 0805	Panasonic ECU-V1H223KBG	Digi-Key
9	1	D1	schottky, dual	Motorola MBRD2060CT	Newark
10	1	D2	diode	Motorola MMBD6100LT1	Newark
11	1	D3	zener diode	Panasonic Digi-Key MA3110TR-ND	Digi-Key
12	1	L1	Inductor, 10µH	J.W. Miller PM54-100M	Newark
13 14	1	Q1	Transistor, NPN	Zetex FZT493	Digi-Key
15	1	Q2	MOSFET, 250V	I.R. IRF634S	Newark
16	1	R1	res, 39k, 0805	Panasonic ERJ-6GEYJ393V	Digi-Key
17	1	R2	res, 200k, 1%, 0805	Panasonic ERJ-6ENF2003V	Digi-Key
18	1	R3	res, 30.1K, 0805	Panasonic ERJ-6ENF3012V	Digi-Key
19	1	R4	res, 0.2ohm, 1% 1206	Dale WSL1206R200FE25	Allied 800-433-5700
20	1	R6	res, 17.4k, 0805	Panasonic ERJ-6ENF1742V	Digi-Key
21	1	R7	res, 1k, 0805	Panasonic ERJ-6GEYJ103V	Digi-Key
22	1	R8	res, 10k, 1%, 0805	Panasonic ERJ-6ENF1002V	Digi-Key
23	2	R9, 10	res, 10k, 0805	Panasonic ERJ-6GEYJ103V	Digi-Key
24	1	T1	Inductor with aux. winding	Coiltronics CTX15-14527	Coiltronics 561-241-7876
25	1	T2	Transformer, forward	Coiltronics CTX15-14526	Coiltronics
26	1	U1	Current Mode Controller	ON Semiconductor CS5126-DR8	ON Semiconductor 401-885-3600
27	1	U2	Opto-isolator	Motorola / QT Optoelectronics MOC8106	Arrow Electronics 516-391-1300
28	1	U3	Shunt Regulator	Texas Instruments TLV431CDBV	Wyle Electronics 781-271-9953

Miscellaneous Bill of Material					
Item	**Qty.**	**Reference**	**Part**	**Mfg. & P/N**	**Distributor**
1	4	TP1, 2, 4, 5	turret terminal	Cambion 160-1558-02-01-00	Newark
2	10	TP3, 6-14	single pin header	Winpoint 201-01-S-3-02-T	
3	4	F1-4	standoff	Bumpons (Digi-Key) SJ5003-0-ND	Digi-Key

PCB Layout

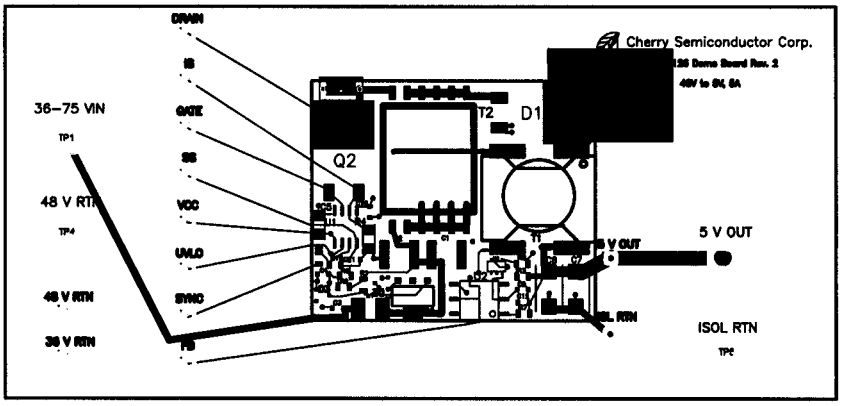


Figure 27: Top (component) Layer.

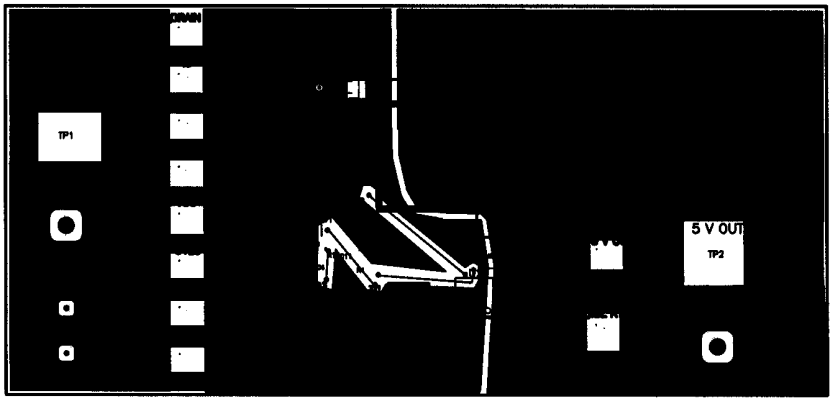


Figure 28: Bottom (solder) Layer.

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