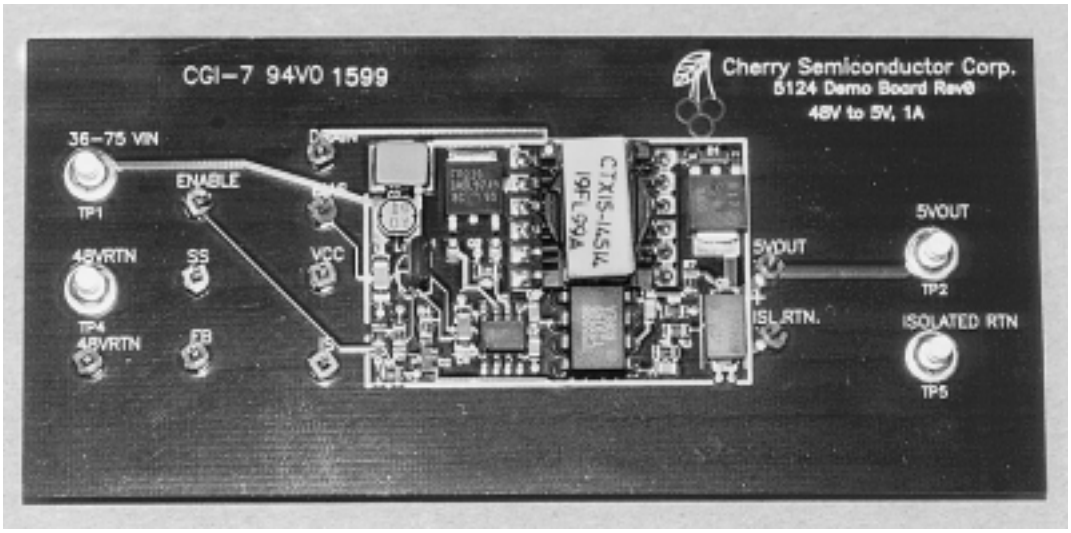
48V to 5V, 1A Flyback Converter

a CS5124 Demonstration Manual



September, 1999 - Rev. 0
CS5124DM

ON Semiconductor

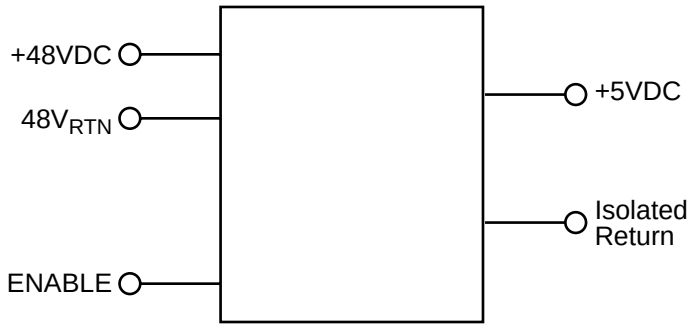
Description

The CS5124 Demonstration Board is a fixed frequency, isolated, 48VDC to 5VDC flyback converter. High efficiency over a wide input voltage range is accomplished by powering the CS5124 controller from a winding on the flyback transformer. Short circuit, overload, and input undervoltage protection are all accomplished by integrated CS5124 circuitry. The demonstration board also accomplishes bootstrapping, Soft Start and blanking with a minimal number of discrete components.

Features

- 36 to 75VDC Input Voltage Range
- 5V, 1A Isolated Output
- 1" × 1.6" Footprint
- Up to 82% Efficiency
- Input Undervoltage Shutdown and Sleep Mode
- Remote Enable Input
- Overcurrent Protection
- Thermal Shutdown

Applications Diagram



Pin Description

Pin Symbol	Pin Description
+48VDC	36 to 75 VDC Input.
48V$_{RTN}$	Return for +48VDC Input.
ENABLE	This pin is internally pulled up and performs the UVLO function if left open. Pull this pin to between 2.25V and 2.5V to stop the converter from switching. Pull this pin to below 1.5V to put the converter in sleep mode.
+5VDC	+5VDC Isolated Output.
Isolated Return	Return for +5VDC Output and load.

Absolute Maximum Ratings

T_A = 25°C			
Input/Output Name	**Minimum**	**Maximum**	**Units**
+48VDC	–0.3	80.0	Volts
Output Current		Internally Limited	Amps
ENABLE	–0.3	6.0	Volts
Isolated Return	–500	+500	VDC

Electrical Characteristics

T_A = 25°C, 36V to 75V, unless otherwise specified.					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	$0.15A < I_{OUT} < 1A$	4.85	5.00	5.15	V
Load Reg.	$0.15A < I_{OUT} < 1A$ $36V < V_{IN} < 75V$		0.25		%
Line Reg.	$0.15 < I_{OUT} < 1A$ $36V < V_{IN} < 75V$		0.15		%
Transient Regulation and Recovery Time to within 1%	Step between 50% and 75% of maximum load.		100 200		mV µs
Output Ripple and Noise	$75V_{IN}$ @ Full Load (20MHz BW)		200 20		mV_{p-p} mV_{rms}
Efficiency	0.2A Out 1A Out		72 82		% %
Enable (Turn-on) Threshold		2.30	2.63	2.76	V
Enable Hysteresis		170	185	200	mV
Sleep Mode (Turn-off) Threshold		1.50	1.83	2.30	V
Sleep Mode Hysteresis		35	85	150	mV
Enable Pin Source Current	Enable Pin = 0V			1	mA
Sleep Mode Input Current	$75V_{IN}$		650	1000	µA
Enable / S.S. Time	Full Load		5		ms
Undervoltage Lockout (Turn-off)		28	31	33	V
Undervoltage Lockout (Turn-on)		31	33	35	V
Undervoltage Lockout Hysteresis			2		V
Overcurrent Limit Threshold	V_{IN} = 36V V_{IN} = 75V		1.2 1.7		A
Oscillator Freq.		380	400	420	kHz

Operating Instructions

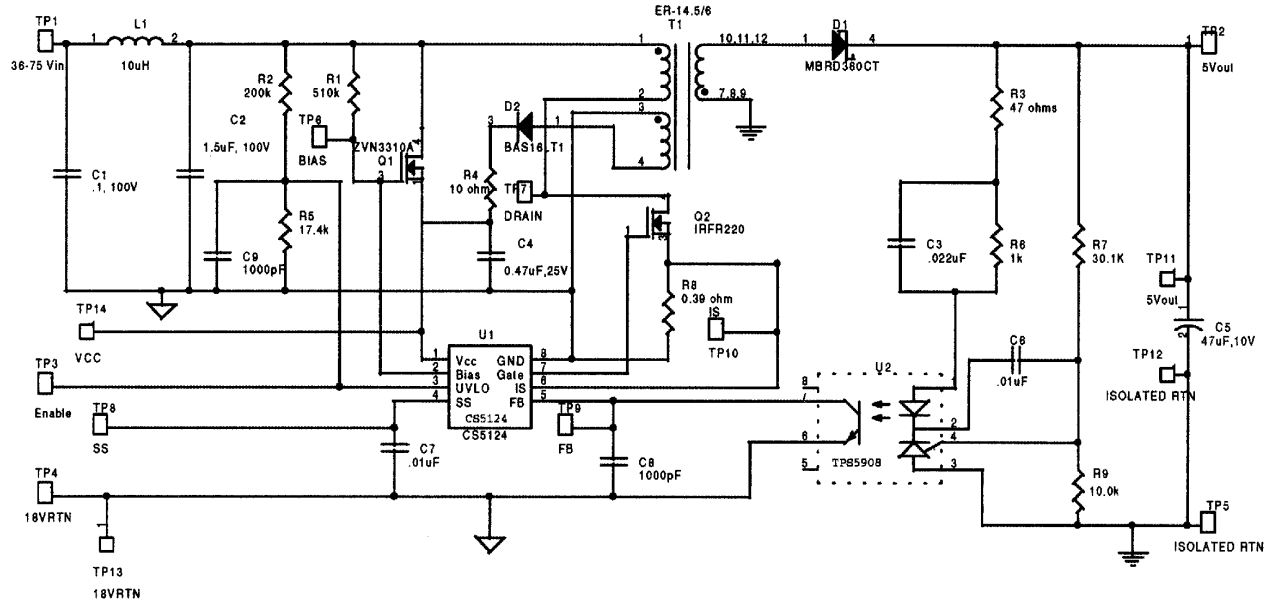
Input Power

The converter is designed to run with an input voltage between 36VDC to 75VDC. Approximately 180mA of current will be required for full load with a 36V input.

Output Load

An external load is required for the demo board to run normally at fixed frequency. If the demo board is run with a load less than about 80mA it will regulate the output at 5V in hiccup mode.

Circuit Schematic



Theory of Operation

Enable/UVLO

R2 and R5 form a divider for the UVLO function. If the ENABLE pin of the supply is left open it will operate in three modes depending on the input voltage. For V_{IN} less than 18V the supply will be in sleep mode. For V_{IN} between approximately 18V and 31V the BIAS section is operational and V_{CC} is regulated to 8V, but the PWM section is disabled. If V_{IN} exceeds 35V the supply operates normally.

C9 is included on the demonstration circuit to prevent radiated noise from coupling to the ENABLE pin through the ENABLE test point. This part may not be needed with a more typical pcb layout.

The ENABLE pin can also be controlled by open collector logic to perform an ENABLE function. When the ENABLE pin is below 1.5V the supply will be in sleep mode and input current will be less than 1mA.

V_{CC} Bias

R1 provides a pull-up to turn Q1 on and the BIAS pin sinks current to regulate V_{CC} or turn off Q1. When the IC is operational, but not powered by the flyback winding, V_{CC} will be regulated to 8V by the BIAS pin and Q1. During normal operation, when sufficient energy to power the controller is available from the flyback winding, V_{CC} rises above 8V and the BIAS pin turns Q1 off.

Current Sensing

R8 is the current sense resistor. The turn-on spikes, shown in Figures 11-13, are blanked internally by the CS5124.

During heavy load conditions the primary current is pulse by pulse limited as shown in Figure 14. Under conditions where the current sense pin measures high

Theory of Operation

currents with fast rise-times the CS5124 second threshold will be exceeded the converter will enter a low duty cycle hiccup mode as shown in Figures 15 and 16. The CS5124 Demonstration Board typically reaches this condition only when the input voltage is greater than 65V and there is a low impedance short across the output pins.

Soft Start & Hiccup Mode

Soft Start capacitor C7 determines the Soft Start time during turn-on, and the dead time when the supply is operating in hiccup mode. During Soft Start there will be a dead time of about 1.5ms while C7 charges to 1.6V. The ramp-up time of the output voltage will last about 1-2ms depending on output load.

During hiccup mode the dead time will be about 1.4ms while C8 charges from 0.25V to 1.6V as shown in Figure 16.

Feedback

R7 and R9 divide the 5V output to the 1.24V reference of U2. C6 and the thevenin resistance of R7 and R9 set the low frequency roll-off of U2. R6 sets the maximum current through U2's photodiode and adjusts gain. C3 provides phase boost near the crossover frequency. C8 is primarily for high frequency noise reduction.

Design Information

Flyback Transformer

The transformer was designed to operate in continuous and discontinuous conduction modes. Running in discontinuous conduction mode at light loads allows for a smaller core size, and by requiring a higher peak current offers a larger current sense signal. Operating in continuous conduction mode during at heavy loads reduces ripple current in the output filter capacitor.

The transformer also runs at less than 50% duty cycle under all conditions. This eliminates the need to choose the transformer inductance to meet slope compensation criteria and in a continuous flyback converter lower duty cycle means lower output filter capacitor ripple.

The V_{CC} flyback winding powers the controller and is clamped to a voltage proportional to the secondary voltage. If the initial turn-off spike is snubbed this winding will provide a regulated Vcc voltage. To provide Vcc power from the flyback winding rather than the bias circuit during normal operation, the number of turns should be chosen to to provide more than 9V under operating conditions.

Flyback Transformer Design Procedure

1. Choose duty cycle less than 50% at low line. For a 400kHz nominal operating frequency choose T_{ON} = 1.1µs and T_{OFF} = 1.4µs with $36V_{IN}$.

2. Choose primary to secondary ratio.

$$\frac{N_P}{N_S} = \frac{T_{ON}}{T_{OFF}} \times \frac{V_{IN}}{V_{OUT}} = \frac{1.1\mu s}{1.4\mu s} \times \frac{36V}{5.4V} = \frac{5.2}{1}$$

3. Choose auxiliary to secondary ratio.

$$\frac{N_A}{N_S} = \frac{V_{CC} + 0.7V + I_{CC} \times R_{SNUB} \times 2}{V_{OUT} + 0.4V}$$

$$= \frac{11.7 + 10mA \times 10\Omega \times 2}{5.4V} = \frac{2.2}{1}$$

4. Calculate the minimum primary inductance so that the on time at minimum load and maximum V_{IN} is longer than CS5124 blanking plus propagation delay time. (See CS5124 Data Sheet.) Minimum Load is chosen to be 60mA.

$$L \geq \frac{V^2 \times D^2}{P_{MIN} \times Freq \times 2}$$

$$= \frac{75^2 \times 0.124^2}{0.52W \times 400kHz \times 2} = 208\mu H$$

where

$$D = (T_{BLANK} + T_{PROP}) \times Freq$$

$$= (130ns + 180ns) \times 400kHz = 0.124$$

and

$$P_{MIN} = \frac{(V_{OUT} \times I_{OUT}) + P_{CS5124}}{Efficiency}$$

$$= \frac{(5.3V \times 60mA) \times 100mW}{0.8} = 52W$$

Design Information continued

5. Choose core type and design the transformer using standard techniques. The winding sheet for the demo board transformer is shown below.

2/1/1999 5124 Flyback Transformer

ITEM	DESCRIPTION	
CORE	Coiltronics ER14.5, AL-2	AL = 2.16E-07
BOBBIN		MLT = 1.06
TAPE		
CLIP		

TRANSFORMER WINDING DATA

LEAD TERM	LEAD TERM	TURNS	WIRE SIZE	# of Wires	RNOM	LNOM	NOTES
	2						
		30	32	1	0.431	1.9E-04	1, 2
	4						
		14	32	1	0.201	4.2E-05	1
10, 11, 12							
7, 8, 9	1 3	6	31	3	0.023	7.8E-06	1

NOTES

1. Start all windings together. (The number of turns are the total for each winding.)
2. Finish with tape.
3. A minimum of 500V isolation is required.

Output Filter

Figure 1A shows the output filter ripple currents at low line and full load. The lower left section shows current supplied to the output by the output filter while the main switch (Q2) is on. The lower right section shows current supplied to the output by the transformer secondary when Q2 is off (during flyback). The upper right shows current supplied by the transformer secondary to recharge the output filter. The total charge in the upper right section must be equal the (dis)charge in the lower left during steady state. The RMS current in the output filter capacitor (C5) is ≅ 1A.

Due to the high di/dt in the output filter of flyback converters, spikes on the output are nearly impossible to eliminate with one filter stage. In this design the output filter sees approximately a 2A step current in 50ns. With such a high di/dt just 3nH (a typical via is 0.7nH) of inductance in a single stage output filter will produce a 120mV spike. See Figure 6. If this spike is unacceptable a second filter stage, as shown in Figure 1B, using a ferrite bead (Steward HI0805N410R) and a ceramic capacitor can reduce the spike to the magnitude shown in Figure 7. (The feedback connection should also be moved to connect to the 1µF filter capacitor.)

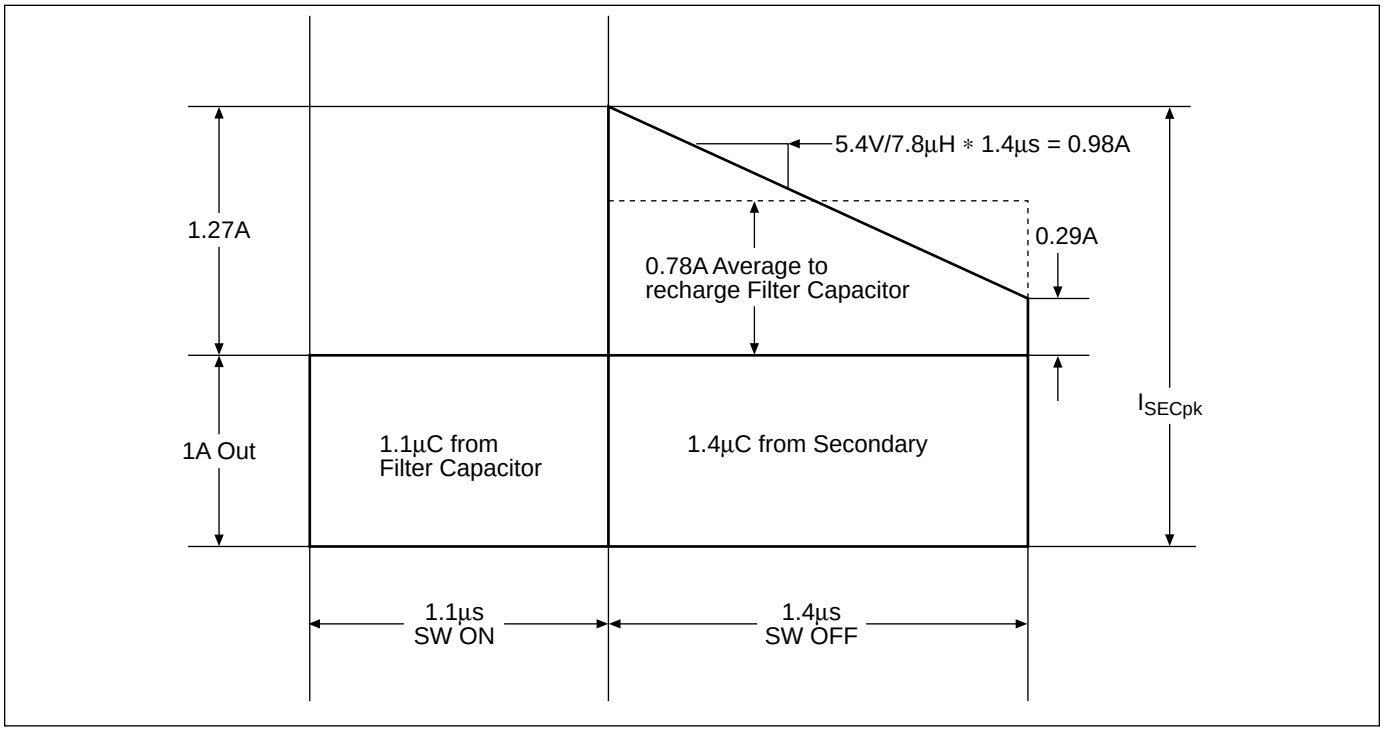


Figure 1A. Output Filter Currents.

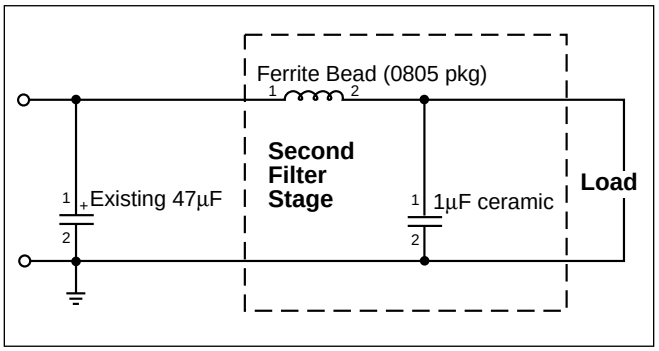


Figure 1B. Second Output Filter Stage.

Current Sense Resistor Selection

The current sense resistor (R8) value is chosen to keep the peak voltage of the current sense waveform below the CS5124 1st Threshold during normal operation. The peak primary current can be calculated by dividing the secondary peak current (in Figure 1A) by the transformer ratio.

$$I_{PRIpk} = I_{SECpk} \times \frac{N_S}{N_P} = 2.27A \times \frac{6}{30} = 0.45A$$

The First Current Sense Threshold decreases with higher duty cycles and should be calculated at maximum duty cycle.

$$\text{CS5124 1st Threshold} = \frac{2.9V - 170mV/\mu s \times T_{ON}}{10} - 60mV$$

$$= \frac{2.9V - 170mV/\mu s \times 1.1\mu s}{10} - 60mV$$

$$= 211mV$$

The current sense resistor with a 20% margin is:

$$R_{SENSE} = \frac{\text{1st Threshold}}{I_{PRIpk} \times 1.2} = \frac{211mV}{0.45V \times 1.2} = 391m\Omega$$

Typical Performance Characteristics

The figures below show typical performance of the CS5124 Demo Board. Unless noted all waveforms were taken with the 20MHz filter option selected on the oscilloscope.

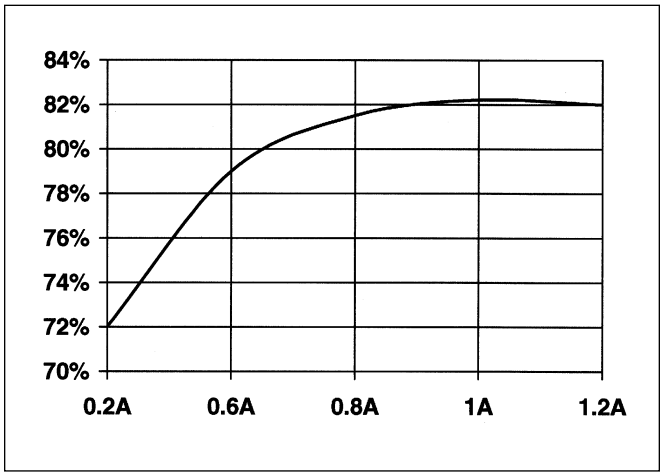


Figure 2: Typical Output Efficiency at $48V_{IN}$.

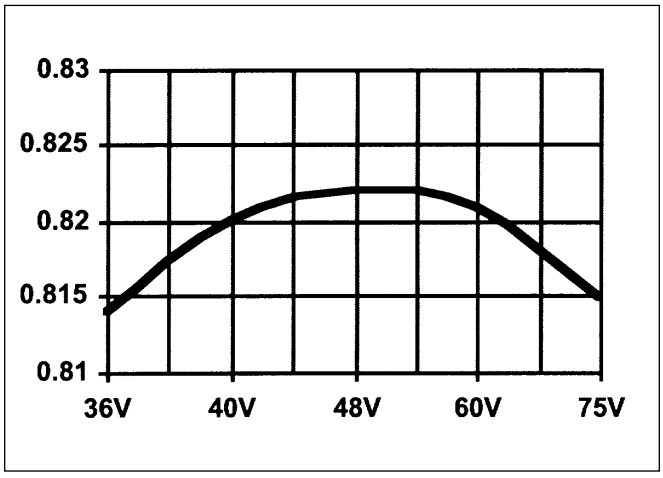


Figure 3: Typical Output Efficiency at 1A Out.

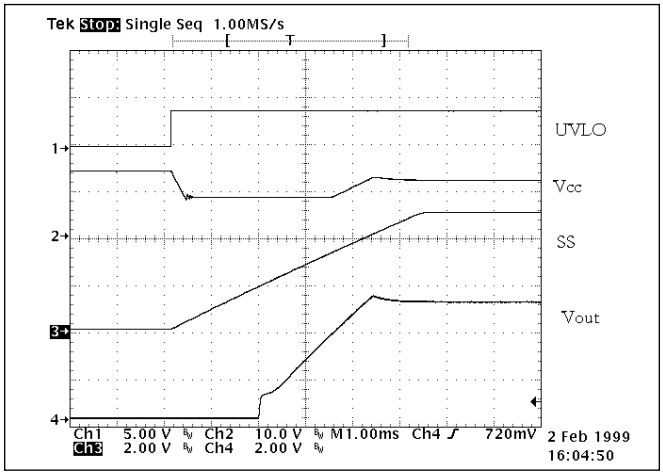


Figure 4: Start-up Waveforms at $48V_{IN}$, 1A Load.

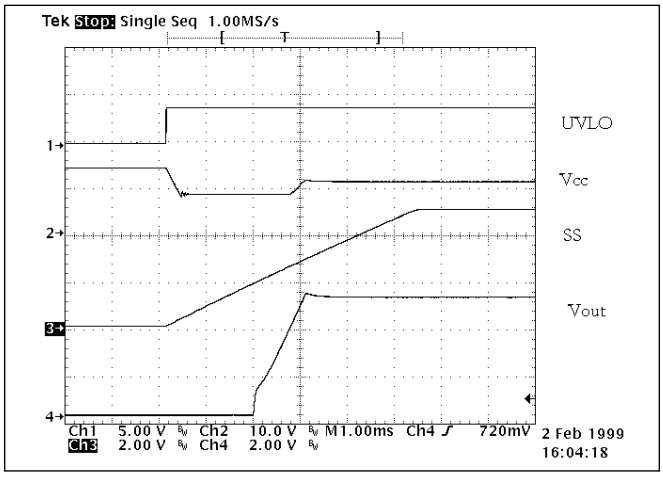


Figure 5: Start-up Waveforms at $48V_{IN}$ with 0.17A Load.

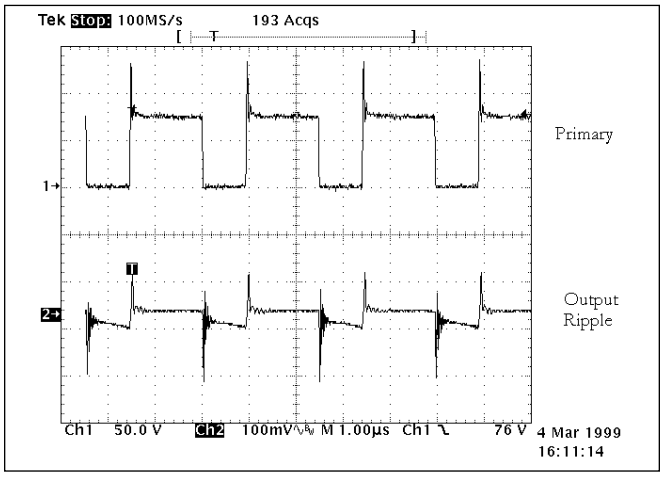


Figure 6: Primary Voltage and Output Ripple at $36V_{IN}$, 1A Out.

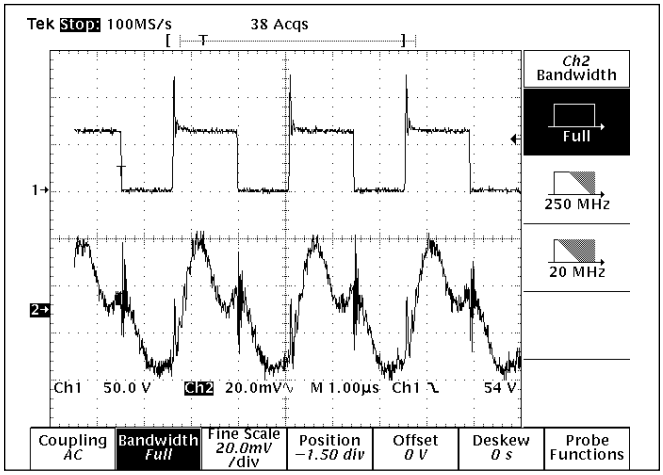


Figure 7: Primary Voltage and Output Ripple with Additional Filter Stage; Ferrite Bead and 1µF Ceramic Capacitor — Full Bandwidth Measurement.

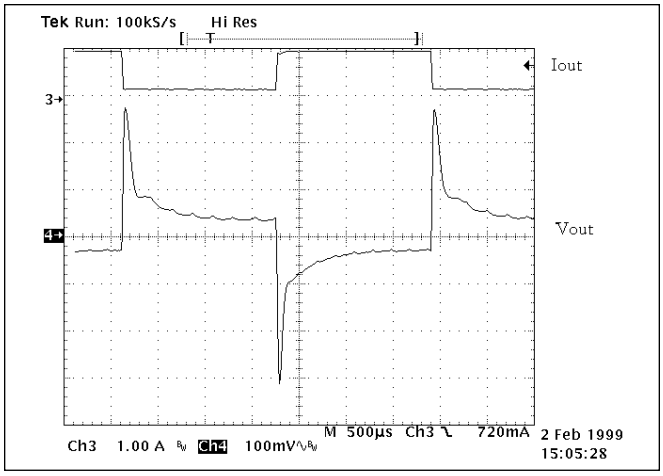


Figure 8: Transient Response 0.17A to 1A Step.

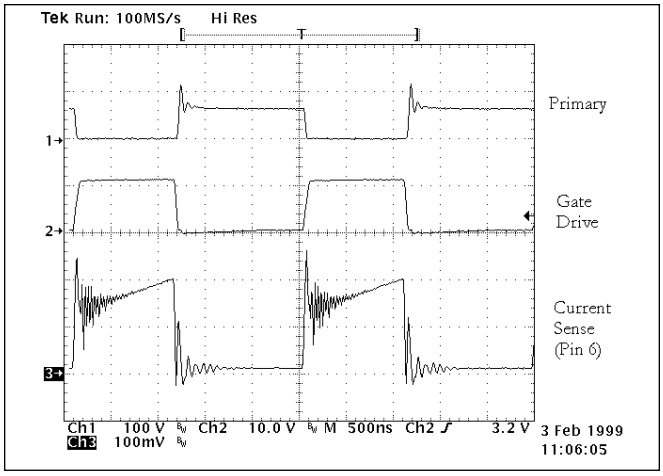


Figure 11: Current Sense 36V_{IN}, 1A out.

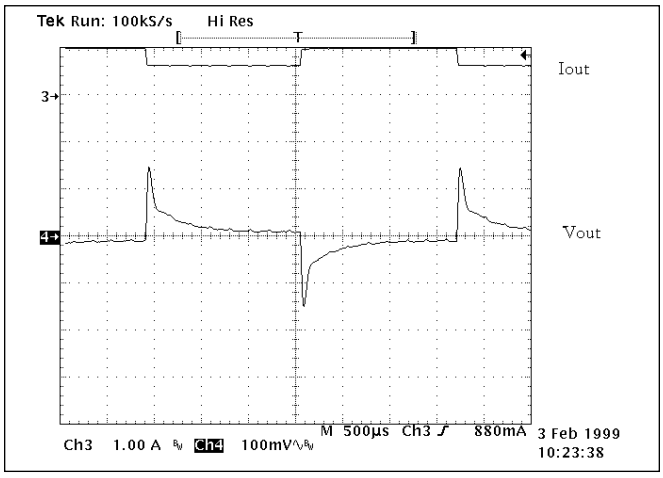


Figure 9: Transient Response 0.6A to 1A Step.

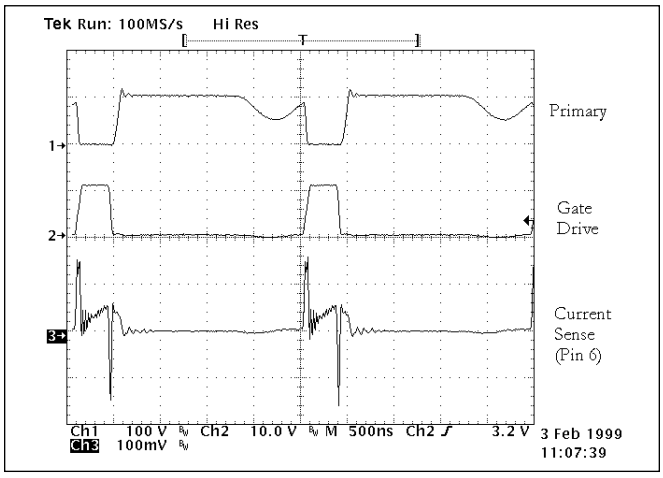


Figure 12: Current Sense 75V_{IN}, 0.15A Out.

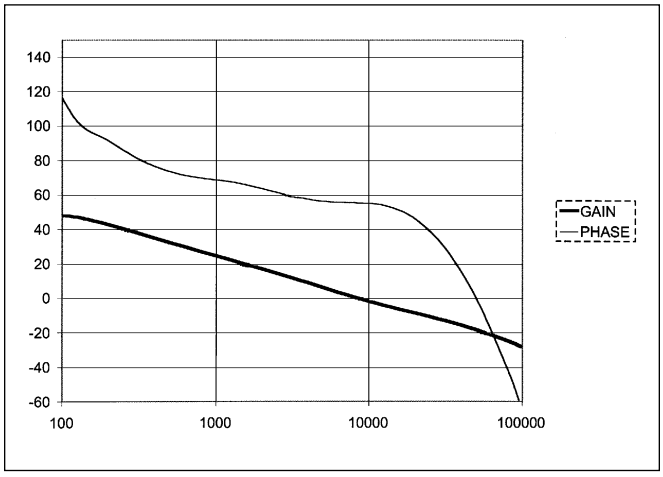


Figure 10: Control Loop at 48V_{IN}, 0.5A Out.

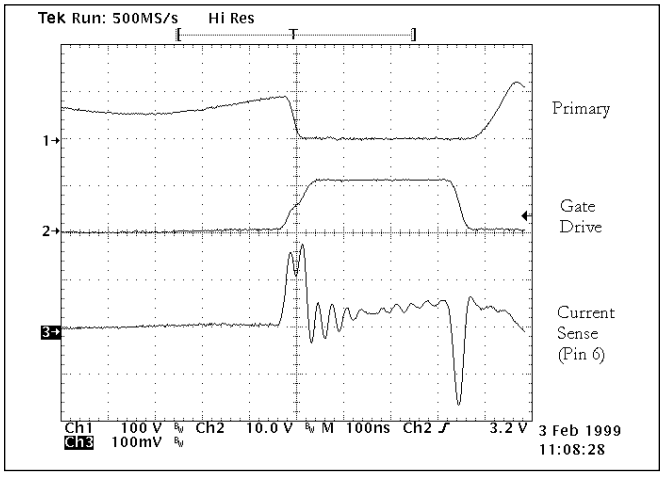


Figure 13: Current Sense 75V_{IN}, 0.15A Out Expanded.

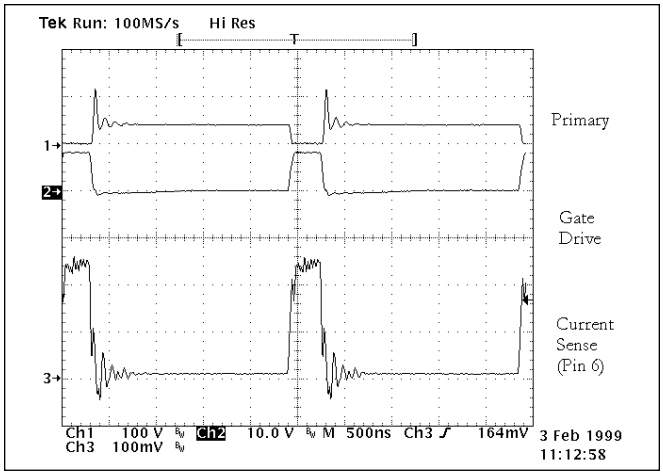


Figure 14: Current Sense 36V_{IN}, Output Shorted.

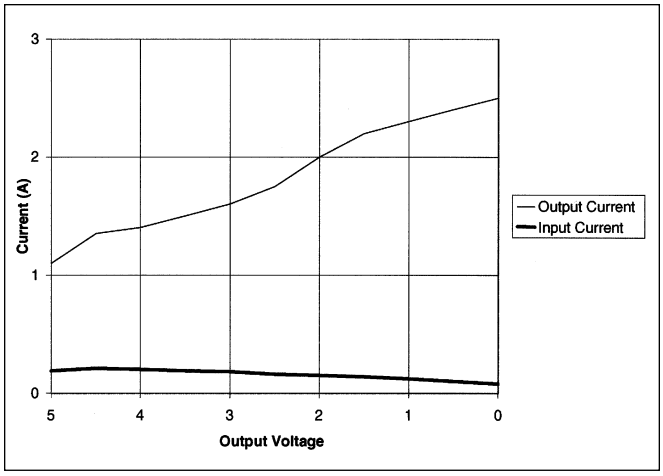


Figure 17: V-I Curves During High Output Currents and 36V_{IN}.

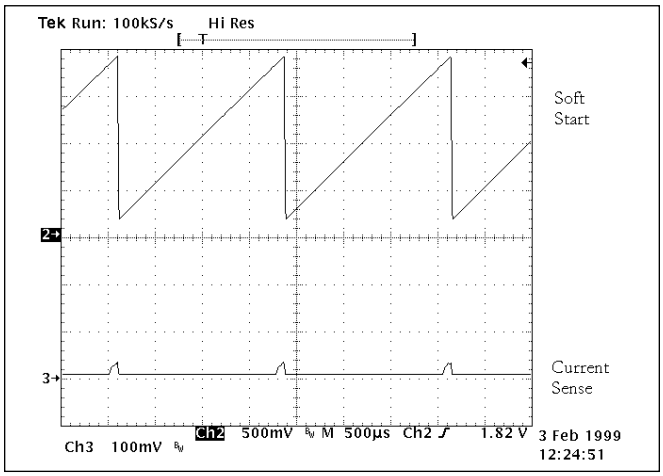


Figure 15: Second Threshold Operation 75V_{IN}, Output Shorted. (Current Sense pulses are attenuated due to sampling frequency.)

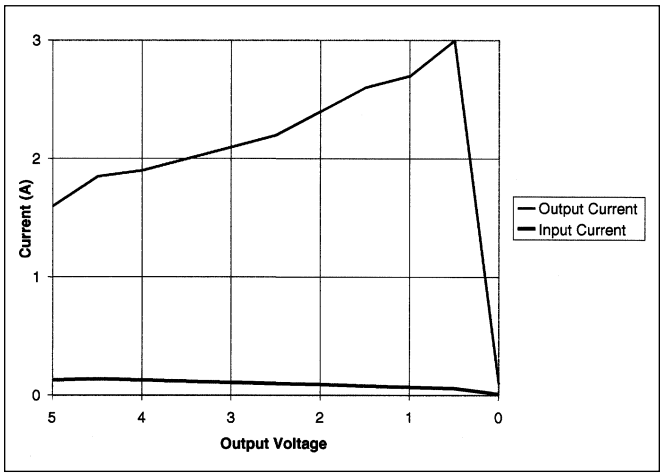


Figure 18: V-I Curves During High Output Currents and 75V_{IN}. (Low currents near 0V_{OUT} occur during hiccup mode.)

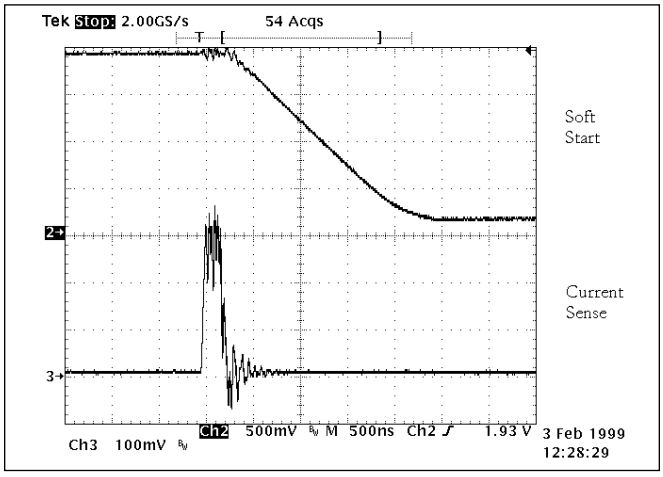


Figure 16: Second Threshold Operation — the last Pulse Before Soft Start, 75V_{IN}, Output Shorted.

Location	0.15A Output	1A Output	Shorted Output (~2.5A)
Ambient	24°C	25°C	26°C
PCB (below U1 & U2)	27°C	31°C	37°C
U1	42°C	46°C	52°C
U2	28°C	36°C	46°C
Q2	31°C	40°C	46°C
T1	30°C	45°C	67°C
D1	28°C	43°C	72°C

Figure 19: Component Temperature at 48V_{IN}.

Bill of Materials

Converter Bill of Materials					
Item	**Qty**	**Reference**	**Part**	**Mfg. & P/N**	**Distributor**
1	1	C1	cer, 0.1µF, 100V, 1206	Kemet C1206C104M5UAC	Newark 800-463-9275
2	1	C2	cer, 1.5µF, 100V	TDK C5750XR72A155K	TDK 603-886-6600
3	1	C3	cer, 0.022µF, 50V, 0805	Panasonic ECU-V1H223KBX	Digi-Key 800-344-4539
4	1	C4	0.47µF, 25V, 1206	Panasonic ECJ-3YB1E474K	Digi-Key
5	1	C5	47µF, 6.3V	Panasonic EEFCDOJ470R	Digi-Key
6	2	C6, C7	cer, 0.01µF, 50V, 0805	Panasonic ECU-V1H103KBG	Digi-Key
7	2	C8, C9*	cer, 1000pF, 50V, 0805	Panasonic ECU-V1H102KBN	Digi-Key
8	1	D1	Schottky	Motorola MBRD360CT	Newark
9	1	D2	Diode	Motorola BAS16LT1	Newark
10	1	L1	Inductor, 10µH	J.W. Miller PM43-100M	Newark
11	1	Q1	MOSFET, 100V	Zetex ZVN3310A	Digi-Key
12	1	Q2	MOSFET, 200V, 0.8Ω	International Rectifier IRFR220	Newark
13	1	R1	res, 510k, 0805	Panasonic ERJ-6GEYJ514V	Digi-Key
14	1	R2	res, 200k, 1%, 0805	Panasonic ERJ-6ENF2003V	Digi-Key
15	1	R3	res, 47Ω, 0805	Panasonic ERJ-6GEYJ470V	Digi-Key
16	1	R4	res, 10Ω, 0805	Panasonic ERJ-6GEYJ100V	Digi-Key
17	1	R5	res, 17.4k, 0805	Panasonic ERJ-6ENF1742V	Digi-Key
18	1	R6	res, 1k, 0805	Panasonic ERJ-6GEYJ103V	Digi-Key
19	1	R7	res, 30.1K, 0805	Panasonic ERJ-6ENF3012V	Digi-Key
20	1	R8	res, 0.39Ω, 1%, 0805	Panasonic ERJ-6RQFR39V	Digi-Key
21	1	R9	res, 10k, 1%, 0805	Panasonic ERJ-6ENF1002V	Digi-Key
22	1	T1	Transformer	Coiltronics CTX15-14514	Coiltronics 561-241-7876
23	1	U1	Current Mode Controller	ON Semiconductor CS5124-DR8	ON Semiconductor 401-885-3600
24	1	U2**	Optoisolated Feedback Amp.	Texas Instruments TPS5908	Wyle 781-271-9953

*For the Rev-0 printed circuit, C9 is a leaded component on the solder side.

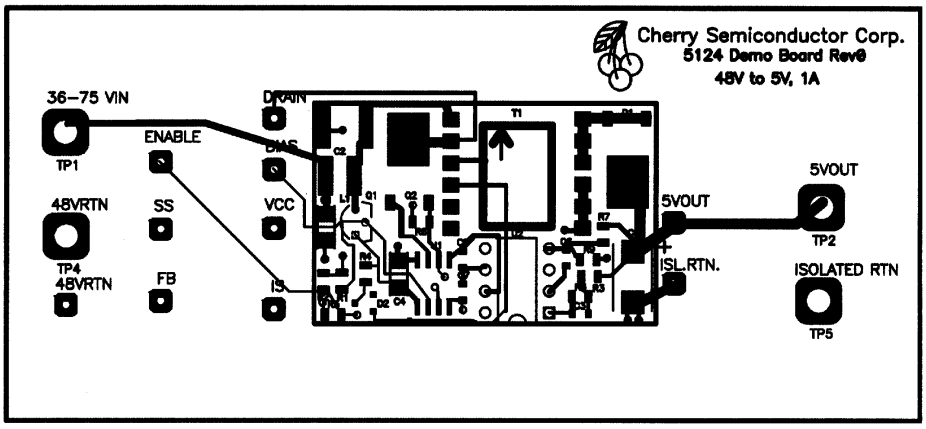
**TPS5908 is now an obsolete part and may be replaced by a TLV431 and an MOC8106.

Bill of Materials continued

Miscellaneous Bill of Materials					
Item	**Qty**	**Reference**	**Part**	**Mfg. & P/N**	**Distributor**
1	4	TP1, 2, 4, 5	turret terminal	Cambion 160-1558-02-01-00	Newark
2	10	TP3, 6-14	single pin header	Winpoint 201-01-S-3-02-T	
3	4	F1-4	standoff	Bumpons (Digi-Key) SJ5003-0-ND	Digi-Key

PCB Layout

Top (Component) Layer



Bottom (Solder) Layer