CS51227

Enhanced Voltage Mode PWM Controller

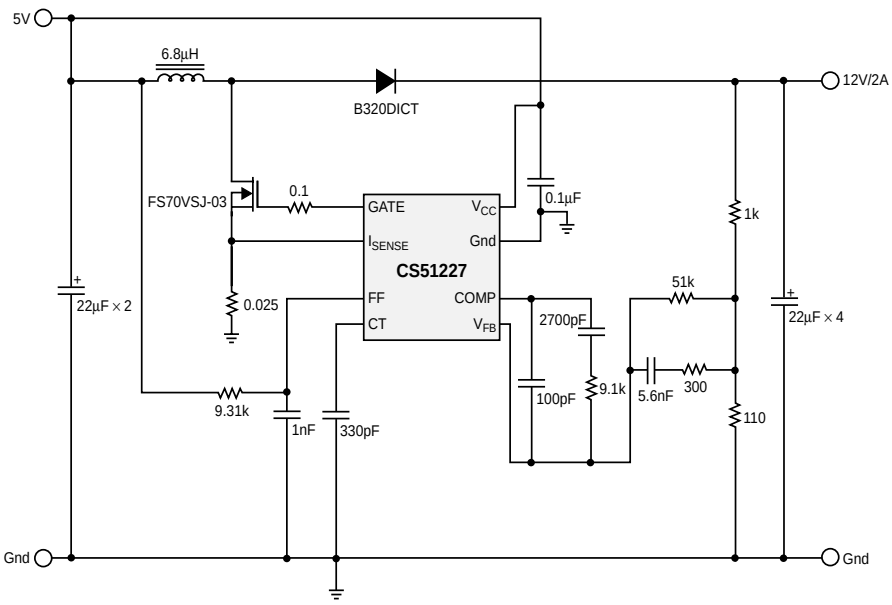
Description

The CS51227 is a fixed frequency, single output PWM controller using feed forward voltage mode control. Feed forward control provides superior line regulation and line transient response. This PWM controller has been optimized for high frequency primary side control operation. It has undervoltage lockout with 4.7V start up voltage and 75µA start up current. One external capacitor can program the switching frequency up to 1MHz. The protection features include pulse-by-pulse current limit with leading edge blanking and thermal shutdown. The CS51227 is available in 8 lead SO narrow surface mount package.

Features

- 1MHz Frequency Capability
- 4.7V Start-Up Voltage
- Fixed Frequency Voltage Mode Operation with Feed Forward
- Undervoltage Lockout
- 75µA Start-Up Current
- Thermal Shutdown
- 1A Sink/Source Gate Drive
- Pulse By Pulse Current Limit with Leading Edge Blanking
- 50ns GATE Rise and Fall Time (1nF load)
- Maximum Duty Cycle Over 85%
- Programmable Volt-Second Clamp

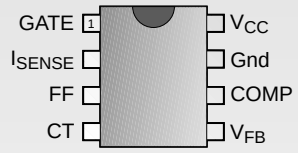
Applications Diagram



5V to 12V/2A Boost Converter

Package Options

8 Lead SO Narrow



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Absolute Maximum Ratings

Pin Symbol	Lead Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
GATE	Gate Drive Output	20V	–0.3V	1.0A Peak 200mA DC	1.0A Peak 200mA DC
I_{SENSE}	Current Sense Input	6V	–0.3V	1mA	1mA
CT	Timing Capacitor	6V	–0.3V	1mA	10mA
FF	Feed Forward	6V	–0.3V	1mA	25mA
COMP	Error Amp Output	6V	–0.3V	10mA	20mA
V_{FB}	Feedback Voltage	6V	–0.3V	1mA	1mA
V_{CC}	Power Supply	20V	–0.3V	10mA	1.0A Peak 200mA DC
Gnd	Ground	N/A	N/A	1.0A Peak 200mA DC	N/A

Operating Junction Temperature, T_J ..... 150°C
Storage Temperature Range, T_S ..... –65° to 150°C
ESD (Human Body Model) 2kV
Lead Temperature Soldering: Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: –40°C < T_A < 85°C; –40°C < T_J < 125°C; 4.7V < V_{CC} < 18V; C_T = 390pF; unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Start/Stop Voltages					
Start Threshold		4.4	4.5	4.7	V
Stop Threshold		3.2	3.8	4.2	V
Hysteresis	Start – Stop	300	700	1400	mV
I_{CC} @ Startup	V_{CC} < UVL Start Thresh.		38	75	µA
■ Supply Current					
I_{CC} Operating	No load		10	16	mA
■ Overcurrent Protection					
Over Current Threshold	Ramp I_{SENSE}	0.27	0.30	0.33	V
I_{SENSE} to GATE Delay	V_{FB} = 0.5V (no blanking)		60	125	ns
■ Error Amp					
Reference Voltage	V_{FB} connected to COMP	1.234	1.263	1.285	V
V_{FB} Input Current	V_{FB} = 1.25V		1.3	2.0	µA
Open Loop Gain	(Note 1)	60	90		dB
Unity Gain Bandwidth	(Note 1)	1.5	2.5		MHz
COMP Sink Current	COMP = 1.4V, V_{FB} = 1.45V	3	12	32	mA
COMP Source Current	COMP = 1.4V, V_{FB} = 1.15V	1.0	1.7	2.4	mA
COMP High Voltage	V_{FB} = 1.15V	2.8	3.1	3.4	V
COMP Low Voltage	V_{FB} = 1.45V	75	150	300	mV
PSRR	Freq = 120Hz (Note 1)	60	85		dB

Electrical Characteristics: –40°C < T_A < 85°C; –40°C < T_J < 125°C; 4.7V < V_{CC} < 18V; C_T = 390pF; unless otherwise stated.

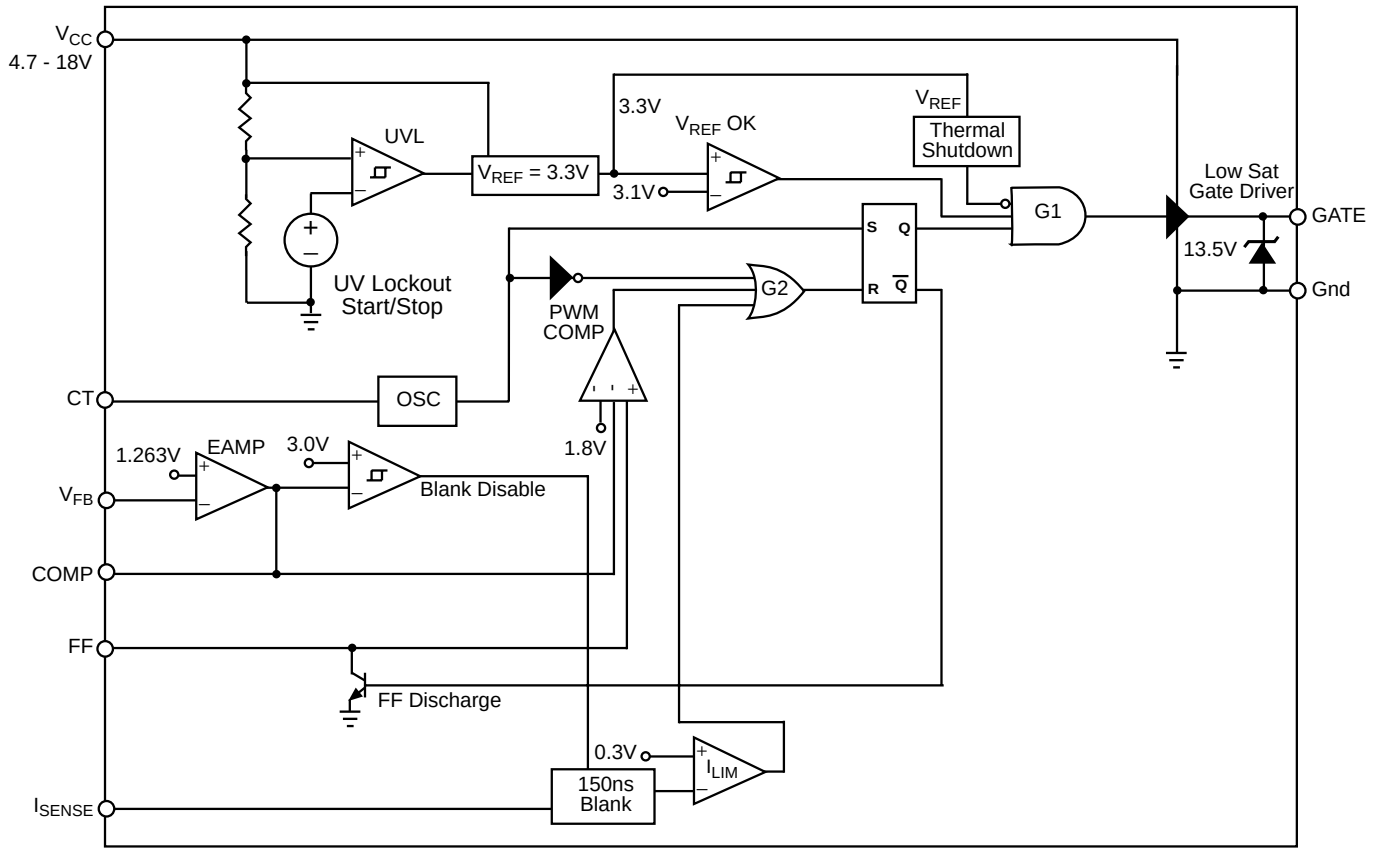
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Oscillator					
Frequency Accuracy		200	235	270	KHz
Max Duty Cycle		85	90	95	%
Peak Voltage	(Note 1)	1.99	2.05	2.11	V
Valley Clamp Voltage		0.90	0.95	1.00	V
Valley Voltage	(Note 1)	0.90	0.95	1.00	V
Discharge Current		0.85	1.00	1.15	mA
Charge Current		95	115	135	µA
■ Gate Driver					
High Saturation Voltage	$V_{CC} - V_{GATE}$, V_{CC} = 10V, I_{SOURCE} = 150mA		1.5	2.0	V
Low Saturation Voltage	V_{GATE}, I_{SINK} = 150mA		1.2	1.5	V
High Voltage Clamp		11.0	13.5	16.0	V
Output UVL Leakage	V_{GATE} = 0V		1	50	µA
Rise Time	1nF load, V_{CC} = 18V, 1V < V_O < 9 V		32	50	ns
Fall Time	1nF load, V_{CC} = 18V, 9V < V_O < 1V		25	50	ns
Max GATE Voltage @ UVL	I_{LOAD} = 100µA	0.4	0.7	1.5	V
■ Feed Forward (FF)					
Discharge Voltage	I_{FF} = 2mA		0.3	0.7	V
Discharge Current	FF = 1V	2	16	30	mA
FF to GATE Delay		50	75	125	ns
FF Max Voltage	V_{FB} = 1.15V	1.7	1.8	1.9	V
■ Blanking					
Blanking Time		50	150	250	ns
COMP Blanking Disable Threshold	V_{FB} < 1V	2.8	3.0	3.3	V
■ Thermal Shutdown					
Thermal Shutdown	(Note 1)	125	150	180	°C
Thermal Hysteresis	(Note 1)	5	10	15	°C

Note 1: Guaranteed by design, not 100% tested in production.

Package Lead Description

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
8 Lead SO		
1	GATE	External power switch driver with 1.0A peak capability. Rail-to-rail output occurs when the capacitive load is between 470pF and 10nF.
2	I_{SENSE}	Current sense comparator input.
3	FF	PWM ramp.
4	CT	Timing capacitor C_T determines oscillator frequency.
5	V_{FB}	Feedback voltage input. Connected to the error amplifier inverting input.
6	COMP	Error amplifier output.
7	Gnd	Ground.
8	V_{CC}	Supply Voltage.

Block Diagram



Theory of Operation

Feed Forward Voltage Mode Control

In conventional voltage mode control, the ramp signal is fixed and often generated by the oscillator. The output voltage is the only feedback path for regulation against load and line variations. Feed forward voltage mode uses the ramp signal driven by the input line, as shown in Figure1. Therefore, the ramp signal responds immediately to line change. At the start of each switch cycle, the FF pin capacitor is charged up through a resistor connected to the input line. Meanwhile, the Gate output is turned on to drive an external power switching device. When the FF pin voltage reaches the error amplifier output V_{COMP}, the PWM comparator turns off the Gate and the FF pin capacitor is quickly discharged by an internal current source.

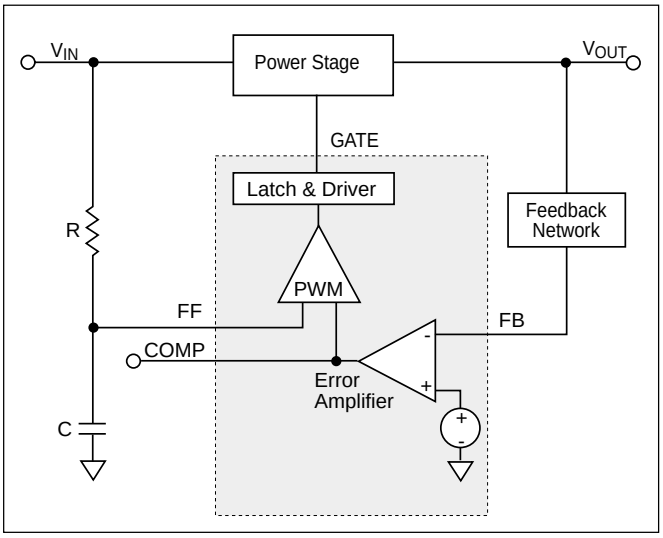


Figure 1: Feed Forward Voltage Mode Control..

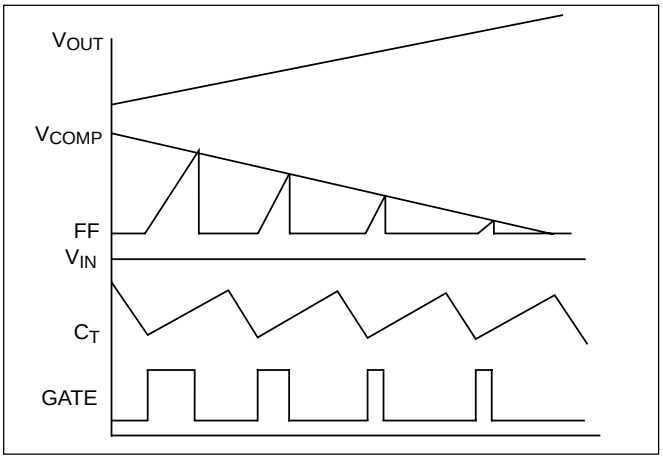


Figure 2: Pulse Width Modulated by Output Current with Constant Input Voltage.

Overall, the dynamics of the duty cycle are controlled by both input and output voltages. As shown in Figure 2, an elevated output voltage reduces V_{COMP} through the error amplifier. This in turn decreases the duty cycle and corrects the deviation of the output voltage. For line variation, the ramp signal responds immediately, which provides much improved line transient response. The delay associated with the power stage and feedback path has been totally avoided. As an example, shown in Figure 3, when the input line goes up, the slope of the ramp signal increases, reducing duty cycle to counteract the change.

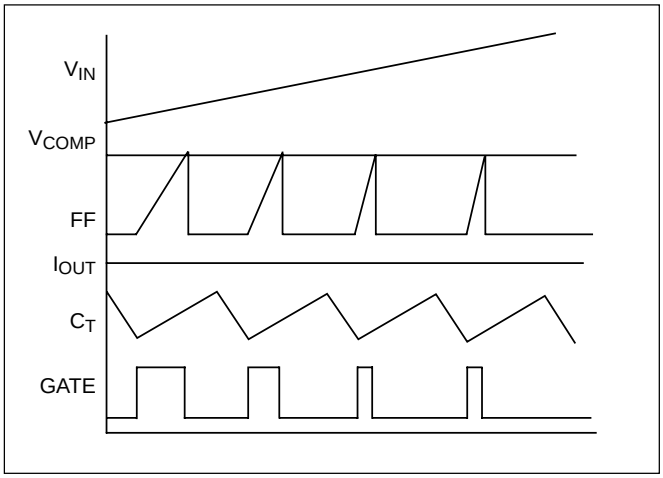


Figure 3: Pulse Width Modulated by Input Voltage with constant Output Current.

The feed forward feature can also be employed to implement volt-second clamping, which limits the maximum product of input voltage and turn on time. This clamp is used in circuits, such as Forward and Flyback converters, to prevent the transformer from saturating. The calculation for volt-second clamping is presented in the Design Guidelines section.

Powering the IC & UVL

The internal logic monitors the supply voltage to ensure the controller has enough operating headroom. The V_{REF} block provides power to the controller's logic. The $V_{REF(OK)}$ comparator monitors the internal 3.3V V_{REF} line and flags a fault if V_{REF} falls below 3.1V.

The Undervoltage Lockout (UVL) comparator has two voltage references; the start and stop thresholds. During power-up, the UVL comparator disables V_{REF} (which in-turn disables the entire IC) until the controller reaches its V_{CC} start threshold. During power-down, the UVL comparator allows the controller to operate until the V_{CC} stop threshold is reached. The CS51227 requires only 50µA during startup. During low V_{CC} and abnormal operation conditions, the output stage is held at a low level, low impedance state.

Current Sense and Over Current Protection

The I_{SENSE} pin monitors the switch current for pulse by pulse current limit. When the I_{SENSE} pin voltage exceeds the internal threshold (0.3V typical), the current limit comparator immediately turns off the Gate signal. The Gate will then stay off for the remainder of the cycle. Various

techniques, such as using current sensing resistor or current transformer, are widely adopted to generate the current signal.

The current sense signal is prone to leading edge spikes caused by switching transitions. A RC low-pass filter can effectively reduce the spikes and avoid premature triggering. However, the low pass filter will inevitably change the shape of the current pulse and also add cost. The CS51227 has built-in leading edge blanking circuitry that blocks out the first 150ns (typ) of each current pulse. This feature removes the leading edge spikes without altering the current waveform. Blanking is disabled when the COMP pin voltage exceeds 3.0V (typ). This feature reduces the minimum duty cycle during an output short or overload condition.

Design Guidelines

Programming Oscillator Frequency

The switching frequency is set by the capacitor connected to the CT pin. The CT pin voltage oscillates between 1V and 2V. The ratio of the charge and discharge currents sets the maximum duty cycle to be 90%. Use the following equation to select C_T,

$$C_T = \frac{9.027 \times 10^7}{f_S}$$

where f_S = switching frequency

C_T = capacitance in pF

When C_T is less than 100pF, parasitic capacitance associated with the CT pin starts to impact frequency accuracy. Figure 4 shows typical oscillator frequency vs. C_T value.

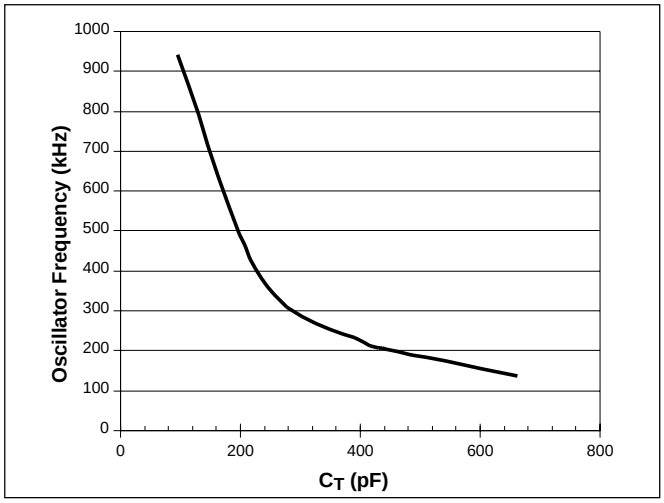


Figure 4: Typical Performance Characteristics: Oscillator frequency vs. CT.

Component Selection for Feed Forward Ramp

FF discharge voltage and FF maximum voltage limit the maximum voltage rise on the FF pin to 1.5V typical. This provides the volt-second clamp feature when the FF pin is driven by the input line. If the line voltage is much greater than the FF pin voltage, the charge current is approximately equal to V_{IN}/R where R is the resistor connecting the FF pin and input line. The voltage second clamp then has the form of:

$$V_{IN} \times T_{ON} = 1.5 \times R \times C_{FF}$$

One can select RC_{FF} to prevent magnetic devices from saturating.

In a buck or forward converter, the error amplifier output V_{COMP} is equal to:

$$V_{COMP} = \frac{V_{OUT} \times T_S}{N \times R \times C_{FF}} + 0.3V$$

where:

N = transformer turns ratio (use 1 for buck converter)

Ts = switching period

This equation shows that the error amplifier output is independent of the input voltage. Therefore, the system does not rely on the error amplifier to respond to line variations. This excludes the delay associated with the error amplifier. The line regulation is also greatly improved because both error amplifier and ramp signal can contribute to DC regulation.

Select Feedback Voltage Divider

As shown in Figure 5, the voltage divider output feeds the FB pin which connects to the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to a 1.263V reference voltage. The FB pin has an input current which has to be taken into account for accurate output voltage programming. The following equation can be used to calculate the R1 and R2 value:

$$\frac{R2}{R1 + R2} \times V_{OUT} = 1.263 - \nabla$$

where ∇ is the correction factor.

$$\nabla = (Ri + R1 // R2) \times Ier$$

Ri = DC resistance between the FB pin and the voltage divider output, as shown in Figure 5.

Ier = FB pin input current, 1.3µA typical.

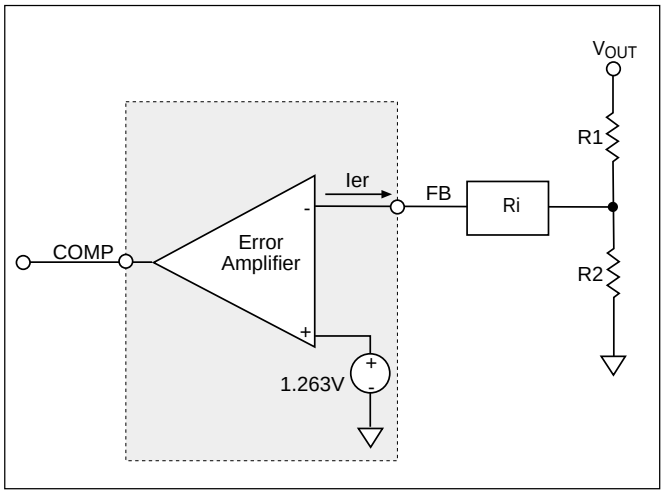


Figure 5: The feedback voltage divider design has to consider the error amplifier input current.

Thermal Management

The CS51227 will enter thermal shutdown when the junction (die surface) temperature exceeds 150°C, typical. 10°C typical thermal hysteresis will prevent part cycling, or a "chattering" startup near the shutdown temperature. Junction temperature is a function of the ambient temperature, thermal resistance of the die and package, and the power dissipated by the package and leads.

Package Specification

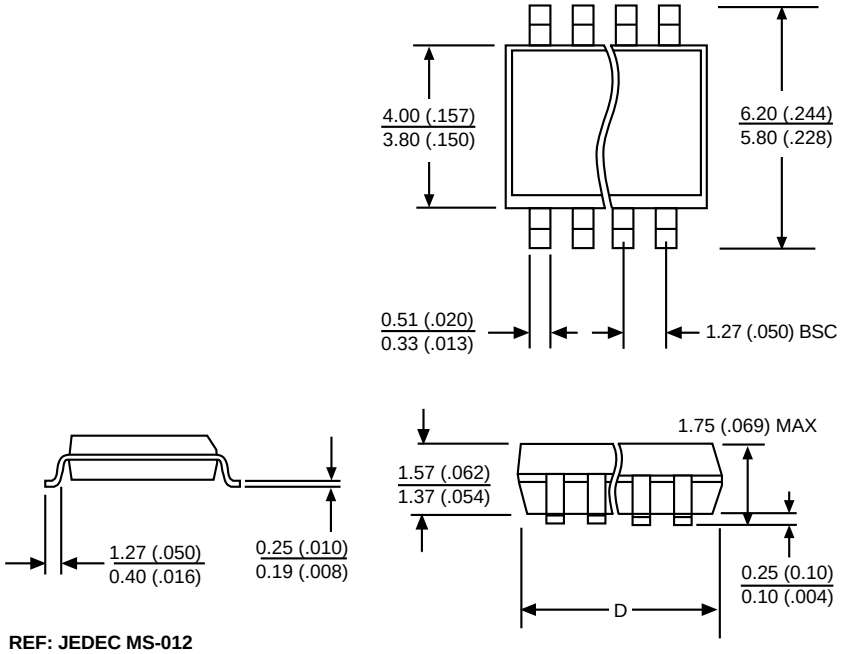
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8 Lead SO Narrow	5.00	4.80	.197	.189

PACKAGE THERMAL DATA

Thermal Data		8L SO Narrow	
$R_{\Theta JC}$	typ	45	°C / W
$R_{\Theta JA}$	typ	165	°C / W

Surface Mount Narrow Body (D); 150 mil wide



REF: JEDEC MS-012

Ordering Information

Part Number	Description
CS51227ED8	8 Lead SO Narrow
CS51227EDR8	8 Lead SO Narrow *(tape & reel)*