AUTOMOTIVE GRADE

CS4124

High Side PWM FET Controller

Description

The CS4124 is a monolithic integrated circuit designed primarily to control the rotor speed of permanent magnet, direct current (DC) brush motors. It drives the gate of an N channel power MOSFET or IGBT with a user-adjustable, fixed frequency, variable duty cycle, pulse width modulated (PWM) signal. The CS4124 can also be used to control other loads such as incandescent bulbs and solenoids. Inductive current from the motor or solenoid is recirculated through an external diode.

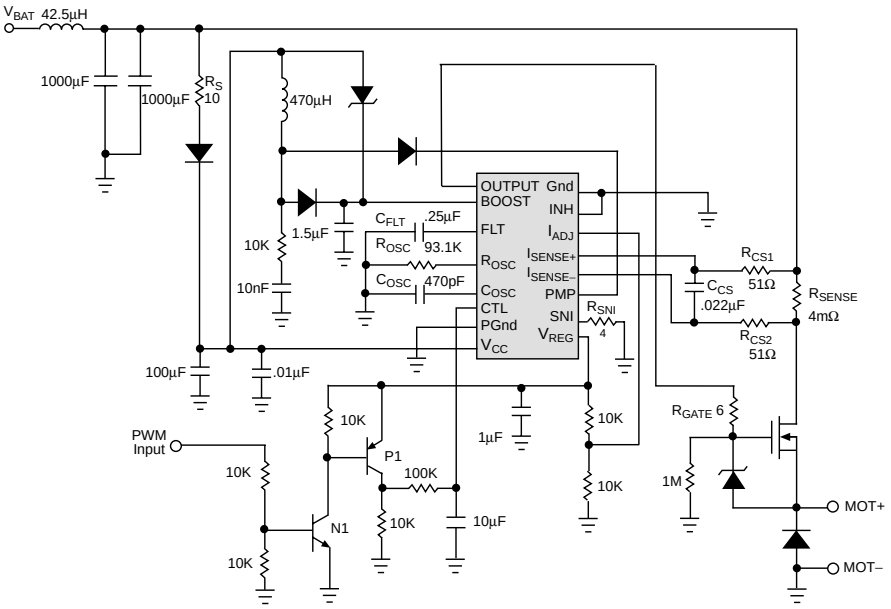
The CS4124 accepts a DC level input signal of 0 to 5V to control the pulse width of the output signal. This signal can be generated by a potentiometer referenced to the on-chip 5V linear regulator, or a filtered 0% to 100% PWM signal also referenced to the 5V regulator.

The IC is placed in a sleep state by pulling the CTL lead below 0.5V. In this mode everything on the chip is shutdown except for the on-chip regulator and the overall current draw is less than 275µA. There are a number of on-chip diagnostics that look for potential failure modes and can disable the external power MOSFET.

Features

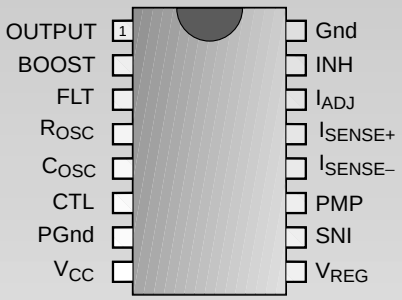
- 150mA Peak PWM Gate Drive Output
- Patented Voltage Compensation Circuit
- 100% Duty Cycle Capability
- 5V, ± 3% Linear Regulator
- Low Current Sleep Mode
- Overvoltage Protection
- Boost Mode Power Supply
- Output Inhibit

Applications Diagram



Package Option

16 Lead PDIP



Consult Factory for 16 Lead SOIC Wide package.

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N. American Technical Support: 800-282-9855
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Absolute Maximum Ratings

Storage Temperature ..... –65°C to 150°C
V_{CC} ..... –0.3V to 30V
V_{CC} Peak Transient Voltage (load dump = 26V w / series 10Ω resistor) 40V
Input Voltage Range (at any input) ..... –0.3V to 10V
Maximum Junction Temperature ..... 150°C
Lead Temperature Soldering
Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak
ESD Capability (Human Body Model) 2kV

Electrical Characteristics: $4V \le V_{CC} \le 26V$; $-40°C < T_A < 125°C$; unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ V_{CC} Supply					
Operating Current Supply	$7V \le V_{CC} \le 18V$		5	10	mA
	$4V \le V_{CC} < 7V$, $18V < V_{CC} \le 26V$			15	mA
Quiescent Current	V_{CC} = 12V		170	275	µA
Overvoltage Shutdown		26.5		29	V
■ Control (CTL)					
Control Input Current	CTL = 0V to 5V	–2	0.1	2	µA
Sleep Mode Threshold		8%	10%	12%	V_{REG}
Sleep Mode Hysteresis	$7V \le V_{CC} \le 26V$	50	100	150	mV
	$4V \le V_{CC} < 7V$	10		150	mV
■ Current Sense					
Differential Voltage Sense	$7V \le V_{CC} \le 18V$				
	I_{ADJ} = 1V and R_{CS1} = 51Ω	18		34	mV
	I_{ADJ} = 4V and R_{CS1} = 51Ω	104		125	mV
	$4V \le V_{CC} < 7V$				
	I_{ADJ} =1V and R_{CS1} = 51Ω	15		39	mV
	$18V < V_{CC} \le 26V$				
	I_{ADJ} = 1V and R_{CS1} = 51Ω	15		39	mV
	I_{ADJ} = 4V and R_{CS1} = 51Ω	102		130	mV
I_{ADJ} Input Current	$4V \le V_{CC} \le 26V$ I_{ADJ} = 0V to 5V	–2	0.3	2	µA
■ Linear Regulator					
Output Voltage, V_{REG}	V_{CC} = 4V	2.0			V
	V_{CC} = 13.2V	4.85		5.15	V
	V_{CC} = 26V	4.85		5.20	V
■ Inhibit					
Inhibit Threshold		40%	50%	60%	V_{REG}
Inhibit Hysteresis	$4V \le V_{CC} \le 7V$	100		500	mV
	$7V \le V_{CC} \le 26V$	150	325	500	mV
■ External Drive (OUTPUT)					
Output Frequency	$4V \le V_{CC} < 7V$				
	R_{OSC} = 93.1kΩ, C_{OSC} = 470pF	10		25	kHz
	$7V \le V_{CC} \le 18V$,				
	R_{OSC} = 93.1kΩ, C_{OSC} = 470pF	17	20	23	kHz
	$18V < V_{CC} \le 26V$				
	R_{OSC} = 93.1kΩ, C_{OSC} = 470pF	17	20	25	kHz

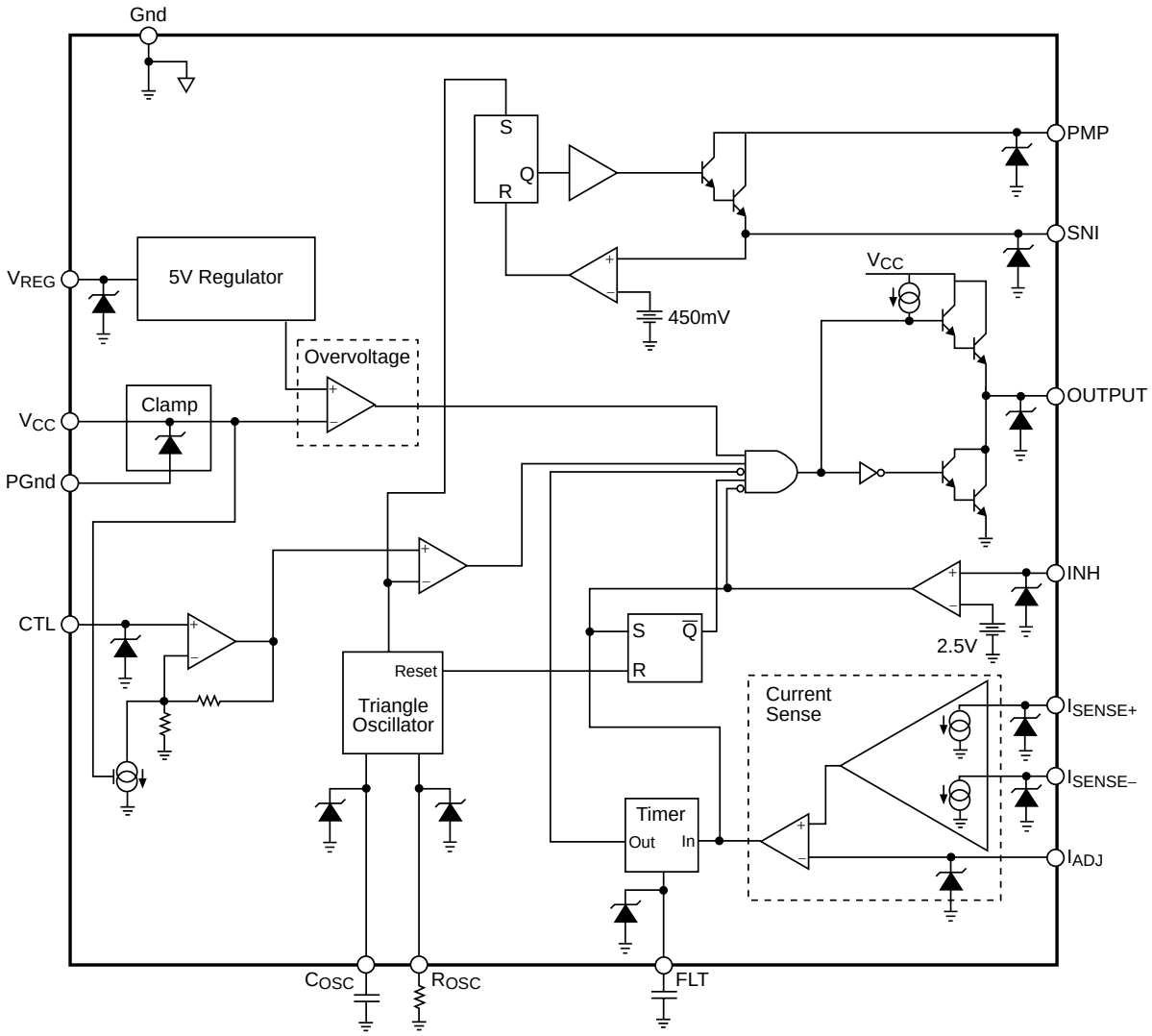
Electrical Characteristics: $4V \le V_{CC} \le 26V$; $-40°C < T_A < 125°C$; unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ External Drive (OUTPUT): continued					
Voltage to Duty Cycle Conversion	$4V \le V_{CC} < 7V$				
	V_{CC} = 13V, CTL = 1V	65		75	%
	V_{CC} = 13V, CTL = 2V	100			%
	$7V \le V_{CC} \le 18V$				
	V_{CC} = 13V, CTL = 30% V_{REG}	28.3		36.3	%
	V_{CC} = 13V, CTL = 55.8% V_{REG}	56.0		64.0	%
	$18V < V_{CC} \le 26V$				
	V_{CC} = 13V, CTL = 1. 5V	11.8		21.8	%
	V_{CC} = 13V, CTL = 3. 5V	34.2		44.2	%
Output Rise Time	$4V \le V_{CC} \le 26V$, $R_{GATE} = 6\Omega$, C_{GATE} = 5nF		.25	1	µs
Output Fall Time	$4V \le V_{CC} \le 26V$, $R_{GATE} = 6\Omega$, C_{GATE} = 5nF		.30	1	µs
Output Sink Current	$4V \le V_{CC} < 7V$, $R_{GATE} = 6\Omega$, C_{GATE} = 5nF		150		mA
	$7V \le V_{CC} \le 26V$, $R_{GATE} = 6\Omega$, C_{GATE} = 5nF		300		mA
Output Source Current	$4V \le V_{CC} < 7V$, $R_{GATE} = 6\Omega$, C_{GATE} = 5nF		150		mA
	$7V \le V_{CC} \le 26V$, $R_{GATE} = 6\Omega$, C_{GATE} = 5nF		300		mA
Output High Voltage	I_{OUT} = 1mA	$V_{BOOST} - 1.7$			V
Output Low Voltage	I_{OUT} = -1mA			1.3	V
■ Charge Pump (DRV)					
Boost Voltage		$V_{CC} + 6.4$			V

Package Lead Description

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
16 Lead PDIP		
1	OUTPUT	MOSFET gate drive.
2	BOOST	Boost voltage.
3	FLT	Fault time out capacitor.
4	R_{OSC}	Oscillator resistor.
5	C_{OSC}	Oscillator capacitor.
6	CTL	Pulse width control input.
7	PGnd	Power ground for on chip clamp.
8	V_{CC}	Positive power supply input.
9	V_{REG}	5V linear regulator.
10	SNI	Sense inductor current.
11	PMP	Collector of boost power transistor.
12	I_{SENSE-}	Current sense minus.
13	I_{SENSE+}	Current sense plus.
14	I_{ADJ}	Current limit adjust.
15	INH	Output Inhibit.
16	Gnd	Ground.

Block Diagram



Application Information

Theory Of Operation

Oscillator

The IC sets up a constant frequency triangle wave at the C_{OSC} lead whose frequency is related to the external components R_{OSC} and C_{OSC}, by the following equation:

$$\text{Frequency} = \frac{0.83}{R_{OSC} \times C_{OSC}}$$

The peak and valley of the triangle wave are proportional to V_{CC} by the following:

$$V_{VALLEY} = 0.1 \times V_{CC}$$

$$V_{PEAK} = 0.7 \times V_{CC}$$

This is required to make the voltage compensation function properly. In order to keep the frequency of the oscillator constant the current that charges C_{OSC} must also vary with supply. R_{OSC} sets up the current which charges C_{OSC}. The voltage across R_{OSC} is 50% of V_{CC} and therefore:

$$I_{ROSC} = 0.5 \times \frac{V_{CC}}{R_{OSC}}$$

I_{ROSC} is multiplied by (2) internally and transferred to the C_{OSC} lead. Therefore:

$$I_{COSC} = \pm \frac{V_{CC}}{R_{OSC}}$$

The period of the oscillator is:

$$T = 2C_{OSC} \times \frac{V_{PEAK} - V_{VALLEY}}{I_{COSC}}$$

The R_{OSC} and C_{OSC} components can be varied to create frequencies over the range of 15Hz to 25kHz. With the sug-

gested values of 93.1kΩ and 470pF for R_{OSC} and C_{OSC} , the nominal frequency will be approximately 20 kHz. I_{ROSC}, at V_{CC} = 14V, will be 66.7 µA. I_{ROSC} should not change over a more than 2:1 ratio and therefore C_{OSC} should be changed to adjust the oscillator frequency.

Voltage Duty Cycle Conversion

The IC translates an input voltage at the CTL lead into a duty cycle at the OUTPUT lead. The transfer function incorporates ON Semiconductor's patented Voltage Compensation method to keep the average voltage and current across the load constant regardless of fluctuations in the supply voltage. The duty cycle is varied based upon the input voltage and supply voltage by the following equation:

$$\text{Duty Cycle} = 100\% \times \frac{2.8 \times V_{CTL}}{V_{CC}}$$

An internal DC voltage equal to:

$$V_{DC} = (1.683 \times V_{CTL}) + V_{VALLEY}$$

is compared to the oscillator voltage to produce the compensated duty cycle. The transfer is set up so that when V_{CC} = 14V the duty cycle will equal V_{CTL} divided by V_{REG}. For example at V_{CC} = 14V, V_{REG} = 5V and V_{CTL} = 2.5V, the duty cycle would be 50% at the output. This would place a 7V average voltage across the load. If V_{CC} then drops to 10V, the IC would change the duty cycle to 70% and hence keep the average load voltage at 7V.

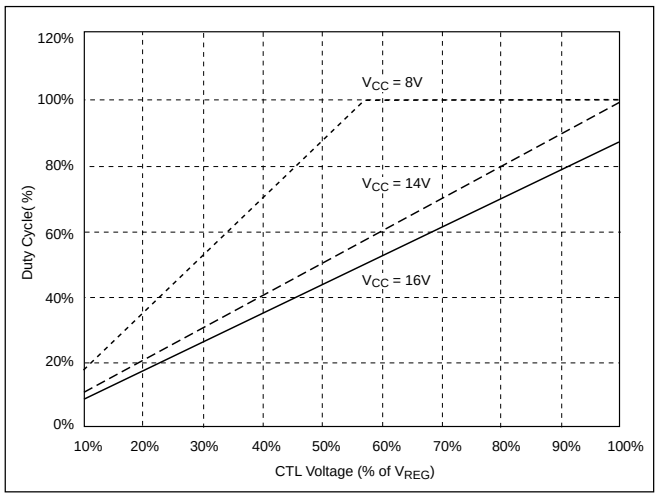


Figure 1: Voltage Compensation

5V Linear Regulator

There is a 5V, 5mA linear regulator available at the V_{REG} lead for external use. This voltage acts as a reference for many internal and external functions. It has a drop out of approximately 1.5V at room temperature.

Current Sense and Timer

The IC differentially monitors the load current on a cycle by cycle basis at the I_{SENSE+} and I_{SENSE-} leads. The differential voltage across these two leads is amplified internally and compared to the voltage at the I_{ADJ} lead. The gain, A_V is set internally and externally by the following equation:

$$A_V = \frac{V_{I(ADJ)}}{I_{SENSE+} - I_{SENSE-}} = \frac{37000}{1000 + R_{CS}}$$

The current limit (I_{LIM}) is set by the external current sense resistor (R_{SENSE}) placed across the I_{SENSE+} and I_{SENSE-} terminals and the voltage at the I_{ADJ} lead.

$$I_{LIM} = \frac{1000 + R_{CS}}{37000} \times \frac{V_{I(ADJ)}}{R_{SENSE}}$$

The R_{CS} resistors and C_{CS} components form a differential low pass filter which filters out high frequency noise generated by the switching of the external MOSFET and the associated lead noise. R_{CS} also forms and error term in the gain of the I_{LIM} equation because the I_{SENSE+} and I_{SENSE-} leads are low impedance inputs thereby creating a good current sensing amplifier. Both leads source 50µA while the chip is in run mode. I_{ADJ} should be biased between 1V and 4V. When the current through the external MOSFET exceeds I_{LIM}, an internal latch is set and the output pulls the gate of the MOSFET low for the remainder of the oscillator cycle (fault mode). At the start of the next cycle, the latch is reset and the IC reverts back to run mode until another fault occurs. If a number of faults occur in a given period of time, the IC "times out" and disables the MOSFET for a long period of time to let it cool off. This is accomplished by charging the C_{FLT} capacitor each time an over current condition occurs. If a cycle goes by with no overcurrent fault occurring, an even smaller amount of charge will be removed from C_{FLT}. If enough faults occur together, eventually C_{FLT} will charge up to 2.4V and the fault latch will be set. The fault latch will not be reset until C_{FLT} discharges to 0.6V. This action will continue indefinitely if the fault persists.

The off time and on time are set by the following:

$$\text{Off Time} = C_{FLT} \times \frac{2.4V - 0.6V}{4.5\mu A}$$

$$\text{On Time} = C_{FLT} \times \frac{2.4V - 0.6V}{I_{AVG}}$$

where:

$$I_{AVG} = (295.5\mu A \times DC) - [4.5\mu A \times (1 - DC)]$$

$$I_{AVG} = (300\mu A \times DC) - 4.5\mu A$$

DC = PWM Duty Cycle

Boost Switch Mode Power Supply

The CS4124 has an integrated boost mode power supply which charges the gate of the external high-side MOSFET to greater than 5V above V_{CC}. Three leads are used for voltage boost. They are Boost, PMP and SNI. The PMP lead is the collector of a darlington tied NPN power tran-

Application Information: continued

sistor. This device charges the inductor during its on time. The boost lead is the input to chip from the external reservoir capacitor. The SNI lead is the emitter of the power NPN and is connected externally to the R_{SNI} resistor.

The power supply is controlled by the oscillator. At the start of a cycle an R-S flip flop is set the internal power NPN transistor is turned on and energy begins to build up in the inductor. The R_{SNI} resistor sets the peak current of the inductor by tripping a comparator when the voltage across the resistor is 450mV. The flip flop is reset and the inductor delivers its stored energy to the load. The ripple voltage (V_{RIPPLE}) at the Boost lead is controlled by C_{BOOST}. A snubber circuit, made up of a series resistor and capacitor, is required to dampen the ringing of the inductor. A value of 4Ω is recommended for R_{SNI}.

A zener diode is needed between the boost output voltage and the battery. This will clamp the boost lead to a specified value above the battery to prevent damage to the IC. A 9 volt zener diode is recommended.

Sleep State

This device will enter into a low current mode (< 275µA) when CTL lead is brought to less than 0.5V. All functions are disabled in this mode, except for the regulator.

Inhibit

When the inhibit is greater than 2.5V the internal latch is set and the external MOSFET will be turned off for the remainder of the oscillator cycle. The latch is then reset at the start of the next cycle.

Overvoltage Shutdown

The IC will disable the output during an overvoltage event. This is a real time fault event and does not set the internal latch and therefore is independent of the oscillator timing (i.e. asynchronous). There is 325mV (typical) of hysteresis on the overvoltage function. There is no undervoltage lockout. The device will shutdown gracefully once it runs out of headroom.

Reverse Battery

The CS4124 will not survive a reverse battery condition. A series diode is required between the battery and the V_{CC} lead for reverse battery.

Load Dump

A 10Ω resistor, (R_S) is placed in series with V_{CC} to limit the current into the IC during 40V peak transient conditions.

Package Specification

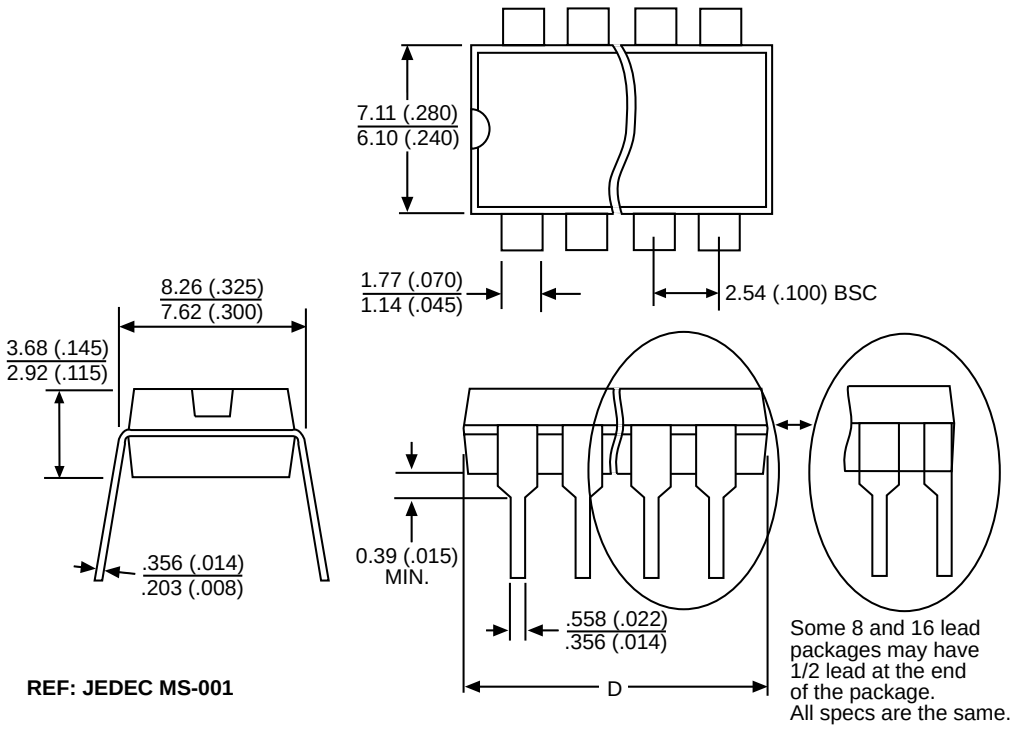
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L PDIP	19.69	18.67	.775	.735

PACKAGE THERMAL DATA

Thermal Data		16 Lead PDIP	
$R_{\Theta JC}$	typ	42	°C / W
$R_{\Theta JA}$	typ	80	°C / W

Plastic DIP (N); 300 mil wide



REF: JEDEC MS-001

Ordering Information

Part Number	Description
CS4124YN16	16L PDIP

Notes