CS212

Security Detector
Serial-Addressable Receiver/Transmitter

Description

The S-ART is a 16 pin circuit designed for data transmission on a two-lead cable. The circuit is specially developed for alarm systems where it is desired to identify each detector individually. There can be up to 30 S-ART circuits / detectors on the same 2-lead cable. This cable transmits both DC supply to the S-ART and information to / from the S-ART.

The S-ART works on the principle by which an address is sent on the line cable and the S-ART which recognizes the address then carries out the order which can, in principle, be two things:

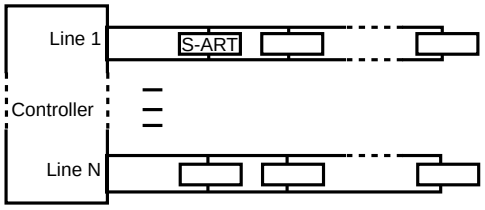
1. Transmit data from the line cable to the S-ART's two outputs OUT0 and OUT1.
2. Answer the S-ART controller with the condition of the 2 inputs IN0 and IN1 or IN2-3.

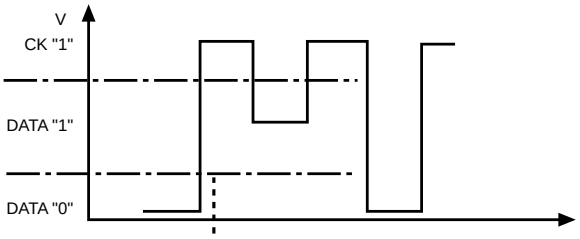
The line signal is divided into 3 levels in order to give a time signal for synchronizing and a data signal containing addresses, orders etc.

Typical signal levels for the three levels would be 15V, 7.5V and 0V.

Block Diagram

A method by which, in principle, the system can be extended to an infinite number of S-ART is shown on the block diagram. The controller scans the in / outputs of a number of lines, each with a maximum of 30 S-ARTs.



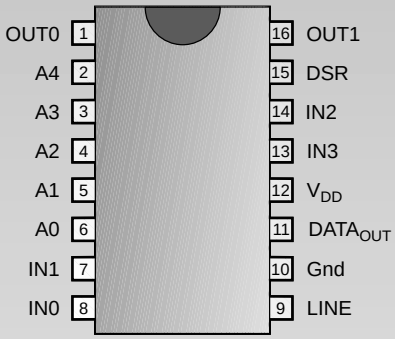


Features

- **Receives/Transmits Data on Only Two Leads**
- **Low Current Consumption**
- **High Noise Immunity**
- **Sabotage Surveilled Loop Input**

Package Options

16L PDIP & 16L SO Wide



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Absolute Maximum Ratings

Lead Temperature Soldering:
- Wave Solder (through hole styles only) . . . . . .10 Sec. max 260°C Peak
- Reflow (SMD styles only) . . . . . .60 Sec max. above 183°C, 230°C Peak

Storage Temperature Range, T_S . . . . . .-65 to 150°C

Maximum Operating Junction Temperature, T_J . . . . . .125°C

Electrical Characteristics: T_A = 25°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Temperature Range, T_A		-40		85	°C
Device Current I_{DD} Not Addressed	Outputs unloaded Line Voltage=0-15V, V_{DD}=15V		0.47	0.80	mA
Device Current I_{DD} Power-Up-Mode (5 corr. addr. bits)C_P4-C_P5	IN0, IN1 are Open IN2, IN3 are Active V_{DD}=15V		3.55	5.50	mA
Device Current I_{DD} Addressed, Line Output Transistor Active	IN2, IN3 not Active IN0, IN1 are Open V_{DD}=15V		6.24	9.64	mA
Device Current I_{DD} Addressed (4 corr.addr.bits) Line Output Transistor Not Active	IN2, IN3 not Active IN0, IN1 are Open V_{DD}=15V		1.84	2.86	mA
Output Voltage Low Level Out0, Out1, DSR	V_{DD}=10-15V I_{SINK}=1mA			1.2	V
Output sink Current Out0, Out1, DSR		1.0			mA
Output Voltage High Level Out0, Out1, DSR				14	V
Leakage Current Out0, Out1, DSR	V_{OUT}=14V			30	µA
Input Voltage Level A0-A4, IN0, IN1 Low A0-A4, IN0, IN1 High	 V_{DD}=10-15V V_{DD}=10-15V	 70%V_{DD}		30%V_{DD}	 V V
Input Current IN0, IN1=Gnd Power-Up Mode (4 corr.addr.bits)	V_{DD}=18V	150		850	µA
Input Current A0-A4, IN0, IN1 Not Addressed	V_{DD}=18V			20	µA
Positive Trigger Threshold V_P, C Voltage V_{dd}=15V V_P, D	 Clock Comparator Data Comparator	 11.0 4.6	 11.7 5.7	 12.4 6.6	 V V
Negative Trigger V_{NC} Threshold Voltage V_{NC}	V_{DD}=15V Clock Comparator V_{DD}=15V, Data Comparator	10.2 3.4	10.9 4.3	11.6 5.2	V V
Hysteresis Voltage Clock / Data Comp.	V_{DD}=15V	0.7	0.8		V
Saturation Voltage For Line Output Driver	V_{DD}=15V, I_C=50mA			1	V
Saturation Voltage For Line Output Driver	V_{DD}=15V, I_C=10mA			0.4	V
Leakage Current For the Line Output	V_{LINE}=0-18V, V_{DD}=18V			±16	µA
Line Signal Freq.	V_{DD}=15V±1V	0		20	kHz
Rise / Fall-Time Line Signal		0.25		250.00	µs

Electrical Characteristics: T_A = 25°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Turn-On Time For Line Output Driver			1.0		µs
Turn-Off Time For Line Output Driver			1.0		µs
Line Voltage VL (Note 1)		0		28	V
Loop Current IN2, IN3		0.1		0.5	mA
Alarm Condition IN2-IN3 Loop Open		1		5	kΩ
Alarm Condition IN2-IN3 Loop Shorted		5		30	kΩ

Note 1: The circuit shall function in the correct way only between 0 and 18V_{DC}. Data driver must not turn on when line voltage is above 18V.

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	OUT0	Output (open collector) from S-ART.
2	A4	Address input. Must be connected to V_{DD} or Gnd according to the relevant address code.
3	A3	Address input. Must be connected to V_{DD} or Gnd according to the relevant address code.
4	A2	Address input. Must be connected to V_{DD} or Gnd according to the relevant address code.
5	A1	Address input. Must be connected to V_{DD} or Gnd according to the relevant address code.
6	A0	Address input. Must be connected to V_{DD} or Gnd according to the relevant address code.
7	IN1	Input to S-ART.
8	IN0	Input to S-ART.
9	LINE	Signal lead in the line cable.
10	Gnd	Zero lead in the line cable.
11	$DATA_{OUT}$	Output from the S-ART, which is active in the READ-mode. Transmits data from S-ART to line.
12	V_{DD}	Supply voltage to the S-ART. The voltage is derived from the line signal.
13	IN3	Sabotage surveilled loop (shorting and breaking).
14	IN2	Sabotage surveilled loop (shorting and breaking).
15	DSR	Data Set Ready. Output (open collector) from the S-ART which is active during WRITE-mode, when OUT0 and OUT1 change.
16	OUT1	Output (open collector) from S-ART.

Serial-Addressable Receiver Transmitter S-ART

ADDRESS CODING

The circuit is coded on address inputs A0-A4.

In order to reduce the power consumption to the circuits they are in power down mode for most of the time. Only when a circuit is addressed is the amount to that particular circuit increased.

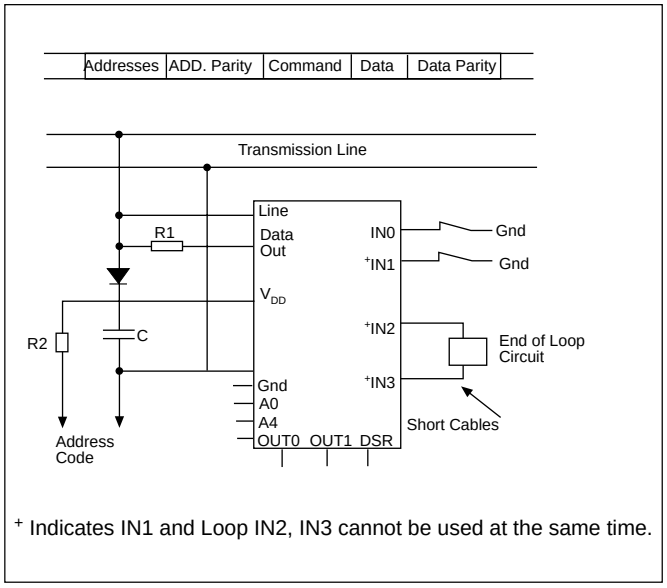
READ

When a S-ART has recognized an address with the correct parity and then received a READ-order the controller becomes passive. The S-ART in question will then send data bits to the controller. These bits are the condition on the IN0 and IN1 or IN2-3 and a parity bit derived from them.

The current in inputs IN0 and IN1 only flows when the S-ART is addressed.

If the sabotage surveilled loop IN2-3 is used IN1 should be open. IN2-3 is then read instead of IN1.

The loop IN2-3 is checked for both shorting and breaking.



+ Indicates IN1 and Loop IN2, IN3 cannot be used at the same time.

WRITE

When a S-ART has recognized an address with correct parity and a write order, the S-ART in question transmits data to the outputs OUT0 and OUT1. This data transmission takes place after a check of the parity bit. If the parity bit is wrong, data transmission to OUT0 and OUT1 is blocked and new data transmission can only take place after a read order which resets the parity fault.

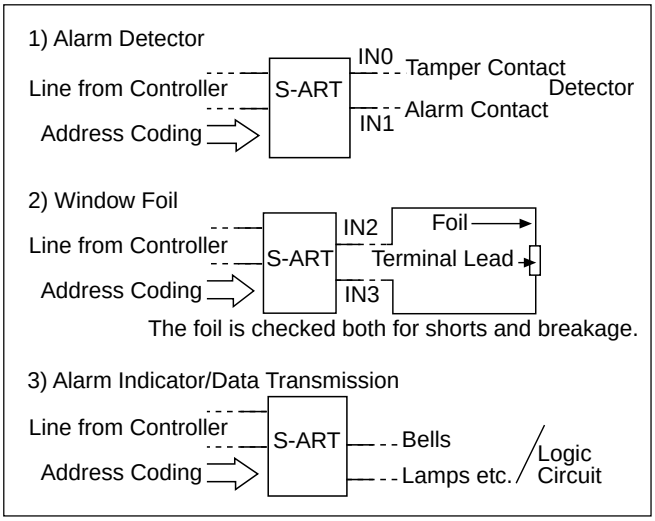
The DSR signal can be used to strobe OUT0 and OUT1 further on in the following logic.

DATA FORMAT

The signals are sent out on the line in words organized as shown in the figure.

The S-ART information consists of two parity bits: an address parity bit and a data parity bit. Both the address and data are checked for even parity. The address parity bit must always be generated by the controller. The data parity bit during the READ-mode is generated by the S-ART. During the WRITE-mode the data parity bit is generated by the controller.

Typical S-ART Applications



Functional Description

GENERAL

The CS212 is a peripheral addressable circuit which is used as a communication link between Detectors / Sensors and a Central Control Unit.

The communication between the CS212 and a control unit takes place via a simple 2-wire cable which also provides power to the IC.

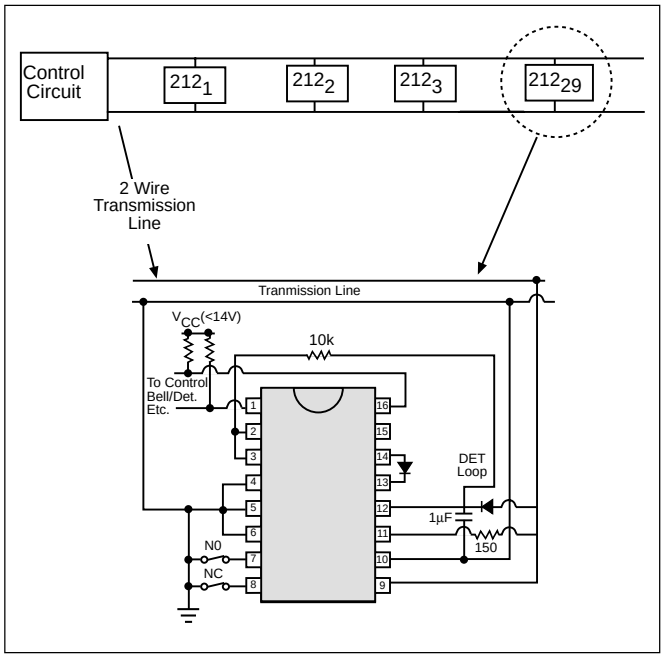
On each 2-wire cable, a maximum of 30 CS212's can be controlled or interrogated with the address binary 0-29. This permits surveillance of up to 30 window protections, door contacts, movement detectors, etc. within the same 2-wire group. Each CS212 can monitor the status of two external surveillance devices and communicate the status back to the control unit. Two outputs are also available for controlling bells, lights, LED's, door locks, etc. These outputs are controlled from the control unit via the 2-wire cable.

WIRE TRANSMISSION CABLE (The Line)

The 2-wire bidirectional transmission cable called "The Line" provides power and data to the CS212 and also provides data back to the control circuit.

The line signal is rectified and filtered at each CS212 and is used for the power supply to the chip. The CS212 also decodes the line signal into clock and data signals used inside the IC.

Functional Description

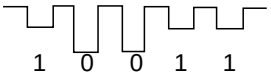


Notes:

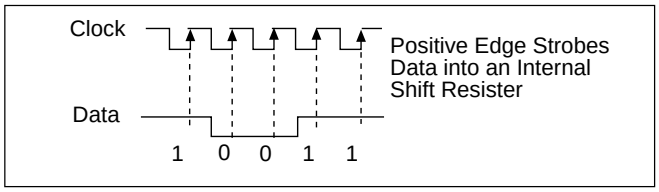
*1. * Indicates IN1 & loop IN2-3 cannot be used at the same time.*

2. This diagram shown CS212 circuit coded to #24.

A typical line signal from the control unit would look like the following:



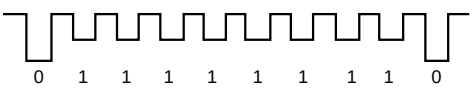
The CS212 would decode this into clock and data.



The CS212 accepts addresses and commands in 10-bit word formats. Three types of words must be generated: Sync, Read and Write.

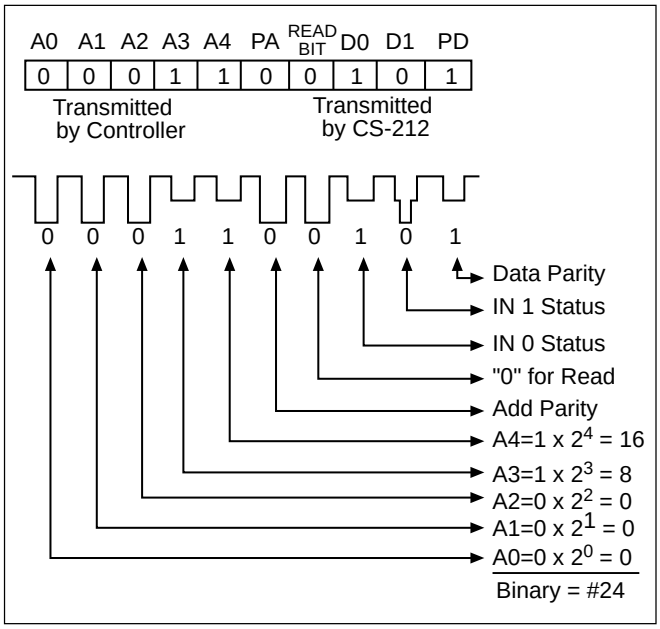
SYNC WORD

Synchronization is obtained by providing the CS212 with 8 or more 1's followed by a "0". To prevent a false sync, it is best to send 0 before the eight 1's. This word insures all circuits on the same line see the commands at the proper time.



READ WORD

To check the status of a CS212's inputs: i.e., IN0 and IN1 or IN2-3, a read word must be sent. The first 5 bits must correspond to the address of the CS212 to be interrogated. Bit #6 is the address parity bit. It must insure that the first 6 bits are an even number of "1" 's. If the parity is even and the CS212 to be interrogated has not previously received a parity error (odd parity), it will transmit its status, along with an internally generated parity bit. D0 corresponds to IN0, D1 corresponds to IN1 or IN2-3. After the address parity bit has been transmitted the controller must pull the line down to about 7.5V to allow the CS212 to transmit. If a "1" is to be transmitted, no change will occur on the line. If a "0" is to be transmitted, the CS212 will then pull the line down. In either case, the controller must pull the line back up to 15V in order to continue. If the CS212 has received a parity fault, it will transmit 3 one's ($D0=D1=P_D=1$). This will allow the controller to detect a parity error. If a parity error is detected by the controller, the read word must be repeated.



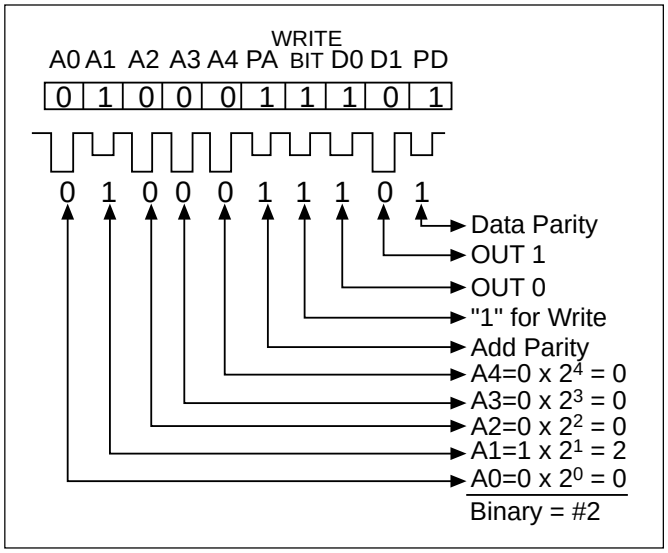
TYPICAL READ WORD

Assume that device #24 is to be interrogated and the status of IN0=1 and IN1=0.

WRITE WORD

In order to update OUT0 and OUT1, a write word must be sent to the CS212. The first 5 bits must correspond to the CS212 to be updated. Bit #6 is an address parity bit. It must insure even parity. D0 corresponds to OUT0 and D1 corresponds to OUT1. An even data parity bit must be received by the CS212. If the address and data parity are even and the CS212 has not previously received a parity error, it will update OUT0 and OUT1. If a parity error was received, the CS212 will not be updated. In this case, a read word must be sent to clear the parity fault.

Functional Description: continued



TYPICAL WRITE WORD:

Assume CS212 #2 is to be updated so that OUT0=1 and OUT1=0.

OUTPUTS

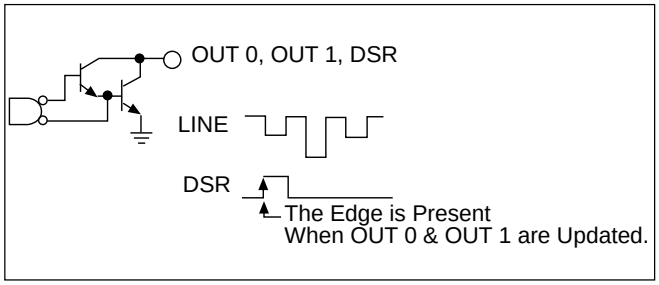
1. OUT0 and OUT1: Pin #'s 1, 16:

   These outputs are updated according to the information present during the write word.

2. DSR: Pin #15:

   The DSR pin is a monitor of the clock signal for the on-chip D flip flops, corresponding to OUT0 and OUT1. It can be used to strobe data from OUT0 and OUT1 into external circuitry connected to the CS212.

These three outputs can sink up to 1mA at 1.2V. They are Darlington type open collector outputs.



3. Data Out: Pin #11:

   The Data Out pin is used to transmit the status of IN0 and IN1 to the line. For Data=1, the line driver is off. For Data=0, the line driver is turned on. This output is a saturated switch capable of sinking 10mA DC at .4V and 50mA at 1V on a transient basis. The 50mA is needed to discharge the line capacitance. A 150Ω resistor from the line to Pin 11 limits the current into Pin 11 when the line driver is on.

INPUTS:

1. Address inputs: Pin#'s 2,3,4,5,6.

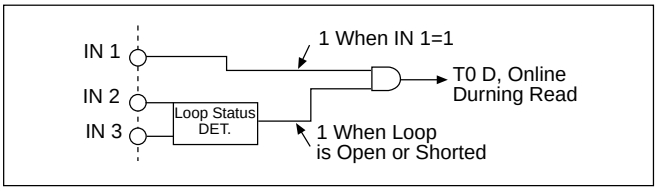
   The CS212 has 5 address inputs which decide what address code it will respond to. Their thresholds are approximately 1/2 V_{DD} and draw less than 20µA. The inputs should be grounded for Logic "0" and tied to V_{DD} (PIN 12) through a 10K resistor for Logic "1". The resistor is necessary for non-destruction of the IC with 28V applied to the line.

2. Data Inputs: Pin#'s 7,8.

   IN0 and IN1 (Pins 8 and 7) are digital inputs and are similar to the address inputs in that they have a threshold of approximately 1/2 V_{DD}. When the CS212 is unaddressed, these inputs draw less than 20µA. When the circuit powers up, IN0 and IN1 typically source 400µA.

3. Detector Loop: Pin #'s 13, 14.

   IN2 and IN3 can be used together to form a detector loop. When used, the outputs are connected together through a window foil and a diode. These inputs will generate a logic “1” at D1 on the line when the pins are shorted or opened.



   When using IN2 and IN3, IN1 must be terminated to V_{DD} through the 10K Resistor used for the address inputs. When using IN1, IN2 and IN3 must be shorted or opened.

4. Line Input: Pin #9

   The line input is internally connected to two comparators. These comparators separate the line signal into clock and data. The line input will draw less than 16µA of input current.

5. V_{DD}: Pin #12

   The V_{DD} Pin provides power to the CS212 circuitry. The line signal is externally rectified and filtered, then applied to V_{DD}. The V_{DD} pin draws varying amounts of current, depending upon the state of the CS212. (See specification). The unaddressed current is less than 0.8mA.

   The operating voltage range is 10V to 18V on Pin 12 of the IC. This wide range is necessary because of losses in the line and ripple on V_{DD}.

   The circuit is designed to withstand 28V applied to the line. This is to prevent the destruction of the IC and its external components if the 2-wire cable is miswired.

Package Specification

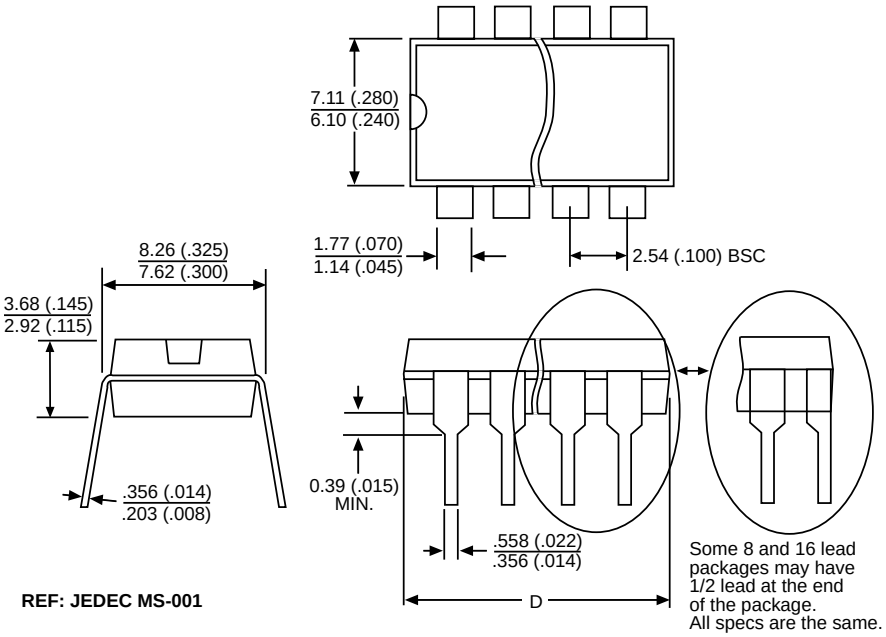
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L PDIP	19.69	18.67	.775	.735
16L SO Wide	10.50	10.10	.413	.398

PACKAGE THERMAL DATA

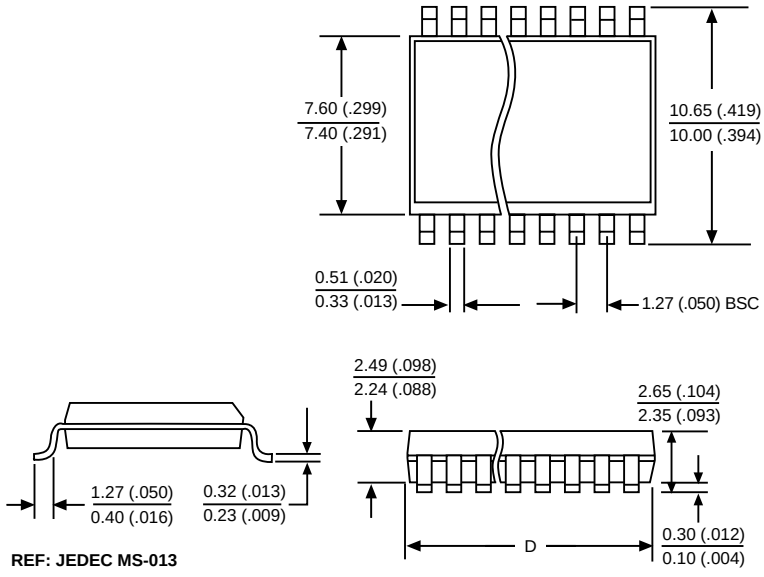
Thermal Data		16L PDIP	16L SO Wide	
$R_{\Theta JC}$	typ	42	23	°C / W
$R_{\Theta JA}$	typ	80	105	°C / W

Plastic DIP (N); 300 mil wide



REF: JEDEC MS-001

Surface Mount Wide Body (DW); 300 mil wide



REF: JEDEC MS-013

Ordering Information

Part Number	Description
CS212EN16	16L PDIP
CS212EDW16	16L SO Wide
CS212EDWR16	16L SO Wide Tape & Reel

Notes