AUTOMOTIVE GRADE

CS2001

1.2A Switching Regulator, and 5V, 100mA Linear Regulator with $\overline{\text{RESET}}$

Description

The CS2001 is a smart power supply ASIC utilized in automotive airbag systems. It contains a current-mode switching regulator with a 1.2A on-chip switch and a 5V, 100mA linear regulator. The linear output capacitor must be 3.3µF or greater with an ESR in the range of 100mΩ to 1Ω. If the ESR of the cap is less than 100mΩ, a series resistor must be used. The switcher can be configured in either a boost or flyback topology. The boost topology (shown below) produces energy reserve voltage VER which is externally adjustable (25V maximum) through the resistor divider connected to the V_{FB} pin. In the event of fault conditions that produce V_{FB} either open or shorted, the switcher is shut down.

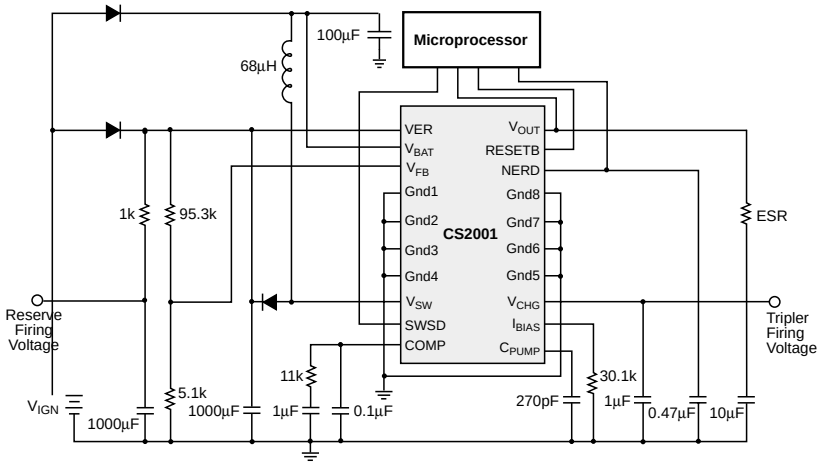
Under normal operating conditions (V_{BAT} > 8V), the current loading on the linear regulator is directed through V_{BAT}. A low battery or loss of battery condition switches the supply for the linear regulator from V_{BAT} to VER and shuts down the switcher using the ASIC's internal "smartswitch". This switchover feature minimizes the power dissipation in both the linear and switcher output devices and saves the cost of using a larger inductor.

The NERD (No Energy Reserve Detected) pin is a dual function output. If V_{OUT} is not in regulation, it provides a Power On Reset function whose time interval is externally adjustable with the capacitor. This interval can be seen on the RESETB pin, which allows for clean power-up and power-down of the microprocessor. Once V_{OUT} is in regulation, the logic level of the NERD output (usually low) indicates to the microprocessor whether or not the VER pin is connected.

A switched-capacitor voltage tripler accepts input voltage VER and produces output voltage V_{CHG} (typically VER +8V). This voltage is used in the system to drive high-side FETS.

This part is capable of withstanding a 50V peak transient voltage. The linear regulator will not shut down during this event.

Application Diagram

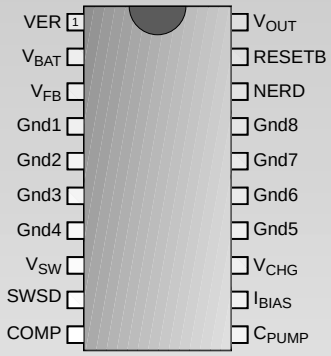


Features

- **Linear Regulator**
  5V ±2% @ 100mA
- **Switching Regulator**
  1.2A Peak Internal Switch
- **Voltage Tripler**
- **Smart Functions**
  Smartswitch
  RESET
  Energy Reserve Status
- **Protection**
  Overtemperature
  Current Limit
  50V Peak Transient Capability

Package Options

20 Lead SO Wide
(internally fused leads)



ON Semiconductor

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Absolute Maximum Ratings

V_{BAT} .....–0.5V to 25V
VER .....–0.5V to 25V
V_{OUT} .....–0.5V to 7V
Digital Input / Output Voltage .....–0.5V to 7V
Peak Transient Voltage (36V Load Dump @ 14V battery voltage) 50V
Storage Temperature Range .....–55° to 150°C
Junction to Free Air Thermal Impedance .....55°C / W
ESD Susceptibility (Human Body Model) 4kV
Lead Temperature Soldering: Reflow (SMD styles only) .....60 sec. max above 183°C, 230°C peak
T_A .....–40°C to 85°C
T_J .....–40°C to 150°C

Electrical Characteristics: $8V \le V_{BAT} \le 16V$, $8V \le VER \le 25V$, $1mA \le I_{V(OUT)} \le 100mA$, $T_{TEST} = –40^{\circ}C$ to $125^{\circ}C$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Linear Regulator					
Output Voltage	Output driven from V_{BAT}: VER = 25V Output driven from VER: V_{BAT} = 0V	4.9 4.9		5.1 5.1	V V
Regulator Bias Current (from V_{BAT})	$I_{V(BAT)}$ @ $I_{V(OUT)}$ = –100mA, SWSD = 4V, V_{BAT} = 16V, VER = 25V T = –40°C T = 25°C T = 125°C			 8 7 6	 mA mA mA
Regulator Bias Current (from VER)	I_{VER} @ $I_{V(OUT)}$ = –100mA SWSD = 4V, V_{BAT} = 0V, VER = 25V T = –40°C T = 25°C T = 125°C			 11 9 8	 mA mA mA
Dropout Voltage $V_{BAT} – V_{OUT}$	VER = 25V, $I_{V(OUT)}$ = –100mA (probe only)			1.5	V
Dropout Voltage VER – V_{OUT}	V_{BAT} = 0V, $I_{V(OUT)}$ = –100mA			1.5	V
Smart Switch Threshold V_{BAT} to VER	VER = 25V, $I_{V(OUT)}$ = –50mA	6.5		8.0	V
Smart Switch Threshold Hysteresis	VER = 25V, $I_{V(OUT)}$ = –50mA	0.5		1.0	V
V_{OUT} Output Noise	V_{BAT} = 16V, VER = 25V, $I_{V(OUT)}$ = –1mA C = 10µF, ESR = 0.5Ω			0.050	V
Line Regulation				0.025	V
Load Regulation				0.025	V
Output Current Limit		120			mA
■ Switching Regulator	**VER = 25V, $I_{V(OUT)}$ = –1mA**				
Switching Frequency	C_{PUMP} = 270pF, $R_{I(BIAS)}$ = 30.1kΩ	135	150	165	kHz
Pump Drive Current	$\Delta I_{V(BAT)}$ for $0A \le I_{V(SW)} \le 1.2A$			50	mA
Switch Saturation Voltage	$I_{V(SW)}$ = 1.2A			1.6	V
Output Current Limit		1.2		2.4	A
V_{FB} Regulation		1.238	1.270	1.303	V
V_{FB} Input Current	V_{FB} above short low detection level			1	µA
V_{FB} Input Shorted Low Detection Level		200	250	300	mV

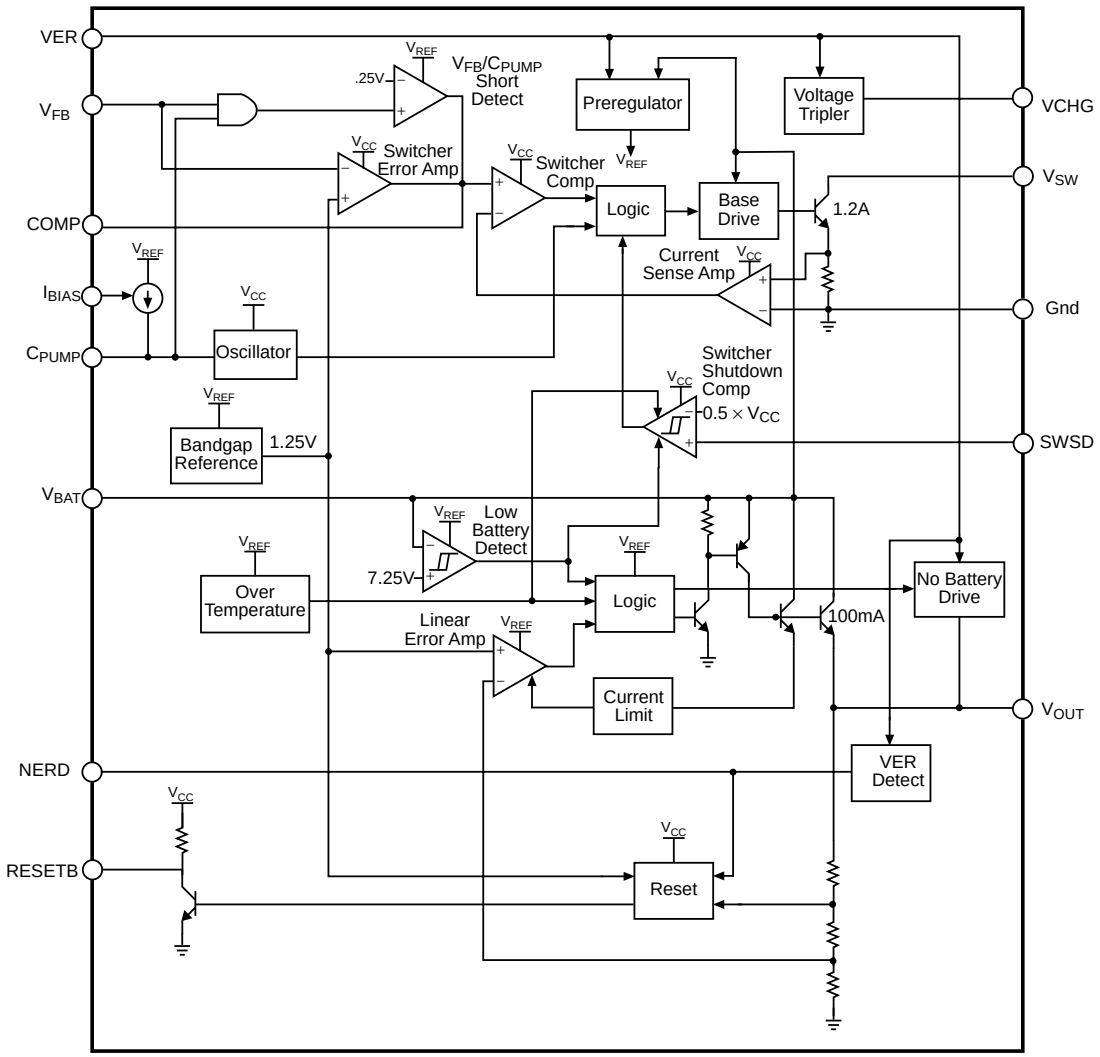
Electrical Characteristics: $8V \le V_{BAT} \le 16V$, $8V \le VER \le 25V$, $1mA \le I_{V(OUT)} \le 100mA$, $T_{TEST} = -40^{\circ}C$ to $125^{\circ}C$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Switching Regulator: continued					
C_{PUMP} Short detection threshold		200	250	300	mV
Maximum Duty Cycle		80		95	%
V_{SW} Leakage Current	$I_{V(SW)}$ @ V_{SW} = 50V, SWSD = V_{OUT}			100	µA
■ Voltage Tripler	**V_{BAT} = 16V, $I_{V(OUT)}$ = –1mA, C_{CHG} = 1.5µF**				
Output Voltage Clamp V_{CHG} – VER	VER = 8V, $I_{V(CHG)}$ = –30µA VER = 12V, $I_{V(CHG)}$ = –90µA	6.25 6.25	8.00 8.00	13.00 13.00	V V
Initial Charge Time	C_{CHG} = 0.15µF, VER = 8V, V_{CHG} = 14.25V			30	ms
Maximum Output Voltage Clamp V_{CHG}		25	32.5	40	V
Output Voltage Clamp V_{CHG}	VER = 28V, $I_{V(CHG)}$ = 0µA	25	32.5	40	V
Short Circuit Path Current Limit VER to V_{CHG}				3	mA
■ RESETB OUTPUT	**V_{BAT} = 0V**				
High Threshold	V_{OUT} increasing	4.525	4.750	4.850	V
Low Threshold	V_{OUT} decreasing	4.500	4.650	4.825	V
Hysteresis		25	100	200	mV
Output Low Voltage	V_{OUT} = 1.0V, I_{RESETB} = 100µA I_{RESETB} = 1mA, V_{OUT} = 4.5V			0.5 0.5	V V
Pull-Up Resistor	RESETB = 1V	25	50	100	kΩ
■ SWSD INPUT	**V_{BAT} = 16V, VER = 25V, $I_{V(OUT)}$ = –1mA**				
High Threshold				$0.7 \times V_{OUT}$	V
Low Threshold		$0.3 \times V_{OUT}$			V
Input Impedance	referenced to ground	10	20	40	kΩ
■ NERD OUTPUT	**V_{BAT} = 16V, $I_{V(OUT)}$ = –1mA, C_{NERD} = 0.47µF**				
VER Detection Voltage		1.5		6.5	V
Output Low Voltage	I_{NERD} = 1mA, V_{OUT} = 4.5V			0.5	V
Pull-Up Current	NERD = 0.5V	30	40	50	µA
Power on Delay		6.25	8.5	11	ms
Clamping Voltage (low)	VER present	1.00	1.25	1.50	V
Clamping Voltage (high)	VER not present	3.50	3.75	4.00	V
■ GENERAL					
VER Load Current	VER = 25V, V_{BAT} = 16V, $I_{V(OUT)}$ = –100mA T = –40°C T = 25°C T = 125°C			 5 5 4	 mA mA mA
Thermal Shutdown	(guaranteed by design)	160		210	°C

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
20 Lead SO Wide *(internally fused leads)*		
1	VER	Energy reserve input.
2	V_{BAT}	Battery input.
3	V_{FB}	Charge PUMP control voltage input.
4	Gnd1	Ground.
5	Gnd2	Ground.
6	Gnd3	Ground.
7	Gnd4	Ground.
8	V_{SW}	Charge PUMP switch collector.
9	SWSD	Charge PUMP shutdown input.
10	COMP	Charge PUMP compensation pin.
11	C_{PUMP}	Charge PUMP timing cap input.
12	I_{BIAS}	Reference current resistor pin.
13	V_{CHG}	Switched cap voltage tripler output.
14	Gnd5	Ground.
15	Gnd6	Ground.
16	Gnd7	Ground.
17	Gnd8	Ground.
18	NERD	No energy reserve detected output.
19	RESETB	Reset output.
20	V_{OUT}	Linear regulator output.

Block Diagram



Circuit Description

Figure 1 is an oscilloscope waveform showing the charge pump collector voltage, collector current and the charge pump timing capacitor during normal operation with I_{VER} = 30mA.

Figure 2 is an oscilloscope waveform showing the voltage tripler output and the energy reserve input during power up.

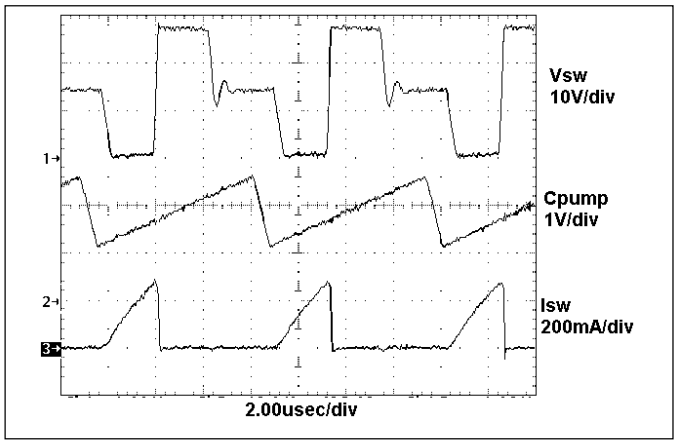


Figure 1. Typical operation with I_{VER} = 30mA.

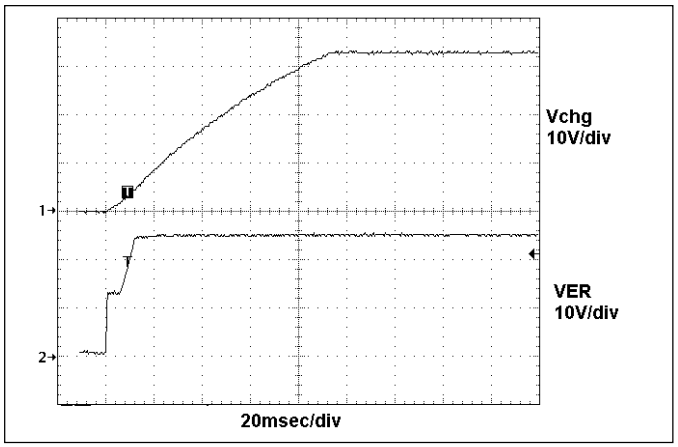


Figure 2. Startup with $R_{V(CHG)}$ = 510k.

Package Specification

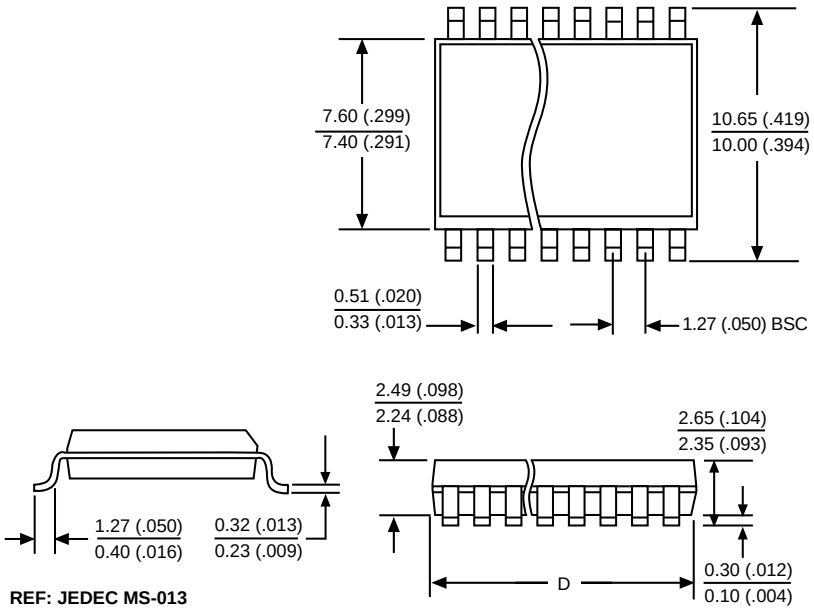
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
24 Lead SO Wide	13.00	12.60	.512	.496

PACKAGE THERMAL DATA

Thermal Data		20 Lead SO Wide *(internally fused leads)*	
$R_{\Theta JC}$	typ	9	°C / W
$R_{\Theta JA}$	typ	55	°C / W

Surface Mount Wide Body (DW); 300 mil wide



Ordering Information

Part Number	Description
CS2001YDWF20	20 Lead SO Wide *(internally fused leads)*
CS2001YDWFR20	20Lead SO Wide *(internally fused leads) (tape & reel)*

Notes

Notes