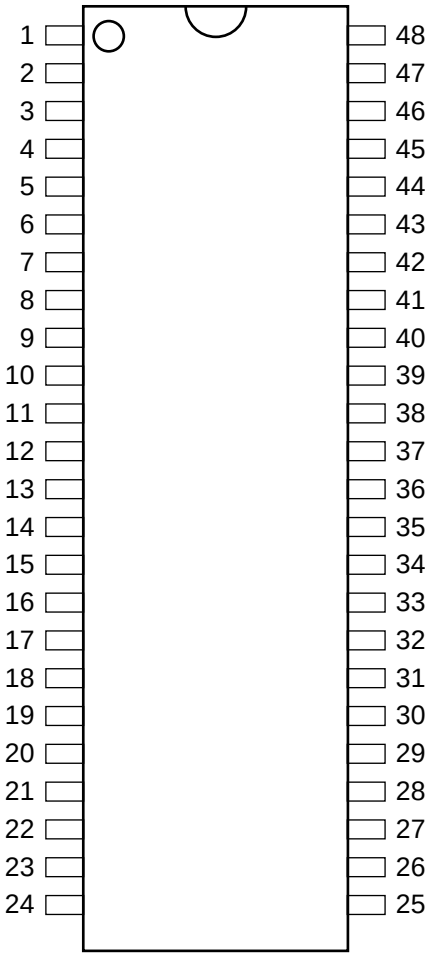
PHASE LOCK LOOP CLOCK DRIVER

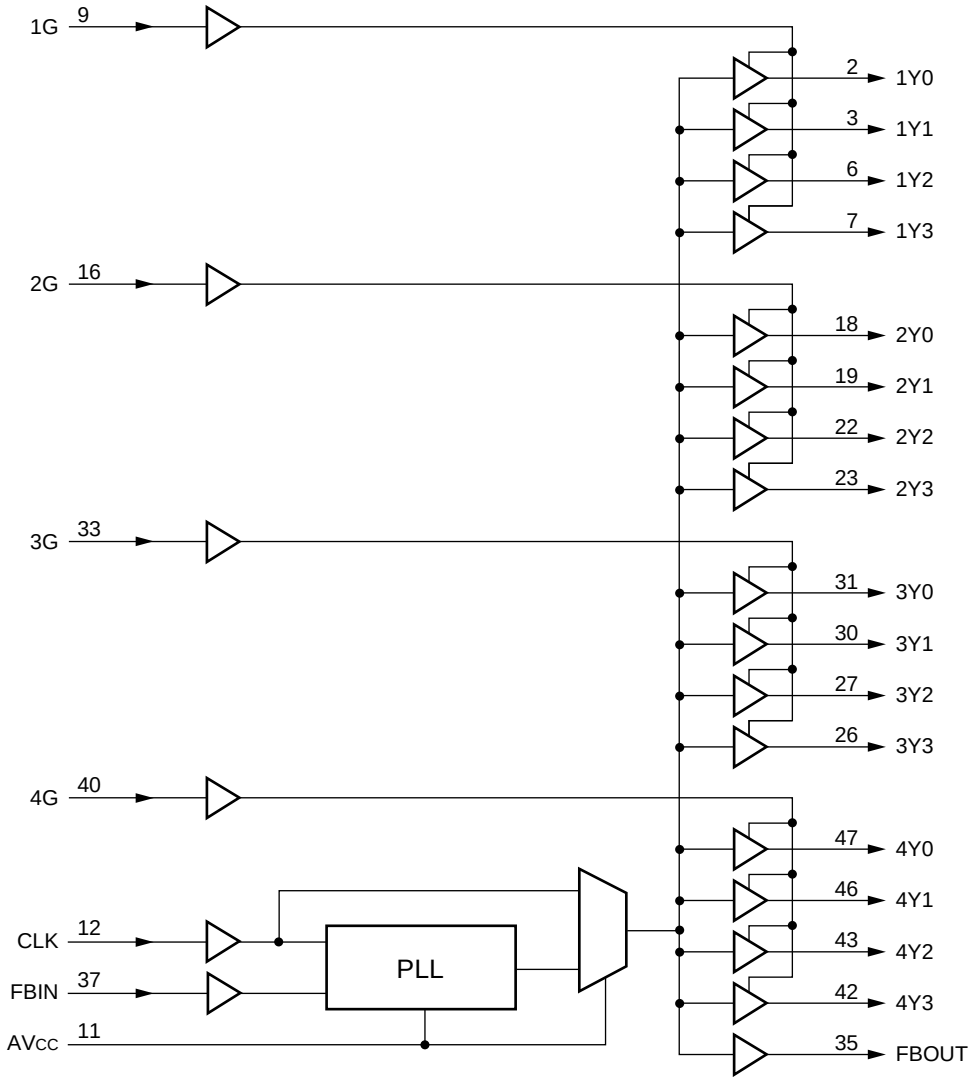
—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	VCC	25	—	VVCC
2	O	1Y0	26	O	3Y3
3	O	1Y1	27	O	3Y2
4	—	GND	28	—	GND
5	—	GND	29	—	GND
6	O	1Y2	30	O	3Y1
7	O	1Y3	31	O	3Y0
8	—	VCC	32	—	VCC
9	I	1G	33	I	3G
10	—	GND	34	—	GND
11	—	AVCC	35	O	FBOUT
12	I	CLK	36	—	AGND
13	—	AGND	37	I	FBIN
14	—	AGND	38	—	AVCC
15	—	GND	39	—	GND
16	I	2G	40	I	4G
17	—	VCC	41	—	VCC
18	O	2Y0	42	O	4Y3
19	O	2Y1	43	O	4Y2
20	—	GND	44	—	GND
21	—	GND	45	—	GND
22	O	2Y2	46	O	4Y1
23	O	2Y3	47	O	4Y0
24	—	VCC	48	—	VCC

INPUTS					OUTPUTS				
1G	2G	3G	4G	CLK	1Y	2Y	3Y	4Y	FBOUT
×	×	×	×	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	1	0	0	0	1	1
0	0	1	0	1	0	0	1	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	0	1	0	1	1
0	1	1	0	1	0	1	1	0	1
0	1	1	1	1	0	1	1	1	1
1	0	0	0	1	1	0	0	0	1
1	0	0	1	1	1	0	0	1	1
1	0	1	0	1	1	0	1	0	1
1	0	1	1	1	1	0	1	1	1
1	1	0	0	1	1	1	0	0	1
1	1	0	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE


1G
9
2G
16
3G
33
4G
40
CLK
12
FBIN
37
AVCC
11
PLL
2
1Y0
3
1Y1
6
1Y2
7
1Y3
18
2Y0
19
2Y1
22
2Y2
23
2Y3
31
3Y0
30
3Y1
27
3Y2
26
3Y3
47
4Y0
46
4Y1
43
4Y2
42
4Y3
35
FBOUT