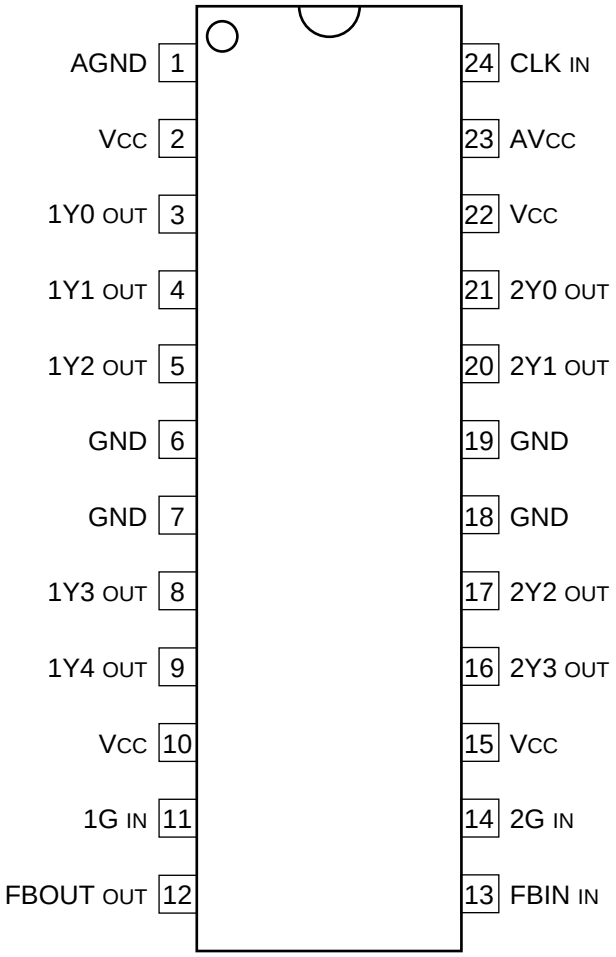
PHASE LOCK LOOP CLOCK DRIVER

—TOP VIEW—



INPUTS			OUTPUTS		
1G	2G	CLK	1Y	2Y	FBOUT
×	×	0	0	0	0
0	0	1	0	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	1

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE