CASERM/D
Rev. 0, Sep-2000

Semiconductor Packaging and Case Outlines

ON Semiconductor

Reference Manual and Design Guide

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Forward

By way of a definition, a semiconductor package constitutes the means of providing both an electrical and a mechanical interface for the active silicon (or gallium arsenide, or germanium, etc.) and the circuit assembly in which it provides its functions. It commonly comprises a protective body from which emerge metal electrical terminals. The body protects the semiconductor die from contamination (moisture, dirt, etc.) and interference (light photons, etc.), and the terminals provide the means to connect the chip to the surrounding circuitry (via soldering, crimping, or other conductive means of fastening.) Both the body–form and terminal–forms can take on a variety of shapes, depending on the semiconductor device's function, intended environment, power level, and assembly related factors. For this reason there are more than a hundred commonly used package styles, each having many variations.

The purpose of this manual is to bring together in a single source a useful compendium of package related information. This information heretofore existed, but was spread out over an entire library of data books, pamphlets, brochures, and application notes. It is hoped that the reader will find this edited compilation a useful tool to facilitate their circuit and assembly design activities.

Lonne Mays
System Applications Engineer

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Section 1

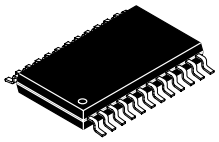
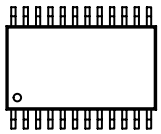
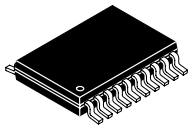
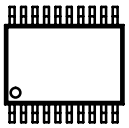
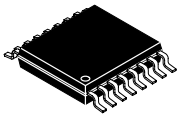
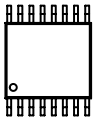
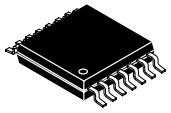
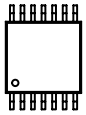
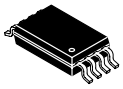
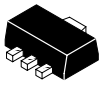
Common Package Reference Table

Common Packages

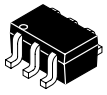
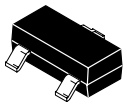
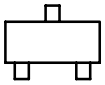
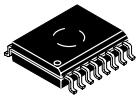
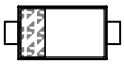
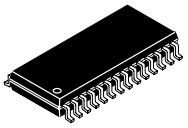
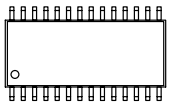
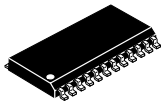
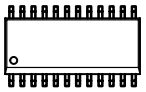
This section of the reference manual contains a tabular listing of more than 100 common package styles utilized by ON Semiconductor for analog integrated circuits, broadband and logic integrated circuits, discrete small signal semiconductors, and power semiconductors. The packages range in size from a few square millimeters in area to several square centimeters in area. Their power dissipations range from a hundred milli–Watts to more than 100 Watts.

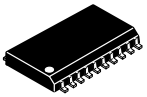
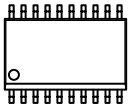
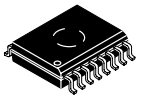
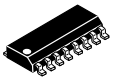
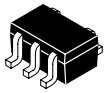
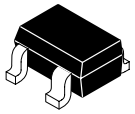
The table is organized by JEDEC package style categories to assist the engineer in quickly locating the desired information.

PACKAGE STYLE CHARACTERISTIC

	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Surface Mount	SO	TSSOP–24	N/A	CASE NO. 948H–01 (page 75)	 SCALE 2:1	
Surface Mount	SO	TSSOP–20	N/A	CASE NO. 948E–02 (page 73)	 SCALE 2:1	
Surface Mount	SO	TSSOP–16	N/A	CASE NO. 948F–01 (page 74)	 SCALE 2:1	
Surface Mount	SO	TSSOP–14	N/A	CASE NO. 948G–01 (page 74)	 SCALE 2:1	
Surface Mount	SO	TSSOP–8	N/A	CASE NO. 948J–01 (page 76)	 SCALE 2:1	
Surface Mount	SO	TSOP–6	N/A	CASE NO. 318G–02 (page 34)	 SCALE 2:1	
Surface Mount	SO	TSOP–5	N/A	CASE NO. 483–01 (page 47)	 SCALE 2:1	
Surface Mount	SO	SOT–89	N/A	CASE NO. 1213–01 (page 79)	 SCALE 2:1	

CASERM

	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Surface Mount	SO	SOT–363	N/A	CASE NO. 419B–01 (page 43)	 SCALE 4:1	
Surface Mount	SO	SOT–23L SIX LEAD	N/A	CASE NO. 318J–01 (page 35)	 SCALE 2:1	
Surface Mount	SO	SOT–23 FIVE LEAD	N/A	CASE NO. 1212–01 (page 79)	 SCALE 2:1	
Surface Mount	SO	SOT–23	TO–236AB	CASE NO. 318–08 (page 32)	 SCALE 4:1	
Surface Mount	SO	SOT–223	N/A	CASE NO. 318E–04 (page 33)	 SCALE 1:1	
Surface Mount	SO	SOP–16L	N/A	CASE NO. 751G–02 (page 58)	 SCALE 1:1	
Surface Mount	SO	SOD–323	N/A	CASE NO. 477–02 (page 47)	 SCALE 4:1	
Surface Mount	SO	SOD–123	N/A	CASE NO. 425–04 (page 44)	 SCALE 5:1	
Surface Mount	SO	SO–8	N/A	CASE NO. 751–06 (page 54)	 SCALE 1:1	
Surface Mount	SO	SO–28L	N/A	CASE NO. 751F–04 (page 58)	 SCALE 1:1	
Surface Mount	SO	SO–24L	N/A	CASE NO. 751E–05 (page 57)	 SCALE 1:1	

	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Surface Mount	SO	SO–20L	N/A	CASE NO. 751D–04 (page 57)	 SCALE 1:1	
Surface Mount	SO	SO–16L	N/A	CASE NO. 751G–02 (page 58)	 SCALE 1:1	
Surface Mount	SO	SO–16	N/A	CASE NO. 751B–05 (page 56)	 SCALE 1:1	
Surface Mount	SO	SO–14	N/A	CASE NO. 751A–03 (page 55)	 SCALE 1:1	
Surface Mount	SO	SMC	N/A	CASE NO. 403–03 (page 40)	 SCALE 1:1	
Surface Mount	SO	SMB	DO–214AA	CASE NO. 403A–03 (page 40)	 SCALE 1:1	
Surface Mount	SO	SMA	N/A	CASE NO. 403B–01 (page 41)	 SCALE 1:1	
Surface Mount	SO	SC–90/SOT–416	N/A	CASE NO. 463–01 (page 46)	 SCALE 4:1	
Surface Mount	SO	SC–88A/SOT–353	N/A	CASE NO. 419A–01 (page 42)	 SCALE 4:1	
Surface Mount	SO	SC–82AB	N/A	CASE NO. 419C–01 (page 44)	 SCALE 4:1	
Surface Mount	SO	SC–75/SOT–416	N/A	CASE NO. 463–01 (page 46)	 SCALE 4:1	
Surface Mount	SO	SC–74	N/A	CASE NO. 318F–02 (page 34)	 SCALE 2:1	

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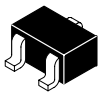
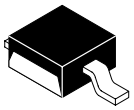
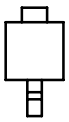
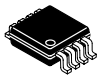
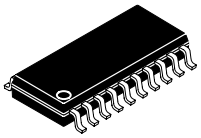
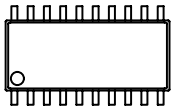
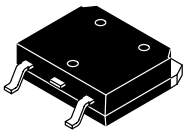
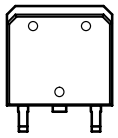
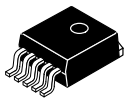
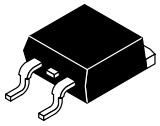
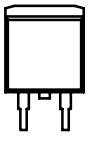
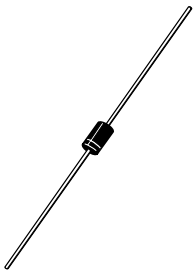
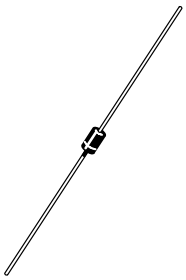
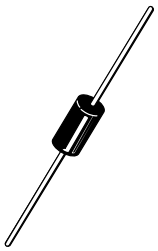
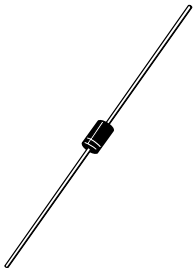
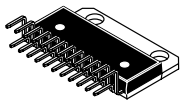
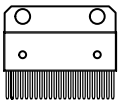
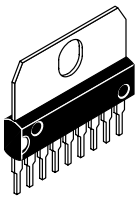
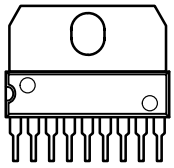
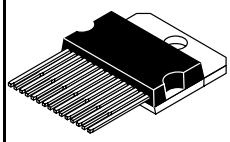
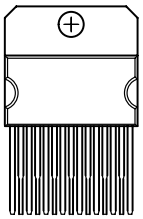
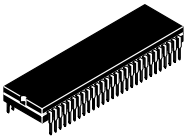
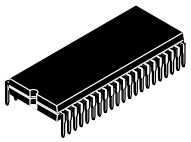
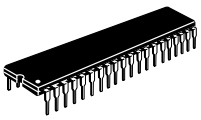
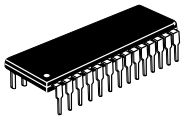
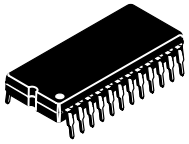
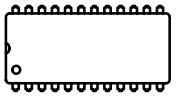
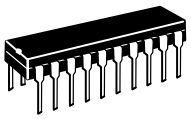
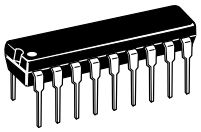
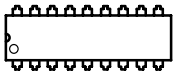
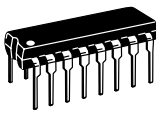
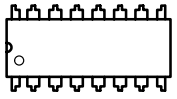
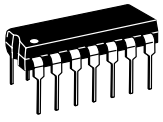
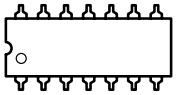
	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Surface Mount	SO	SC–70/SOT–323	N/A	CASE NO. 419–02 (page 42)	 SCALE 4:1	
Surface Mount	SO	SC–59 SIX LEAD	N/A	CASE NO. 318F–01 (page 34)	 SCALE 2:1	
Surface Mount	SO	SC–59	N/A	CASE NO. 318D–04 (page 33)	 SCALE 2:1	
Surface Mount	SO	POWERMITE®	N/A	CASE NO. 457–04 (page 45)	 SCALE 4:1	
Surface Mount	SO	Micro8™	N/A	CASE NO. 846A–02 (page 66)	 SCALE 2:1	
Surface Mount	SO	EIAJ–20	N/A	CASE NO. 967–01 (page 76)	 SCALE 2:1	
Surface Mount	SO	DPAK	N/A	CASE NO. 369A–13 (page 39)	 SCALE 1:1	
Surface Mount	SO	D^3PAK	N/A	CASE NO. 433–01 (page 45)	 SCALE 1:1	
Surface Mount	SO	D^2PAK 5–PIN	N/A	CASE NO. 936A–02 (page 73)	 SCALE 1:1	
Surface Mount	SO	D^2PAK	N/A	CASE NO. 418B–03 (page 41)	 SCALE 1:1	

	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Molded Axial	LF	SURMETIC 40	N/A	CASE NO. 17–02 (page 22)	 SCALE 1:1	
Molded Axial	LF	MOSORB	N/A	CASE NO. 41A–02 (page 25)	 SCALE 1:1	
Molded Axial	LF	MINI MOSORB	N/A	CASE NO. 59–04 (page 26)	 SCALE 1:1	
Molded Axial	LF	GLASS/PLASTIC DO–41	N/A	CASE NO. 59–03 (page 25)	 SCALE 1:1	
Molded Axial	LF	GLASS DO–35/DO–204AH	N/A	CASE NO. 299 (page 31)	 SCALE 1:1	

	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Molded Axial	LF	3A SURMETIC	N/A	CASE NO. 267–03	 SCALE 1:1	
Molded Axial	LF	1A SURMETIC	N/A	CASE NO. 59–04 (page 26)	 SCALE 1:1	
Inline Pin	IP	SZIP–23	N/A	CASE NO. 894–03 (page 71)	 SCALE 1:2	
Inline Pin	IP	SIP–9	N/A	CASE NO. 762–01 (page 59)	 SCALE 1:1	
Inline Pin	IP	SIP–15	N/A	CASE NO. 821D–03 (page 63)	 SCALE 1:1	
Inline Pin	IP	DIP–8	N/A	CASE NO. 626–05 (page 48)	 SCALE 1:1	
Inline Pin	IP	DIP–56 WIDE BODY	N/A	CASE NO. 859–01 (page 68)	 SCALE 1:1	

	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Inline Pin	IP	DIP–42 WIDE BODY	N/A	CASE NO. 858–01 (page 68)	 SCALE 1:1	
Inline Pin	IP	DIP–40 WIDE BODY	N/A	CASE NO. 711–03 (page 52)	 SCALE 1:1	
Inline Pin	IP	DIP–28 WIDE BODY	N/A	CASE NO. 710–02 (page 51)	 SCALE 1:2	
Inline Pin	IP	DIP–24 WIDE BODY	N/A	CASE NO. 649–03 (page 50)	 SCALE 1:1	
Inline Pin	IP	DIP–24	N/A	CASE NO. 724–03 (page 52)	 SCALE 1:2	
Inline Pin	IP	DIP–20	N/A	CASE NO. 738–03 (page 53)	 SCALE 1:1	
Inline Pin	IP	DIP–18	N/A	CASE NO. 707–02 (page 51)	 SCALE 1:1	
Inline Pin	IP	DIP–16	N/A	CASE NO. 648–08 (page 50)	 SCALE 1:1	
Inline Pin	IP	DIP–14	N/A	CASE NO. 646–06 (page 49)	 SCALE 1:1	

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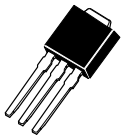
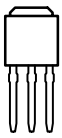
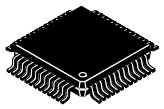
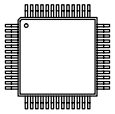
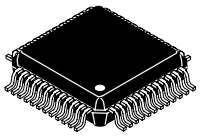
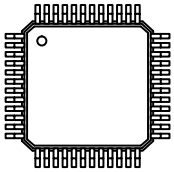
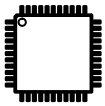
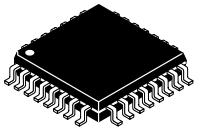
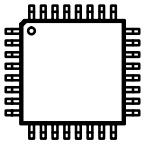
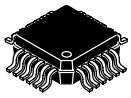
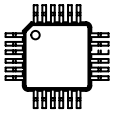
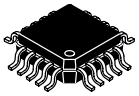
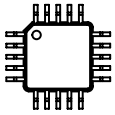
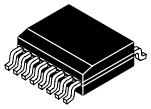
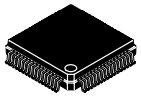
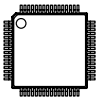
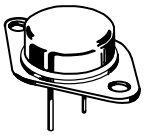
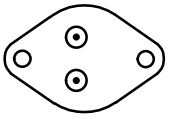
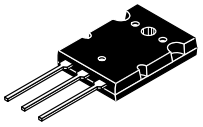
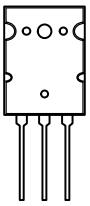
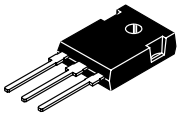
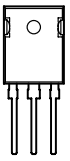
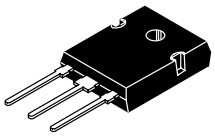
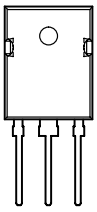
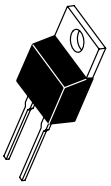
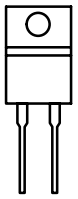
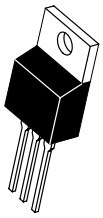
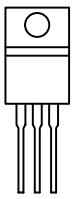
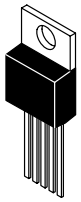
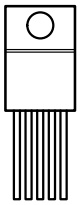
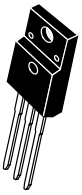
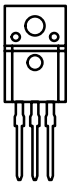
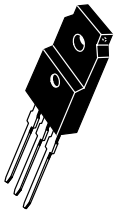
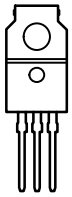
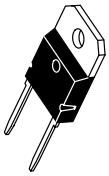
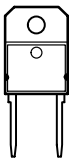
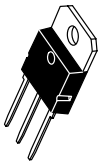
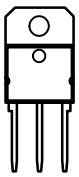
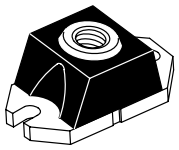
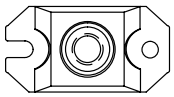
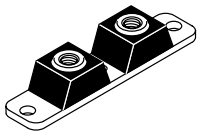
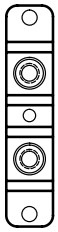
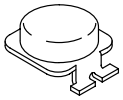
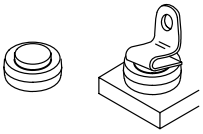
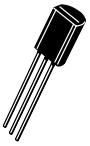
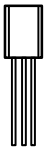
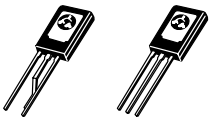
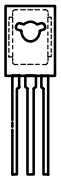
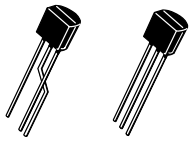
	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Inline Pin	IP	DPAK STRAIGHT LEADS	N/A	CASE NO. 369–07 (page 39)	 SCALE 1:1	
Flat Pack	FP	TQFP–52	N/A	CASE NO. 848B–04 (page 67)	 SCALE 1:1	
Flat Pack	FP	TQFP–49	N/A	CASE NO. 932–02 (page 72)	 SCALE 2:1	
Flat Pack	FP	TQFP–44	N/A	CASE NO. 824D–02 (page 64)	 SCALE 1:1	
Flat Pack	FP	TQFP–32	N/A	CASE NO. 873–01 (page 69)	 SCALE 2:1	
Flat Pack	FP	TQFP–24	N/A	CASE NO. 977–02 (page 78)	 SCALE 2:1	
Flat Pack	FP	TQFP–20	N/A	CASE NO. 976–02 (page 77)	 SCALE 2:1	
Flat Pack	FP	QSOP–16	N/A	TBD (page 80)	 SCALE 2:1	
Flat Pack	FP	QFP–64	N/A	CASE NO. 840F–02 (page 65)	 SCALE 1:1	

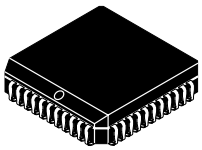
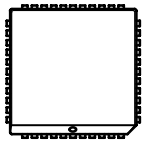
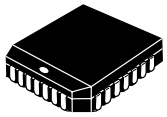
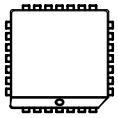
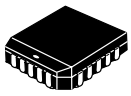
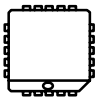
	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Flat Pack	FP	LQFP–32	N/A	CASE NO. 873A–02 (page 70)	 SCALE 1:1	
Flange Mounted	FM	TO–3 40 mil pins	TO–204AA	CASE NO. 1–07 (page 22)	 SCALE 1:2	
Flange Mounted	FM	TO–264/TO–3PBL	TO–264	CASE NO. 340G–02 (page 37)	 SCALE 1:2	
Flange Mounted	FM	TO–247	TO–247	CASE NO. 340K–01 (page 37)	 SCALE 1:1	
Flange Mounted	FM	TO–247	TO–247	CASE NO. 340F–03 (page 36)	 SCALE 1:1	
Flange Mounted	FM	TO–220 TWO LEAD	N/A	CASE NO. 221B–04 (page 30)	 SCALE 1:1	
Flange Mounted	FM	TO–220 THREE LEAD	TO–220AB	CASE NO. 221A–09 (page 29)	 SCALE 1:1	

CASERM

	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Flange Mounted	FM	TO–220 FIVE LEAD	N/A	CASE NO. 314D–04 (page 32)	 SCALE 1:1	
Flange Mounted	FM	TO–220 FULLPACK™ TRANSISTOR	N/A	CASE NO. 221D–02 (page 31)	 SCALE 1:1	
Flange Mounted	FM	TO–220 FULLPACK THYRISTOR	N/A	CASE NO. 221C–02 (page 30)	 SCALE 1:1	
Flange Mounted	FM	TO–218 TWO LEAD	TO–218	CASE NO. 340E–02 (page 36)	 SCALE 1:1	
Flange Mounted	FM	TO–218 THREE LEAD	TO–218	CASE NO. 340D–02 (page 35)	 SCALE 1:1	
Flange Mounted	FM	POWERTAP III	N/A	CASE NO. 357D–01 (page 38)	 SCALE 1:1	
Flange Mounted	FM	POWERTAP II	N/A	CASE NO. 357C–03 (page 38)	 SCALE 1:2	

	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Disk/Button	DB	TOPCAN	N/A	CASE NO. 460–02 (page 46)	 SCALE 1:1	
Disk/Button	DB	MICRODE BUTTON	N/A	CASE NO. 193–04 (page 27)	 SCALE 1:1	
Disk/Button	DB	BUTTON CAN	N/A	CASE NO. 193A–02 (page 28)	 SCALE 1:1	
Disk/Button	DB	AXIAL LEAD BUTTON	N/A	CASE NO. 194–04 (page 28)	 SCALE 1:1	
Non–Axial Cylinder	CY	TO–92 TWO LEAD	TO–226AC	CASE NO. 182–06 (page 27)	 SCALE 1:1	
Non–Axial Cylinder	CY	TO–92 1–WATT	TO–226AE	CASE NO. 29–10 (page 23)	 SCALE 1:1	
Flange Mounted	FM	TO–126	TO–225AA	CASE NO. 77–09 (page 26)	 SCALE 1:1	
Non–Axial Cylinder	CY	TO–92	TO–226AA	CASE NO. 29–11 (page 24)	 SCALE 1:1 SCALE 1:1	

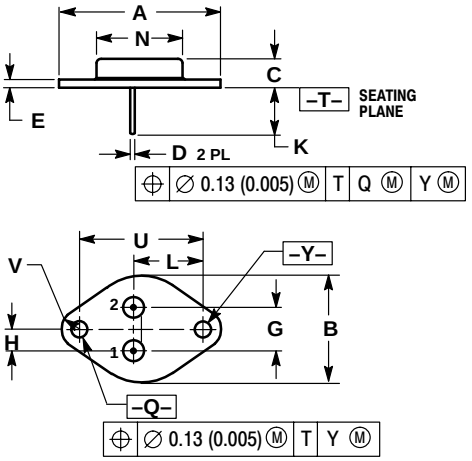
CASERM

	JEDEC STYLE CODE	COMMON PACKAGE DESIGNATION	JEDEC DESIGNATION	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE
Chip Carrier	CC	PLCC–44	N/A	CASE NO. 777–02 (page 62)	 SCALE 1:1	
Chip Carrier	CC	PLCC–28	N/A	CASE NO. 776–02 (page 61)	 SCALE 1:1	
Chip Carrier	CC	PLCC–20	N/A	CASE NO. 775–02 (page 60)	 SCALE 1:1	

Section 2

Case Outlines

TO–3 40 MIL PINS
TO–204AA
CASE 1–07
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

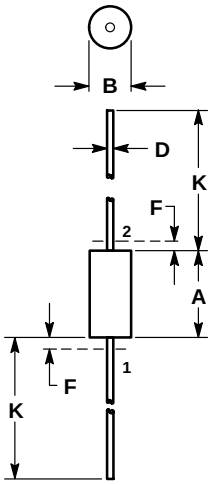
STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

SURMETIC 40
CASE 17–02
ISSUE C

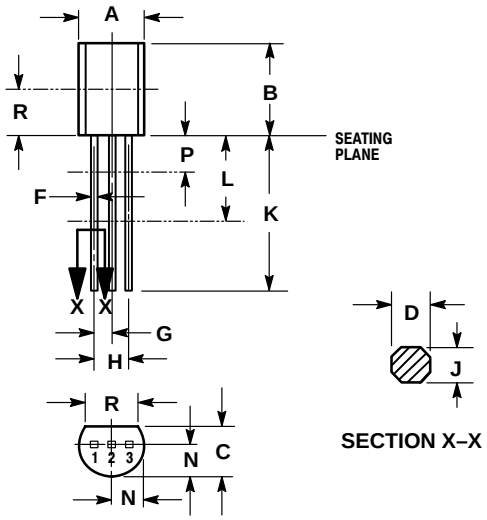


NOTES:
1. LEAD DIAMETER AND FINISH NOT CONTROLLED WITHIN DIMENSION F.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.330	0.350	8.38	8.89
B	0.130	0.145	3.30	3.68
D	0.037	0.043	0.94	1.09
F	---	0.050	---	1.27
K	1.000	1.250	25.40	31.75

STYLE 1:
PIN 1. ANODE
2. CATHODE

TO–92 1–WATT
TO–226AE
CASE 29–10
ISSUE AL



SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MIMIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.457	0.533
F	0.016	0.019	0.407	0.482
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

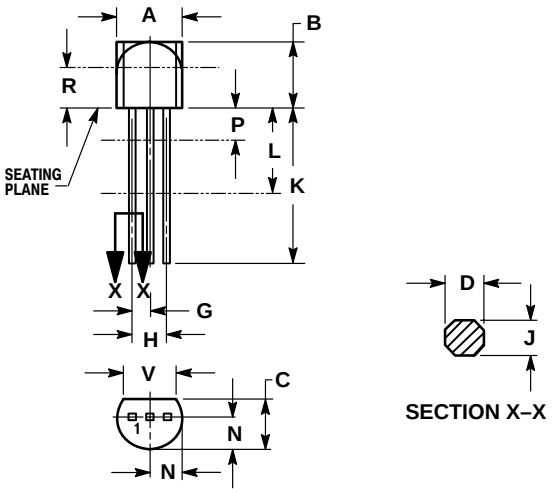
STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

TO–92
TO–226AA
CASE 29–11
ISSUE AL



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

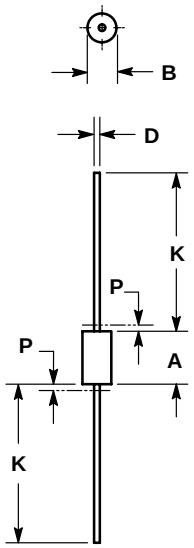
STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

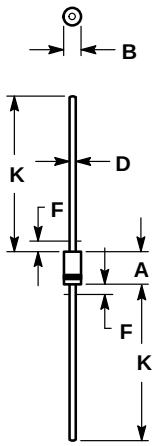
MOSORB
CASE 41A–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. LEAD FINISH AND DIAMETER UNCONTROLLED IN DIMENSION P.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.360	0.375	9.14	9.52
B	0.190	0.205	4.83	5.21
D	0.038	0.042	0.97	1.07
K	1.00	---	25.40	---
P	---	0.050	---	1.27

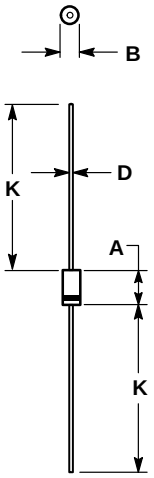
GLASS/PLASTIC
DO–41
CASE 59–03
ISSURE M



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO–41 OUTLINE SHALL APPLY.
2. POLARITY DENOTED BY CATHODE BAND.
3. LEAD DIAMETER NOT CONTROLLED WITHIN F DIMENSION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.07	5.20	0.160	0.205
B	2.04	2.71	0.080	0.107
D	0.71	0.86	0.028	0.034
F	---	1.27	---	0.050
K	27.94	---	1.100	---

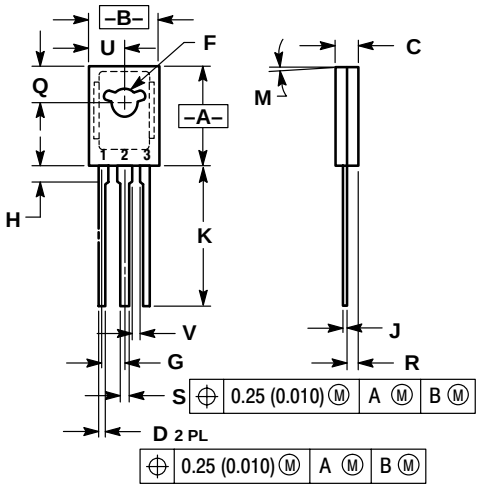
MINI MOSORB
CASE 59–04
ISSUE M



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO–41 OUTLINE SHALL APPLY.
2. POLARITY DENOTED BY CATHODE BAND.
3. LEAD DIAMETER NOT CONTROLLED WITHIN F DIMENSION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	---	1.100	---

TO–126
TO–225AA
CASE 77–09
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 4:
PIN 1. ANODE 1
2. ANODE 2
3. GATE

STYLE 5:
PIN 1. MT 1
2. MT 2
3. GATE

STYLE 6:
PIN 1. CATHODE
2. GATE
3. ANODE

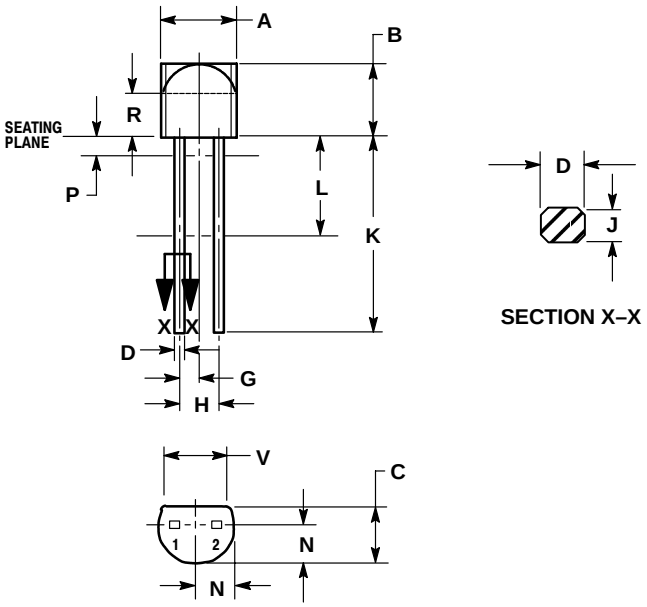
STYLE 7:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 8:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 9:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 10:
PIN 1. SOURCE
2. DRAIN
3. GATE

TO–92 TWO LEAD
TO–226AC
CASE 182–06
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND ZONE R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.21
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.050 BSC		1.27 BSC	
H	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.03	2.66
P	---	0.050	---	1.27
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 1:
PIN 1. ANODE
2. CATHODE

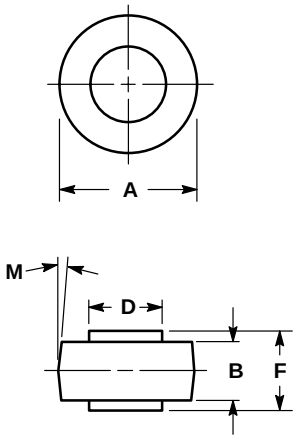
STYLE 2:
PIN 1. CATHODE
2. ANODE

STYLE 3:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2

STYLE 4:
CANCELLED

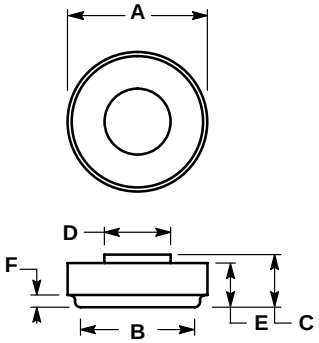
STYLE 5:
PIN 1. INPUT
2. OUTPUT

MICRODE BUTTON
CASE 193–04
ISSUE J



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.43	8.69	0.332	0.342
B	4.19	4.45	0.165	0.175
D	5.54	5.64	0.218	0.222
F	5.94	6.25	0.234	0.246
M	5° NOM		5° NOM	

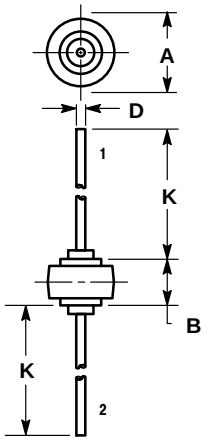
BUTTON CAN
CASE 193A–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.4	11.6	0.449	0.457
B	9.3	9.7	0.366	0.382
C	4.3	4.9	0.169	0.193
D	5.4	5.6	0.213	0.220
E	3.6	4.2	0.142	0.165
F	1.0	2.0	0.039	0.079

AXIAL LEAD BUTTON
CASE 194–04
ISSUE F

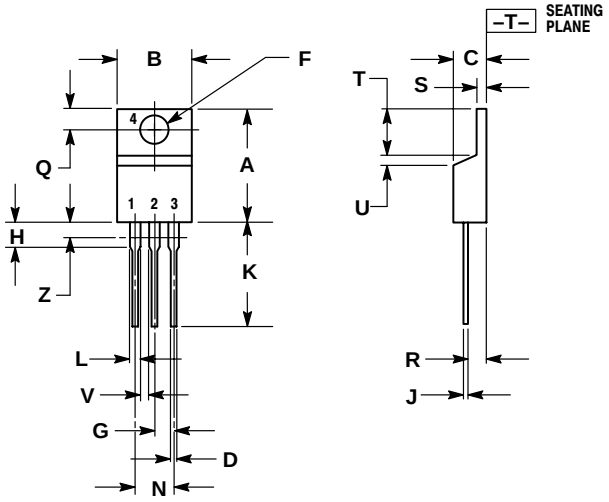


NOTES:
1. CATHODE SYMBOL ON PACKAGE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.43	8.69	0.332	0.342
B	5.94	6.25	0.234	0.246
D	1.27	1.35	0.050	0.053
K	25.15	25.65	0.990	1.010

STYLE 1:
PIN 1. CATHODE
2. ANODE

TO–220 THREE–LEAD
TO–220AB
CASE 221A–09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

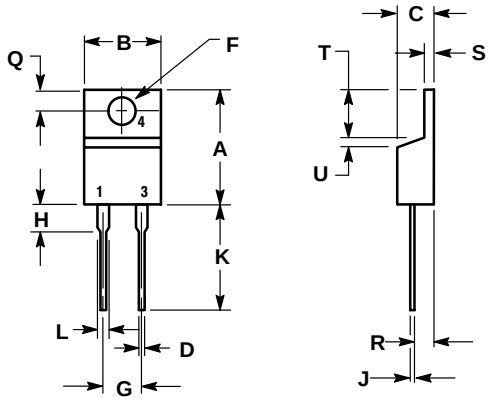
STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

TO–220 TWO–LEAD
CASE 221B–04
ISSUE D



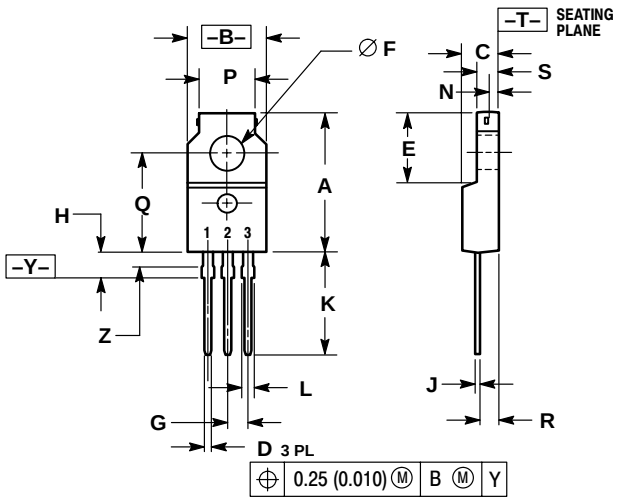
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.595	0.620	15.11	15.75
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.82
D	0.025	0.035	0.64	0.89
F	0.142	0.147	3.61	3.73
G	0.190	0.210	4.83	5.33
H	0.110	0.130	2.79	3.30
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.14	1.39
T	0.235	0.255	5.97	6.48
U	0.000	0.050	0.000	1.27

STYLE 1:
PIN 1. CATHODE
2. N/A
3. ANODE
4. CATHODE

STYLE 2:
PIN 1. ANODE
2. N/A
3. CATHODE
4. ANODE

TO–220 FULLPACK THYRISTOR
CASE 221C–02
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. LEAD DIMENSIONS UNCONTROLLED WITHIN DIMENSION Z.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.680	0.700	17.28	17.78
B	0.388	0.408	9.86	10.36
C	0.175	0.195	4.45	4.95
D	0.025	0.040	0.64	1.01
E	0.340	0.355	8.64	9.01
F	0.140	0.150	3.56	3.81
G	0.100 BSC		2.54 BSC	
H	0.110	0.155	2.80	3.93
J	0.018	0.028	0.46	0.71
K	0.500	0.550	12.70	13.97
L	0.045	0.070	1.15	1.77
N	0.049	---	1.25	---
P	0.270	0.290	6.86	7.36
Q	0.480	0.500	12.20	12.70
R	0.090	0.120	2.29	3.04
S	0.105	0.115	2.67	2.92
Z	0.070	0.090	1.78	2.28

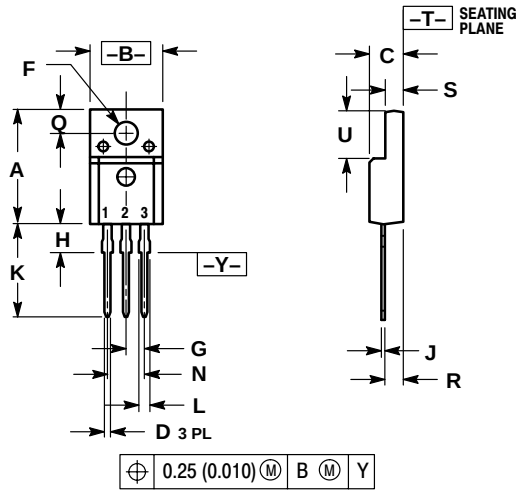
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 3:
PIN 1. MT 1
2. MT 2
3. GATE

STYLE 4:
PIN 1. GATE
2. DRAIN
3. SOURCE

TO–220 FULLPACK TRANSISTOR
CASE 221D–02
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

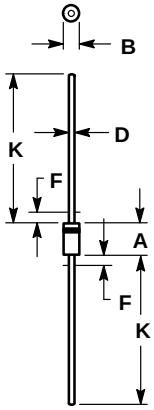
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE

GLASS DO–35/DO–204AH
CASE 299
ISSUE A

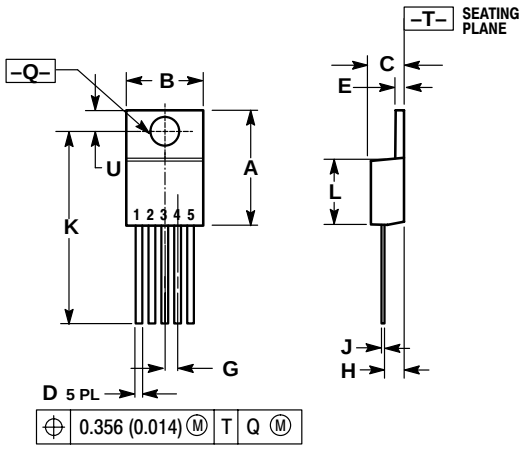


NOTES:
1. PACKAGE CONTOUR OPTIONAL WITHIN A AND B HEAT SLUGS, IF ANY, SHALL BE INCLUDED WITHIN THIS CYLINDER, BUT NOT SUBJECT TO THE MINIMUM LIMIT OF B.
2. LEAD DIAMETER NOT CONTROLLED IN ZONE F TO ALLOW FOR FLASH, LEAD FINISH BUILDUP AND MINOR IRREGULARITIES OTHER THAN HEAT SLUGS.
3. POLARITY DENOTED BY CATHODE BAND.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.05	5.08	0.120	0.200
B	1.52	2.29	0.060	0.090
D	0.46	0.56	0.018	0.022
F	---	1.27	---	0.050
K	25.40	38.10	1.000	1.500

All JEDEC dimensions and notes apply.

TO–220 FIVE–LEAD
CASE 314D–04
ISSUE E

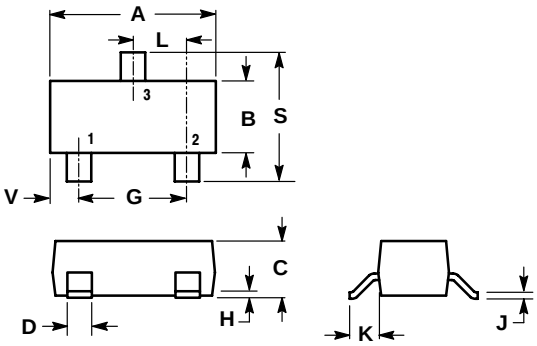


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.990	1.045	25.146	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

STYLE 1 THRU 4:
PIN 4. CANCELLED

SOT–23
TO–236AB
CASE 318–08
ISSUE AF



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE–ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE–ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

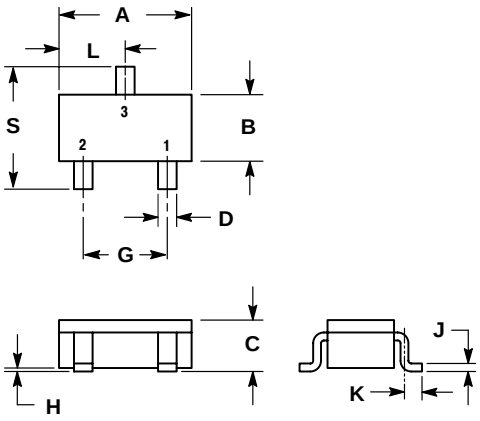
STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

SC–59
CASE 318D–04
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.70	3.10	0.1063	0.1220
B	1.30	1.70	0.0512	0.0669
C	1.00	1.30	0.0394	0.0511
D	0.35	0.50	0.0138	0.0196
G	1.70	2.10	0.0670	0.0826
H	0.013	0.100	0.0005	0.0040
J	0.09	0.18	0.0034	0.0070
K	0.20	0.60	0.0079	0.0236
L	1.25	1.65	0.0493	0.0649
S	2.50	3.00	0.0985	0.1181

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. N.C.
2. ANODE
3. CATHODE

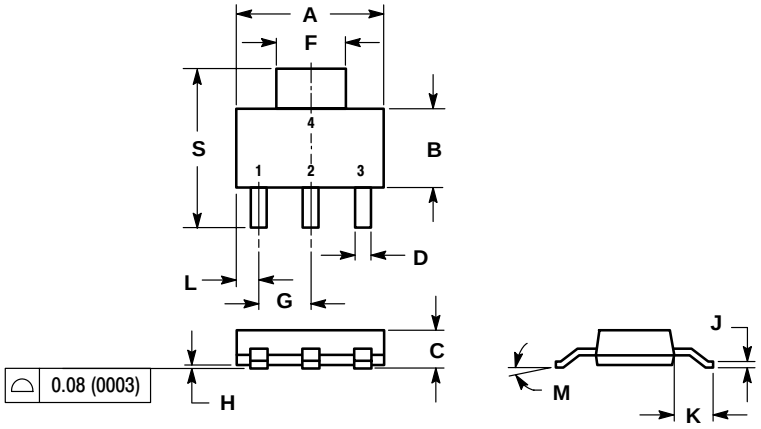
STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. N.C.
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. ANODE/CATHODE

SOT–223
CASE 318E–04
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

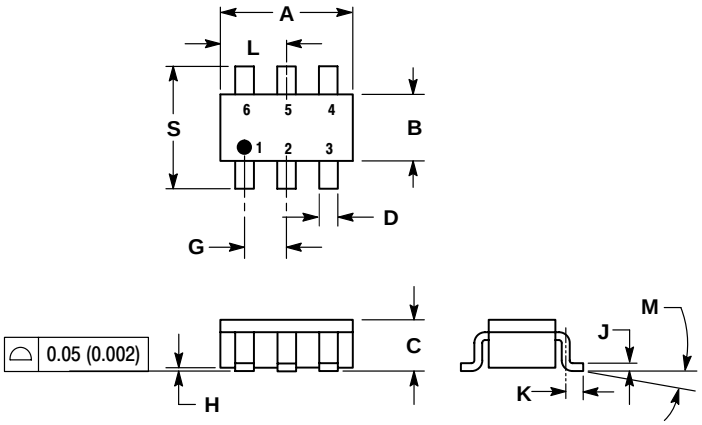
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SC–74
CASE 318F–02
ISSUE C



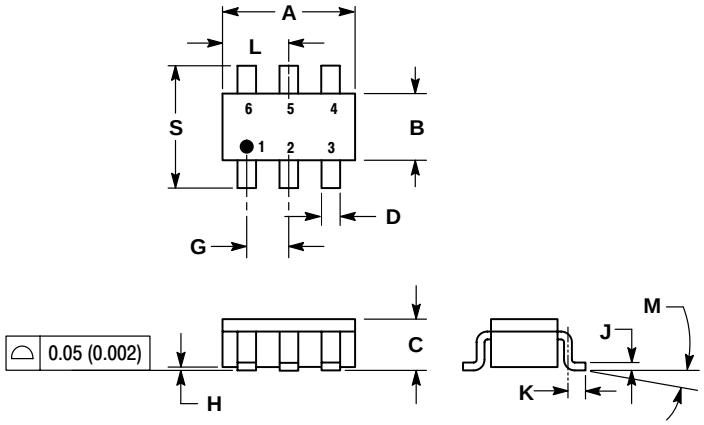
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1063	0.1220	2.70	3.10
B	0.0512	0.0669	1.30	1.70
C	0.0394	0.0511	1.00	1.30
D	0.0098	0.0157	0.25	0.40
G	0.0335	0.0413	0.85	1.05
H	0.0005	0.0040	0.013	0.100
J	0.0040	0.0102	0.10	0.26
K	0.0079	0.0236	0.20	0.60
L	0.0493	0.0649	1.25	1.65
M	0 °	10 °	0 °	10 °
S	0.0985	0.1181	2.50	3.00

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE

TSOP–6
CASE 318G–02
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

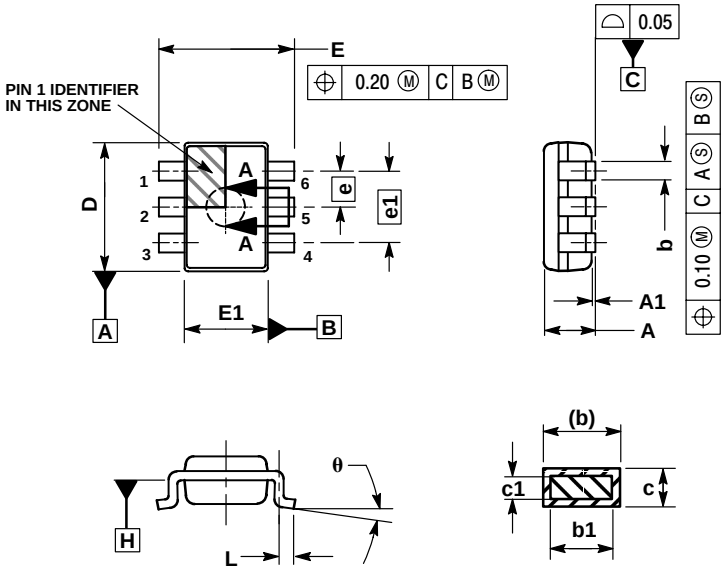
STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

SOT–23L
CASE 318J–02
ISSUE B

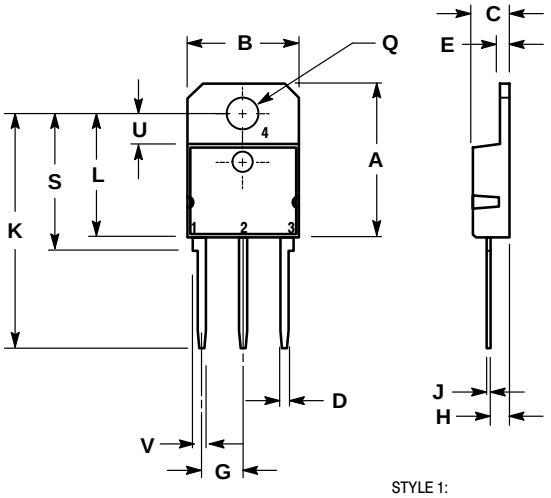


SECTION A–A

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.23 PER SIDE.
4. DIMENSIONS b AND b2 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.40
A1	0.00	0.10
b	0.35	0.50
b1	0.35	0.45
c	0.10	0.25
c1	0.10	0.20
D	3.20	3.60
E	3.00	3.60
E1	2.00	2.40
e	0.95	
e1	1.90	
L	0.25	0.55
θ	0 °	10 °

TO–218 THREE LEAD
TO–218
CASE 340D–02
ISSUE B



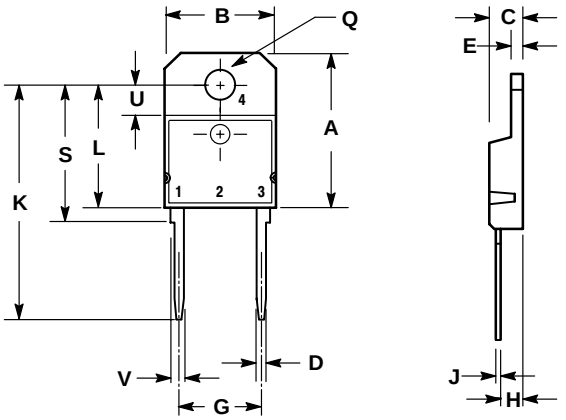
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

TO–218 TWO LEAD
TO–218
CASE 340E–02
ISSUE A

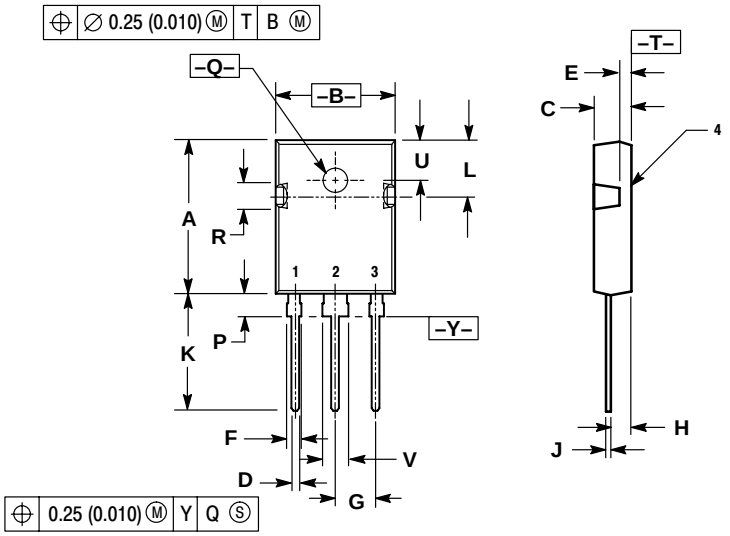


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	10.80	11.10	0.425	0.437
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

STYLE 1:
PIN 1. CATHODE
3. ANODE
4. CATHODE

TO–247
CASE 340F–03
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

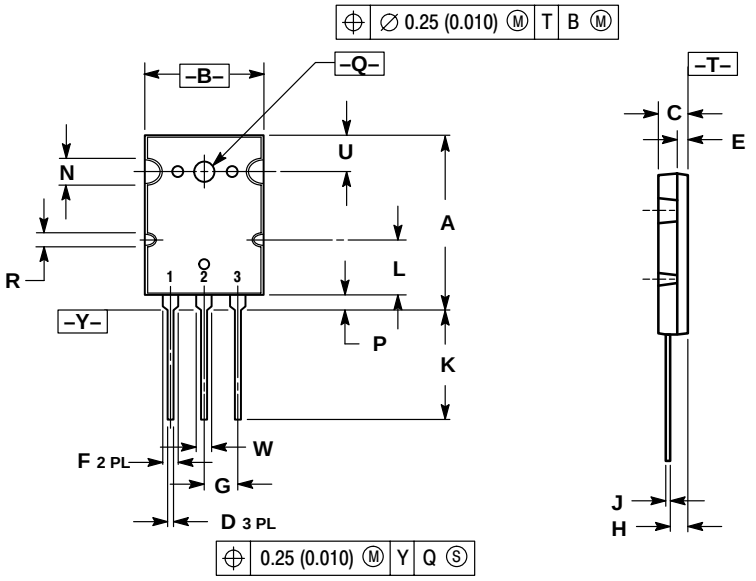
STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE 1
2. CATHODE (S)
3. ANODE 2
4. CATHODE (S)

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

TO–264/TO–3PBL
TO–264
CASE 340G–02
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.8	2.9	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

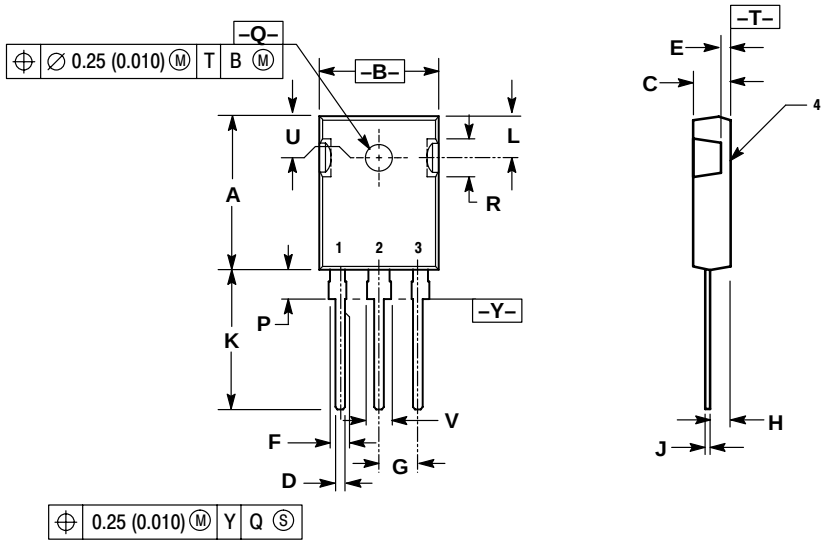
STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 5:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

TO–247
CASE 340K–01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
F	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
J	0.4	0.8	0.016	0.031
K	14.2	14.8	0.559	0.583
L	5.5 NOM		0.217 NOM	
P	3.7	4.3	0.146	0.169
Q	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

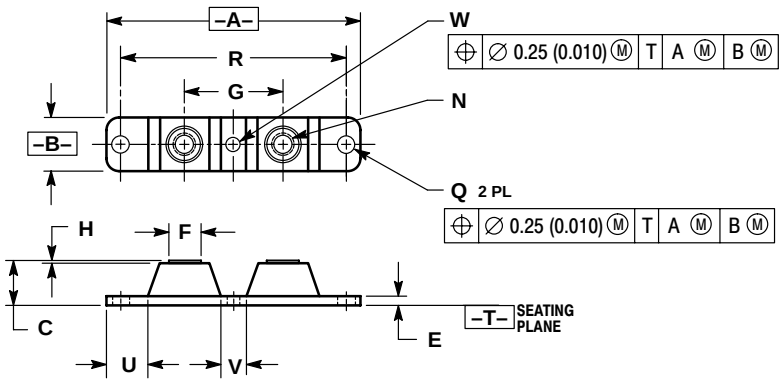
STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE 1
2. CATHODE(S)
3. ANODE 2
4. CATHODE(S)

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

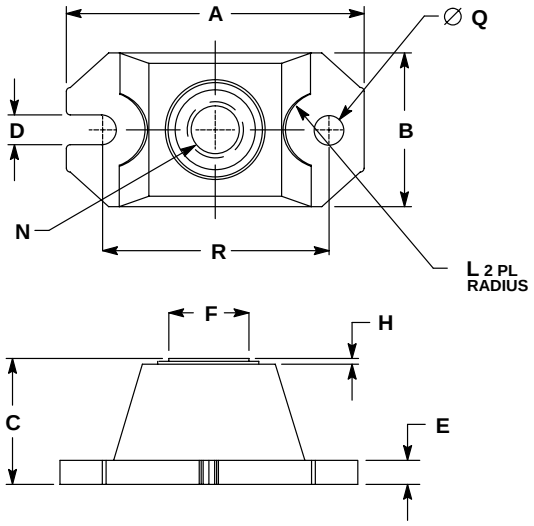
POWERTAP™ II
CASE 357C–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TERMINAL PENETRATION: 5.97 (0.235) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	3.450	3.635	87.63	92.33
B	0.700	0.810	17.78	20.57
C	0.615	0.640	15.63	16.26
E	0.120	0.130	3.05	3.30
F	0.435	0.445	11.05	11.30
G	1.370	1.380	34.80	35.05
H	0.007	0.030	0.18	0.76
N	1/4–20UNC–2B		1/4–20UNC–2B	
Q	0.270	0.285	6.86	7.23
R	31.50 BSC		80.01 BSC	
U	0.600	0.630	15.24	16.00
V	0.330	0.375	8.39	9.52
W	0.170	0.190	4.32	4.82

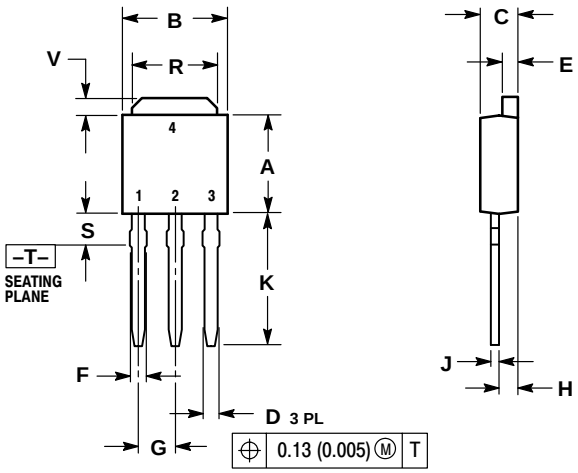
POWERTAP III
CASE 357D–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TERMINAL PENETRATION: 5.97 (0.235) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.520	1.560	38.61	39.62
B	0.783	0.813	19.89	20.65
C	0.615	0.635	15.62	16.13
D	0.152	0.162	3.86	4.11
E	0.120	0.130	3.05	3.30
F	0.435	0.445	11.05	11.30
H	0.007	0.030	0.18	0.76
L	0.210	0.230	5.33	5.84
N	1/4–20UNC–2B		1/4–20UNC–2B	
Q	0.152	0.162	3.86	4.11
R	1.175	1.195	29.85	30.35

DPAK STRAIGHT LEADS
CASE 369–07
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

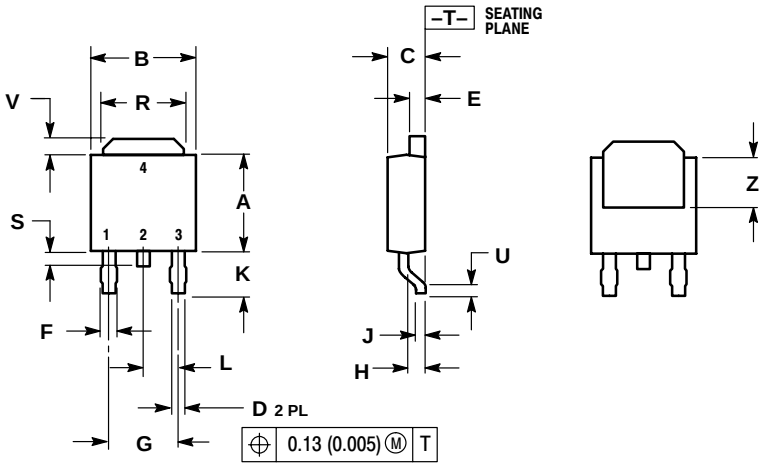
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DPAK
CASE 369A–13
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

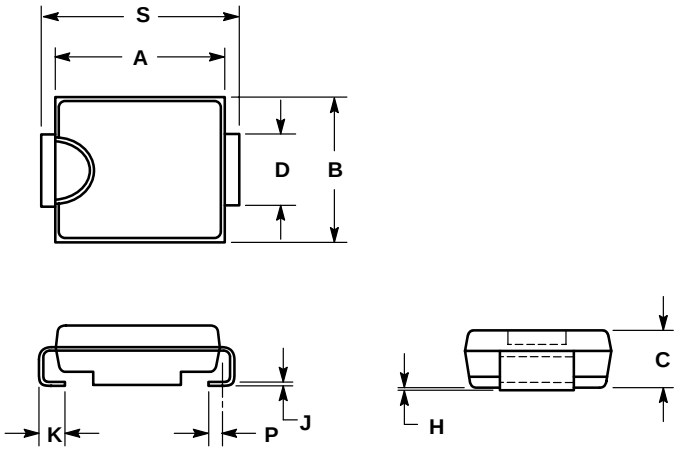
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

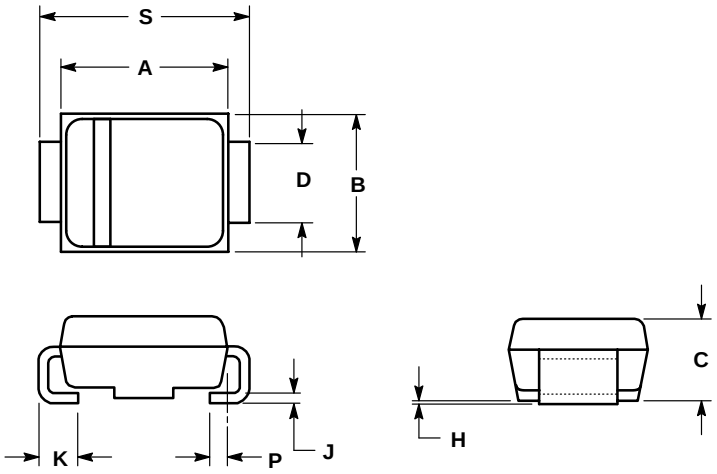
SMC
CASE 403–03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.260	0.280	6.60	7.11
B	0.220	0.240	5.59	6.10
C	0.075	0.095	1.90	2.41
D	0.115	0.121	2.92	3.07
H	0.0020	0.0060	0.051	0.152
J	0.006	0.012	0.15	0.30
K	0.030	0.050	0.76	1.27
P	0.020 REF		0.51 REF	
S	0.305	0.320	7.75	8.13

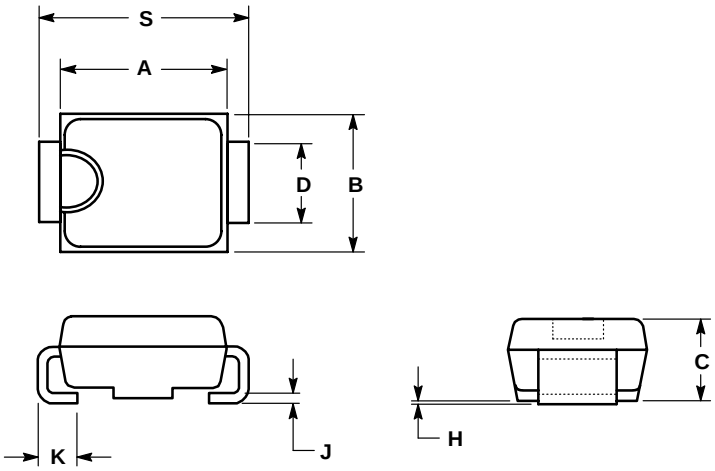
SMB
DO–214AA
CASE 403A–03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.160	0.180	4.06	4.57
B	0.130	0.150	3.30	3.81
C	0.075	0.095	1.90	2.41
D	0.077	0.083	1.96	2.11
H	0.0020	0.0060	0.051	0.152
J	0.006	0.012	0.15	0.30
K	0.030	0.050	0.76	1.27
P	0.020 REF		0.51 REF	
S	0.205	0.220	5.21	5.59

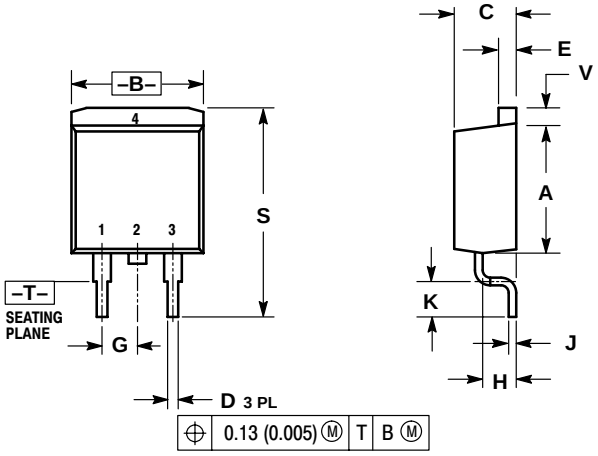
SMA
CASE 403B–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.160	0.180	4.06	4.57
B	0.090	0.115	2.29	2.92
C	0.075	0.105	1.91	2.67
D	0.050	0.064	1.27	1.63
H	0.004	0.008	0.10	0.20
J	0.006	0.016	0.15	0.41
K	0.030	0.060	0.76	1.52
S	0.190	0.220	4.83	5.59

D^{2}PAK
CASE 418B–03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

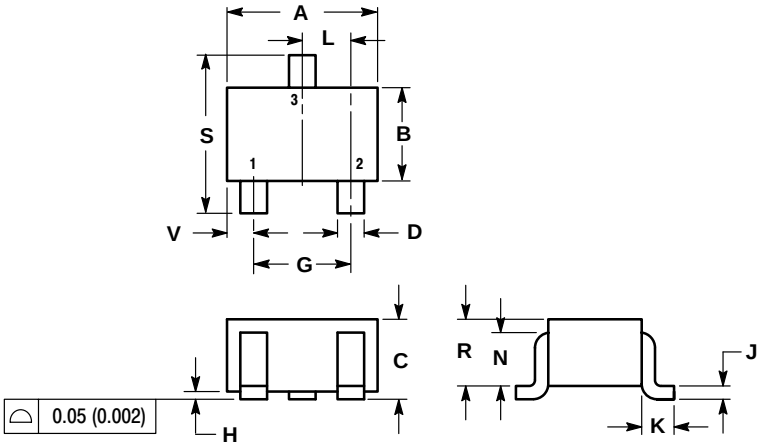
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

SC–70/SOT–323
CASE 419–02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.035	0.049	0.90	1.25
D	0.012	0.016	0.30	0.40
G	0.047	0.055	1.20	1.40
H	0.000	0.004	0.00	0.10
J	0.004	0.010	0.10	0.25
K	0.017 REF		0.425 REF	
L	0.026 BSC		0.650 BSC	
N	0.028 REF		0.700 REF	
R	0.031	0.039	0.80	1.00
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

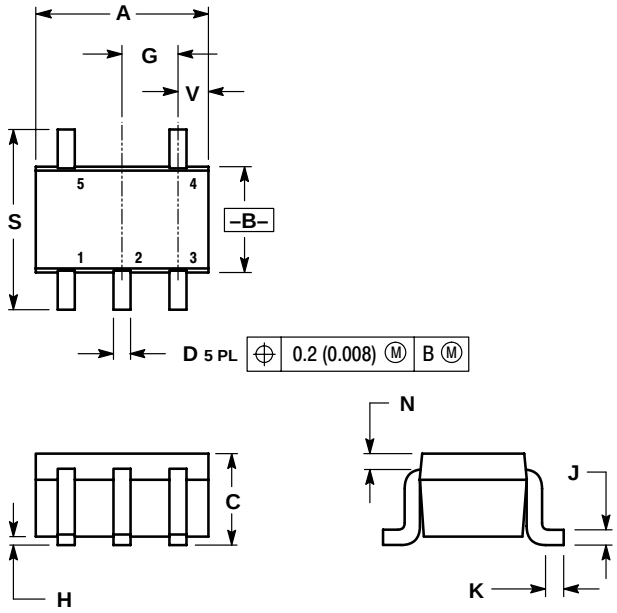
STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE–ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE–CATHODE

SC–88A/SOT–353
CASE 419A–01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

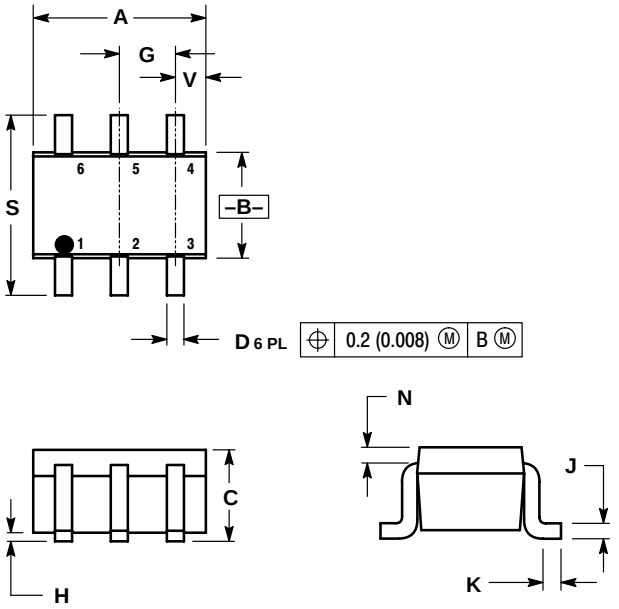
STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

SOT–363
CASE 419B–01
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE
2. ANODE
3. ANODE
4. CATHODE
5. CATHODE
6. CATHODE

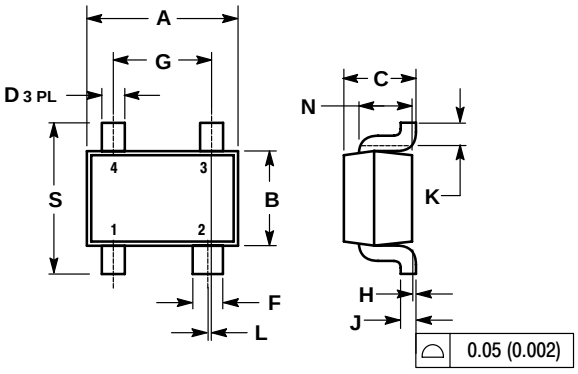
STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

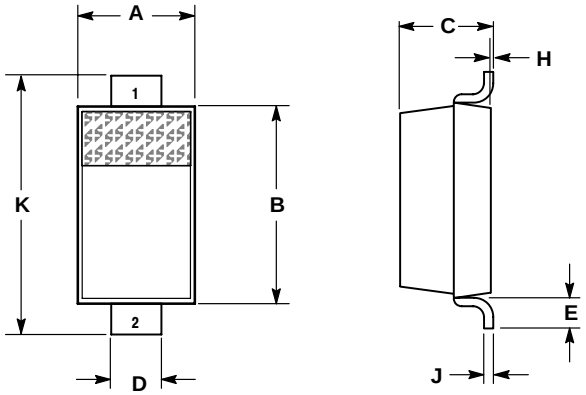
SC–82AB
CASE 419C–01
ISSUE 0



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.8	2.2	0.071	0.087
B	1.15	1.45	0.045	0.057
C	0.8	1.1	0.031	0.043
D	0.2	0.4	0.008	0.016
F	0.3	0.5	0.012	0.020
G	1.1	1.5	0.043	0.059
H	0.0	0.1	0.000	0.004
J	0.10	0.26	0.004	0.010
K	0.1	---	0.004	---
L	0.05 BSC		0.002 BSC	
N	0.7 REF		0.028 REF	
S	1.8	2.4	0.07	0.09

SOD–123
CASE 425–04
ISSUE C

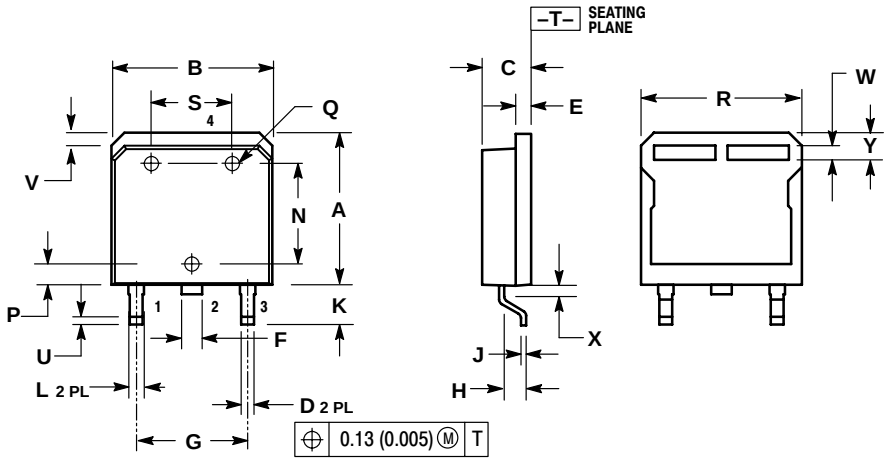


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.055	0.071	1.40	1.80
B	0.100	0.112	2.55	2.85
C	0.037	0.053	0.95	1.35
D	0.020	0.028	0.50	0.70
E	0.01	---	0.25	---
H	0.000	0.004	0.00	0.10
J	---	0.006	---	0.15
K	0.140	0.152	3.55	3.85

STYLE 1:
PIN 1. CATHODE
2. ANODE

D^{3}PAK
CASE 433–01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

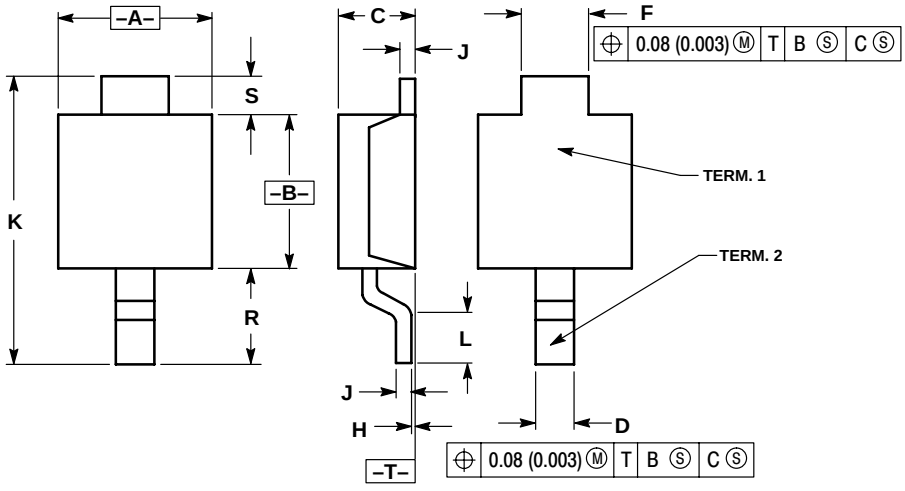
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.588	0.592	14.94	15.04
B	0.623	0.627	15.82	15.93
C	0.196	0.200	4.98	5.08
D	0.048	0.052	1.22	1.32
E	0.058	0.062	1.47	1.57
F	0.078	0.082	1.98	2.08
G	0.430 BSC		10.92 BSC	
H	0.105	0.110	2.67	2.79
J	0.018	0.022	0.46	0.56
K	0.150	0.160	3.81	4.06
L	0.058	0.062	1.47	1.57
N	0.353	0.357	8.97	9.07
P	0.078	0.082	1.98	2.08
Q	0.053	0.057	1.35	1.45
R	0.623	0.627	15.82	15.93
S	0.313	0.317	7.95	8.05
U	0.028	0.032	0.71	0.81
V	0.050	---	1.27	---
W	0.054	0.058	1.37	1.47
X	0.050	0.060	1.27	1.52
Y	0.104	0.108	2.64	2.74

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

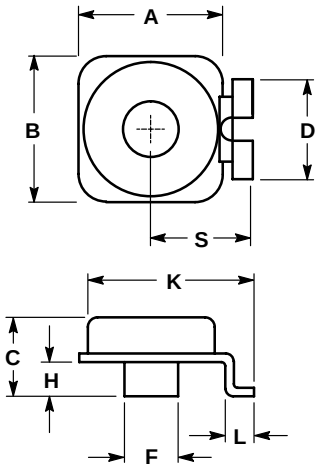
POWERMITE®
CASE 457–04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.75	2.05	0.069	0.081
B	1.75	2.18	0.069	0.086
C	0.85	1.15	0.033	0.045
D	0.40	0.69	0.016	0.027
F	0.70	1.00	0.028	0.039
H	–0.05	+0.10	–0.002	+0.004
J	0.10	0.25	0.004	0.010
K	3.60	3.90	0.142	0.154
L	0.50	0.80	0.020	0.031
R	1.20	1.50	0.047	0.059
S	0.50 REF		0.019 REF	

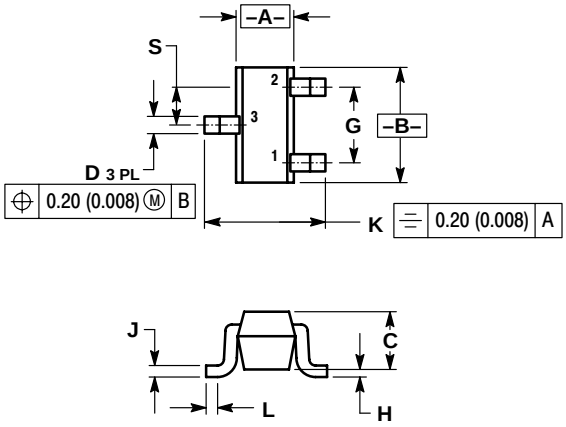
TOP CAN
CASE 460–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.1	9.5	0.358	0.374
B	9.5	9.9	0.374	0.390
C	5.2	5.6	0.205	0.220
D	6.4	6.8	0.252	0.268
F	3.4	3.8	0.134	0.149
H	2.0	2.4	0.079	0.095
K	11.3	11.7	0.445	0.460
L	1.7	2.1	0.067	0.083
S	6.5	6.9	0.256	0.272

SC–90/SOT–416 & SC–75/SOT–416
CASE 463–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	0.70	0.80	0.028	0.031
B	1.40	1.80	0.055	0.071
C	0.60	0.90	0.024	0.035
D	0.15	0.30	0.006	0.012
G	1.00 BSC		0.039 BSC	
H	---	0.10	---	0.004
J	0.10	0.25	0.004	0.010
K	1.45	1.75	0.057	0.069
L	0.10	0.20	0.004	0.008
S	0.50 BSC		0.020 BSC	

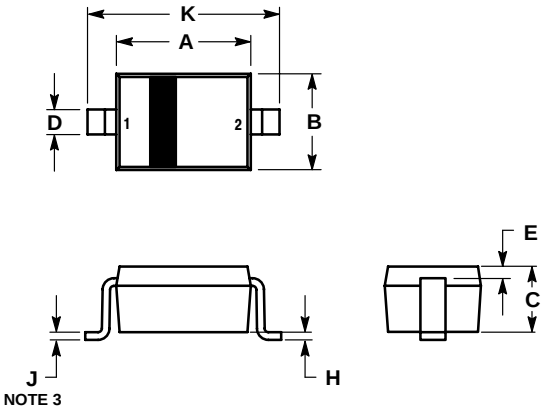
STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

SOD–323
CASE 477–02
ISSUE B

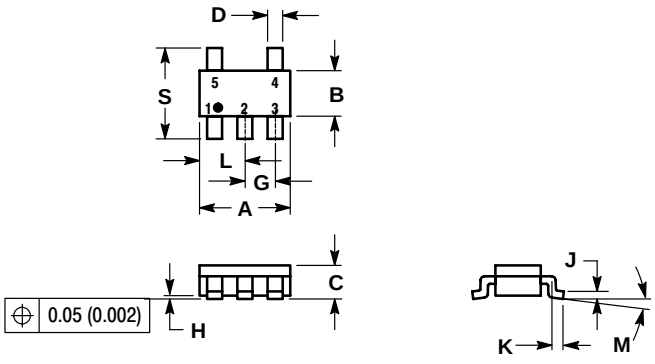


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS SPECIFIED PER L/F DRAWING WITH SOLDER PLATING.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.60	1.80	0.063	0.071
B	1.15	1.35	0.045	0.053
C	0.80	1.00	0.031	0.039
D	0.25	0.40	0.010	0.016
E	0.15 REF		0.006 REF	
H	0.00	0.10	0.000	0.004
J	0.089	0.177	0.0035	0.0070
K	2.30	2.70	0.091	0.106

STYLE 1:
PIN 1. CATHODE
2. ANODE

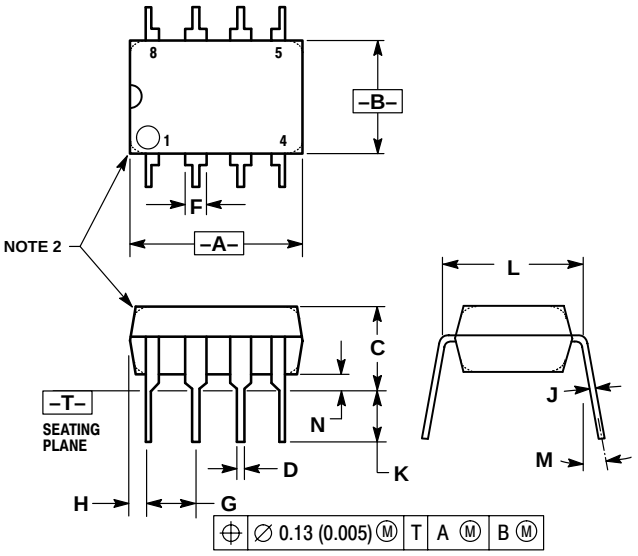
TSOP–5
CASE 483–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.00	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

DIP–8
CASE 626–05
ISSUE K

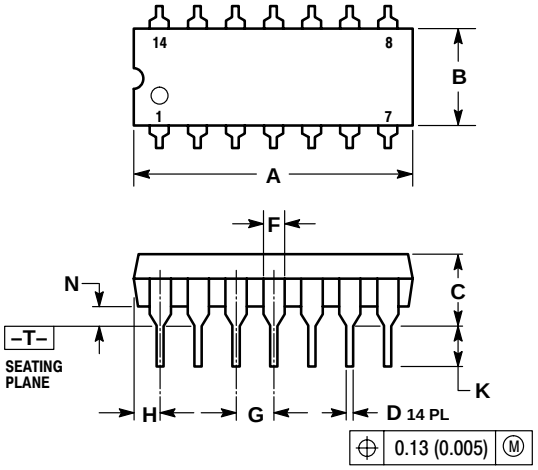


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

DIP–14
CASE 646–06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. NO CONNECTION
5. GATE
6. SOURCE
7. DRAIN
8. DRAIN
9. SOURCE
10. GATE
11. NO CONNECTION
12. GATE
13. SOURCE
14. DRAIN

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. NO CONNECTION
5. SOURCE
6. DRAIN
7. GATE
8. GATE
9. DRAIN
10. SOURCE
11. NO CONNECTION
12. SOURCE
13. DRAIN
14. GATE

STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

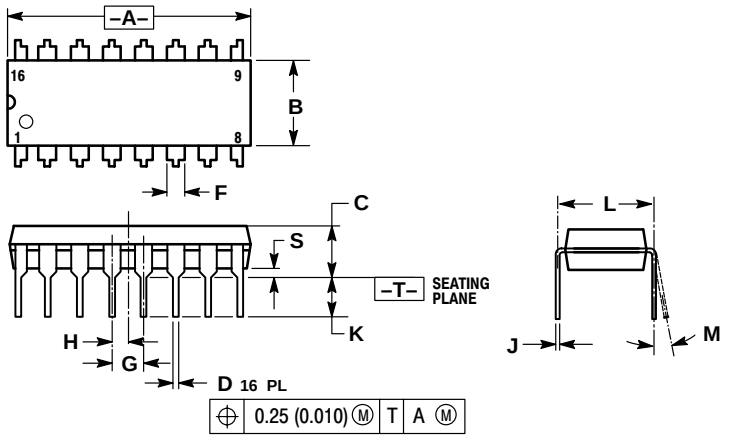
STYLE 9:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

STYLE 10:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 12:
PIN 1. COMMON CATHODE
2. COMMON ANODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. COMMON ANODE
7. COMMON CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
14. ANODE/CATHODE

DIP–16
CASE 648–08
ISSUE R



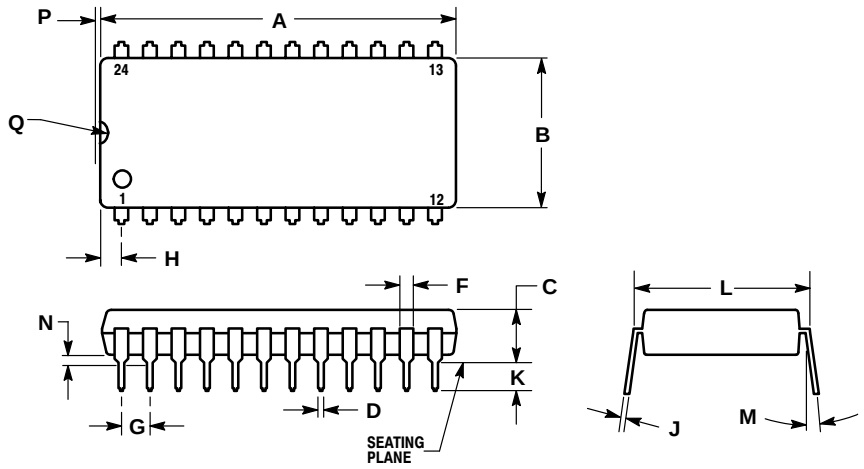
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

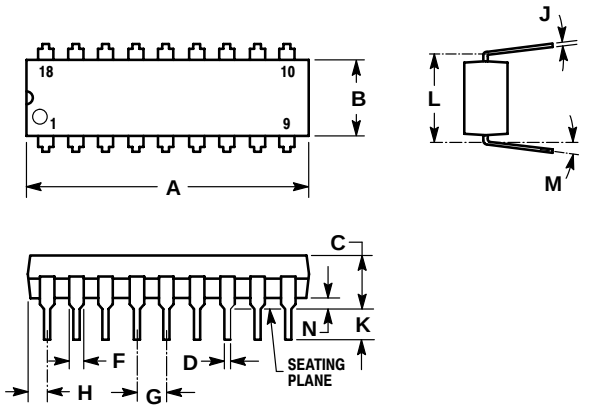
DIP–24 WIDE BODY
CASE 649–03
ISSUE D



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. CONTROLLING DIMENSION:INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.240	1.265	31.50	32.13
B	0.520	0.540	13.21	13.72
C	0.185	0.205	4.70	5.21
D	0.015	0.020	0.38	0.51
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.085	1.65	2.16
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.590	0.610	14.99	15.49
M	---	10°	---	10°
N	0.020	0.040	0.51	1.02
P	0.005	0.015	0.13	0.38
Q	0.020	0.030	0.51	0.76

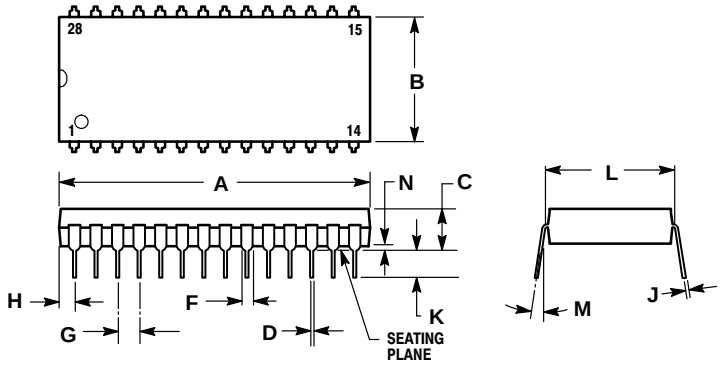
DIP–18
CASE 707–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.02

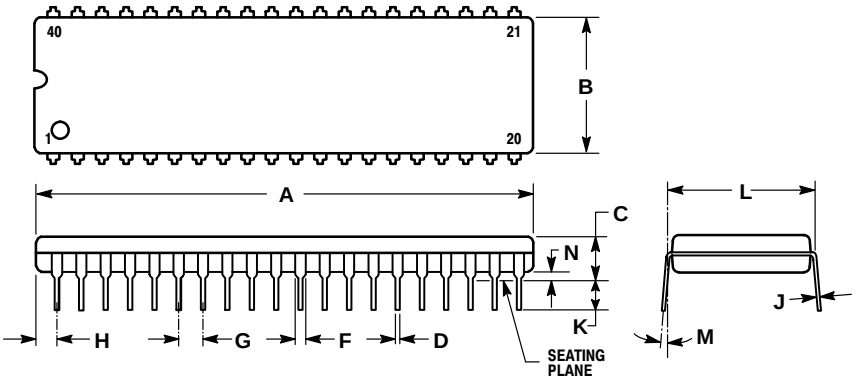
DIP–28 WIDE BODY
CASE 710–02
ISSUE B



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.085	1.65	2.16
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.02

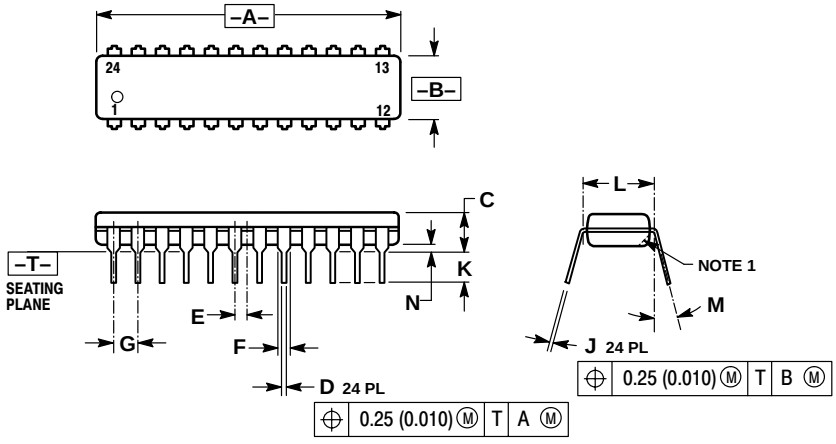
DIP–40 WIDE BODY
CASE 711–03
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

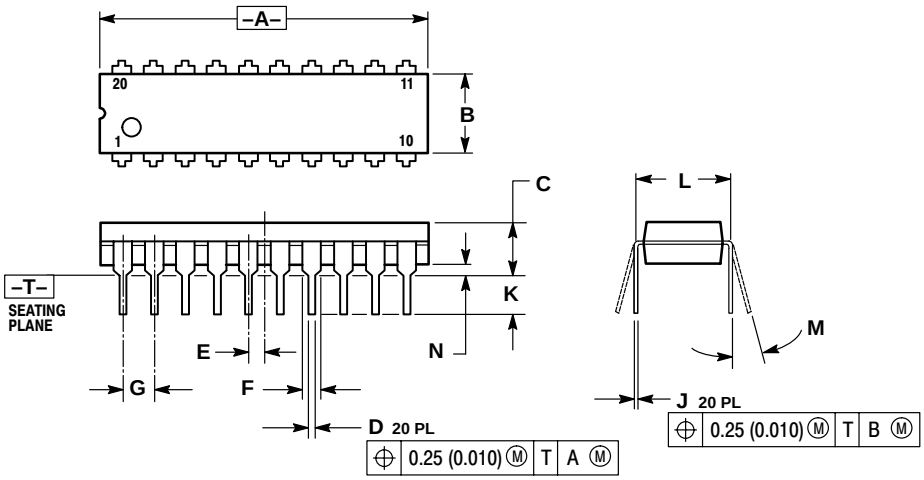
DIP–24
CASE 724–03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

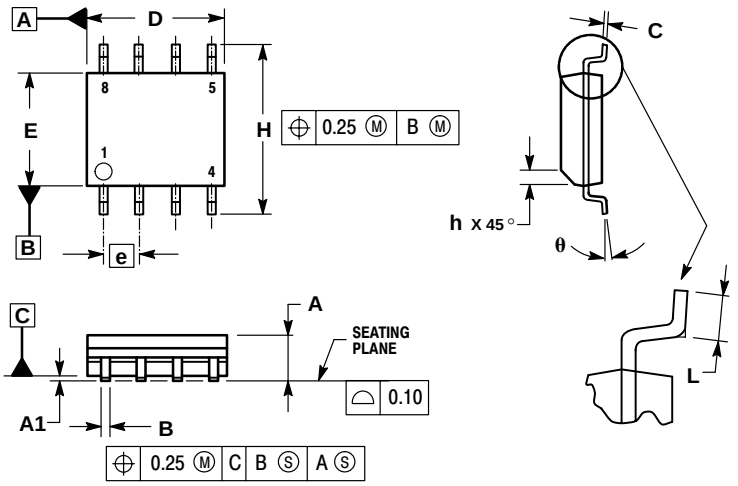
DIP–20
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO–8
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N–SOURCE
2. N–GATE
3. P–SOURCE
4. P–GATE
5. P–DRAIN
6. P–DRAIN
7. N–DRAIN
8. N–DRAIN

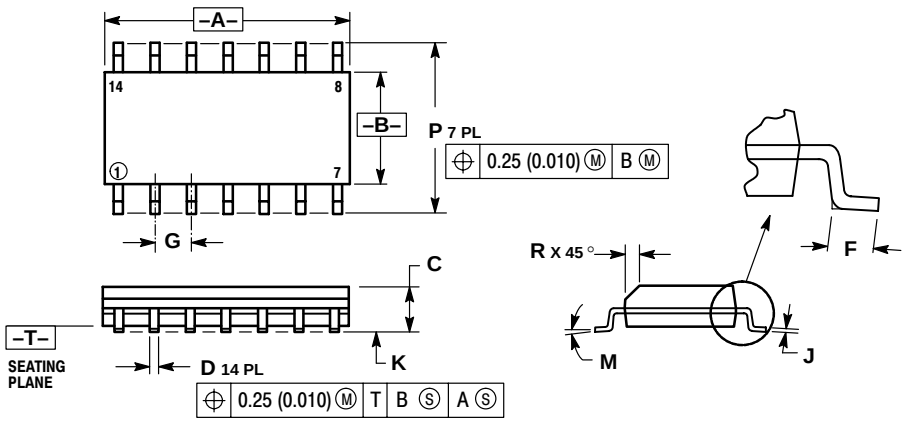
STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

SO–14
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

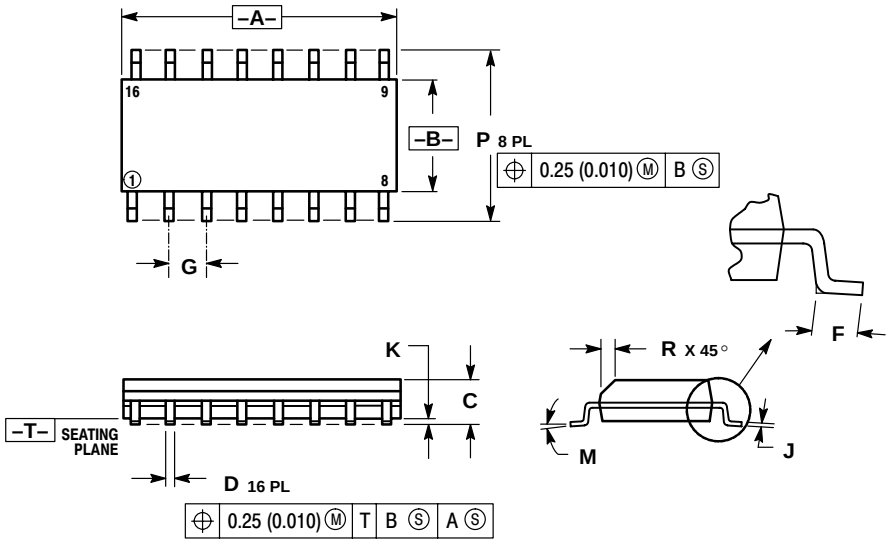
STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

SO–16
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

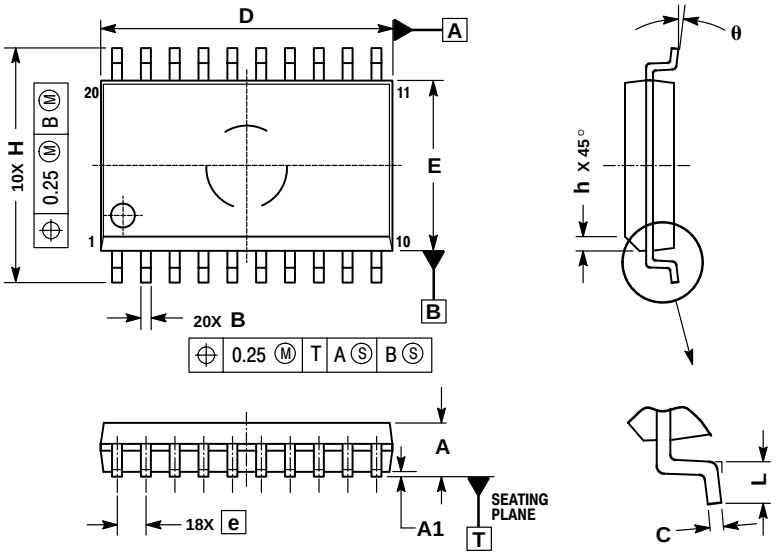
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

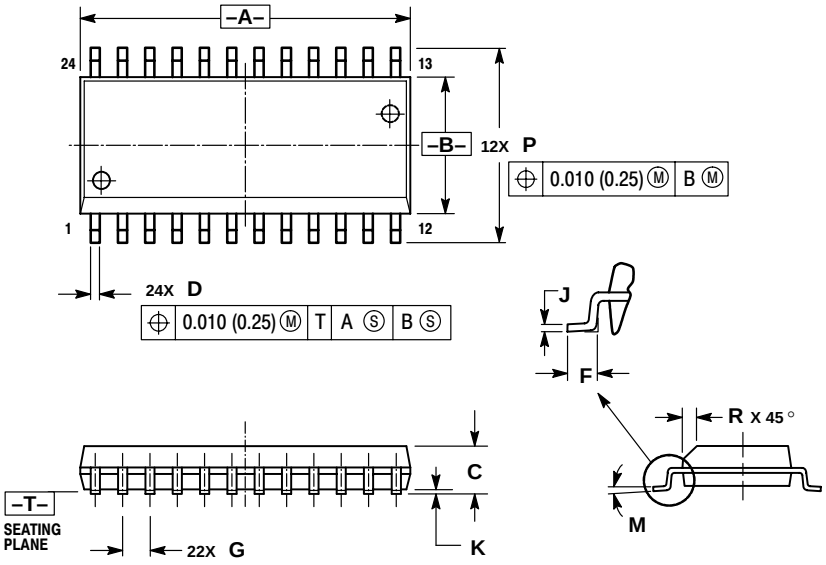
SO–20L
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

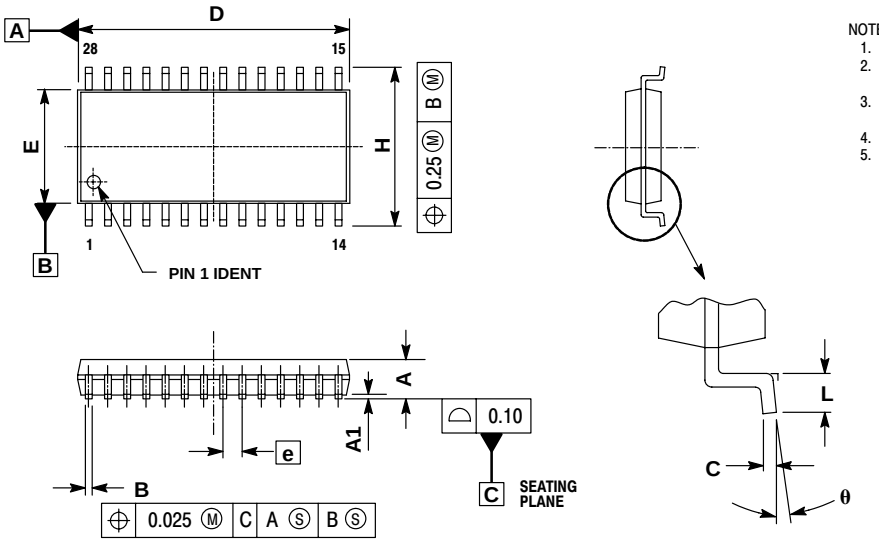
SO–24L
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

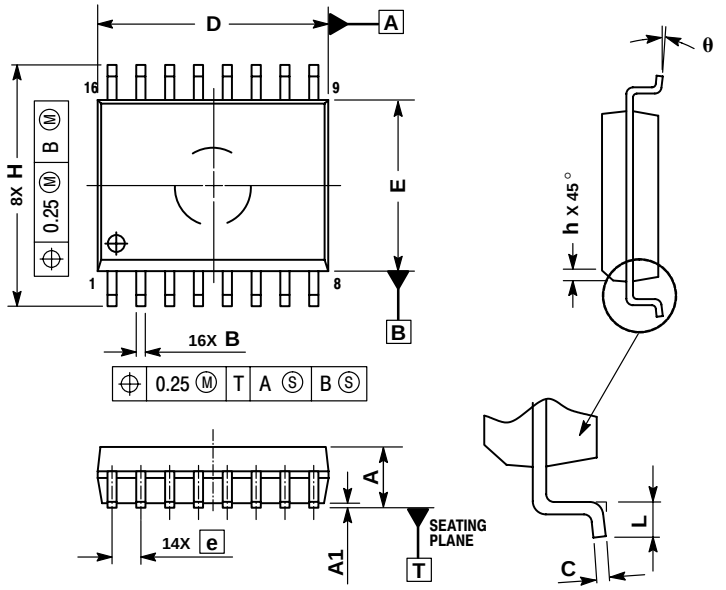
SO–28L
CASE 751F–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0°	8°

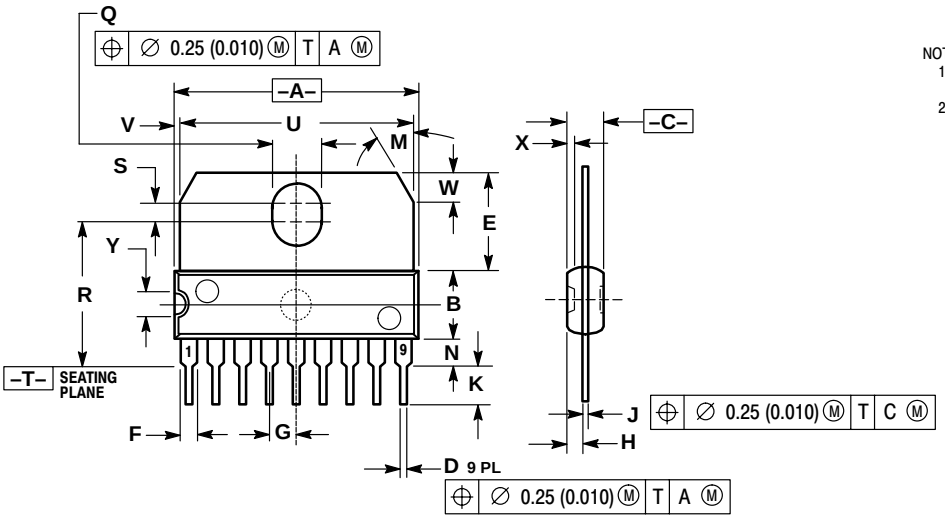
SO–16L
CASE 751G–03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

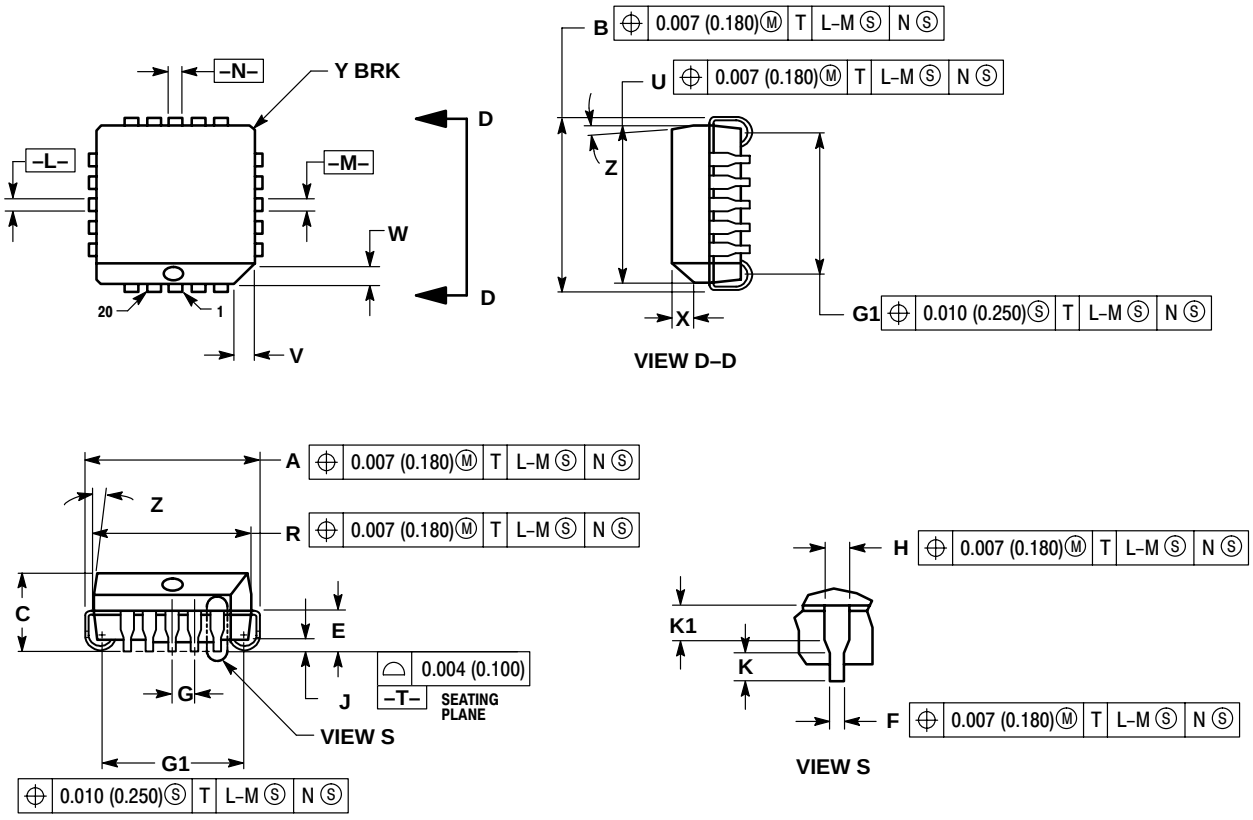
SIP–9
CASE 762–01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.40	23.00	0.873	0.897
B	6.40	6.60	0.252	0.260
C	3.45	3.65	0.135	1.143
D	0.40	0.55	0.015	0.021
E	9.35	9.60	0.368	0.377
F	1.40	1.60	0.055	0.062
G	2.54 BSC		0.100 BSC	
H	1.51	1.71	0.059	0.067
J	0.360	0.400	0.014	0.015
K	3.95	4.20	0.155	0.165
M	30 ° BSC		30 ° BSC	
N	2.50	2.70	0.099	0.106
Q	3.15	3.45	0.124	0.135
R	13.60	13.90	0.535	0.547
S	1.65	1.95	0.064	0.076
U	22.00	22.20	0.866	0.874
V	0.55	0.75	0.021	0.029
W	2.89 BSC		0.113 BSC	
X	0.65	0.75	0.025	0.029
Y	2.70	2.80	0.106	0.110

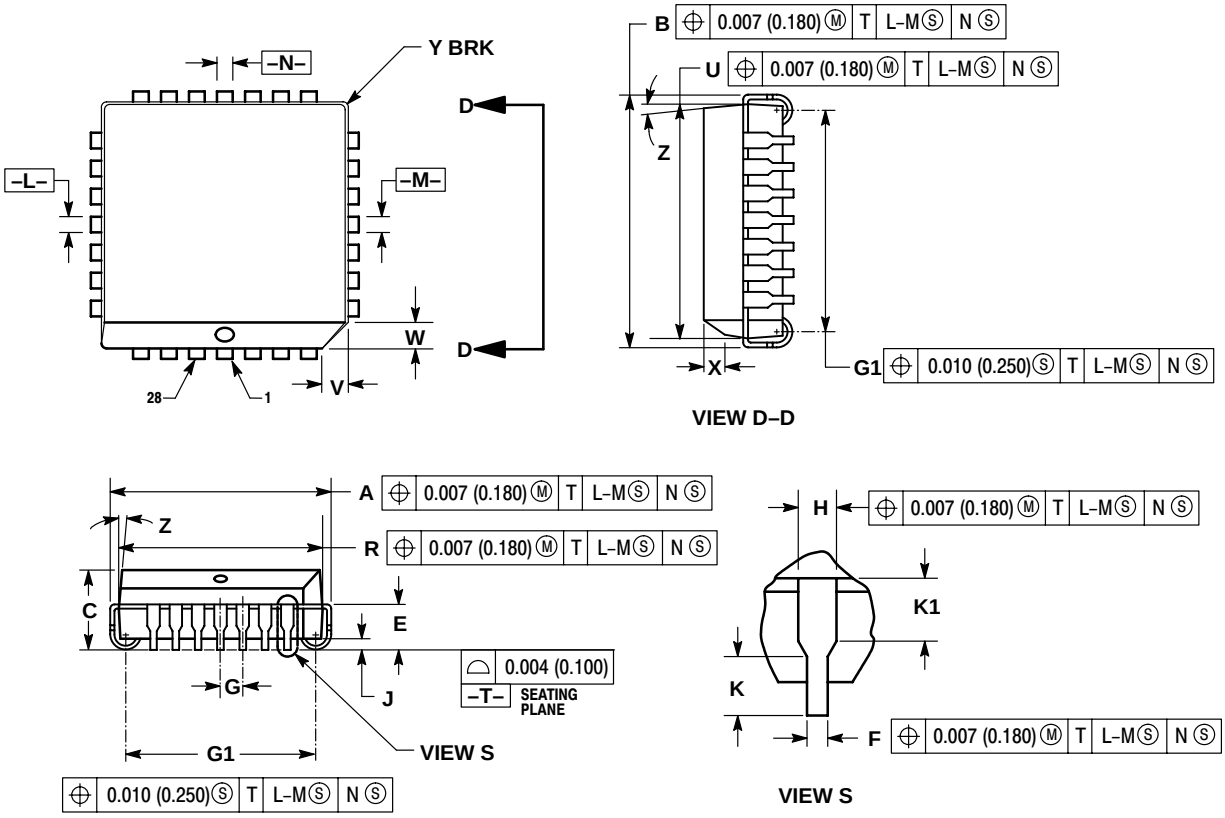
PLCC–20
CASE 775–02
ISSUE C



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

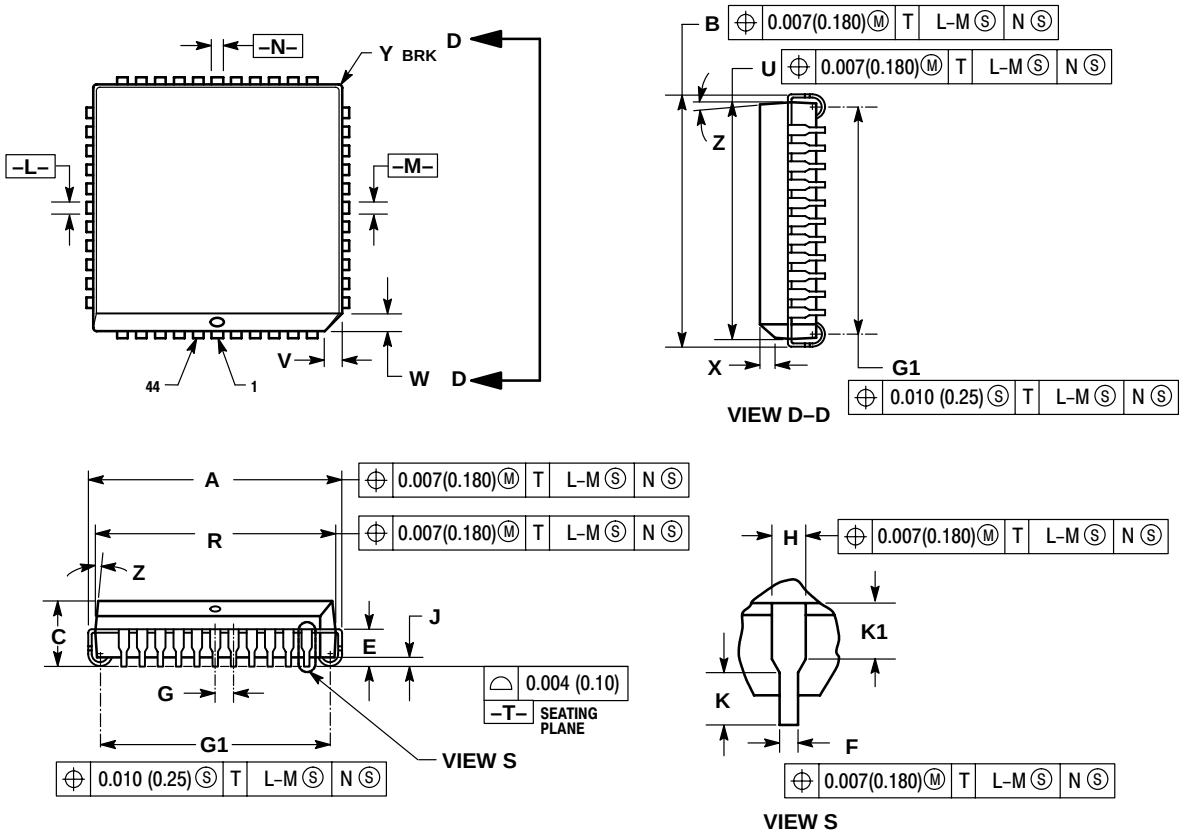
PLCC–28
CASE 776–02
ISSUE D



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

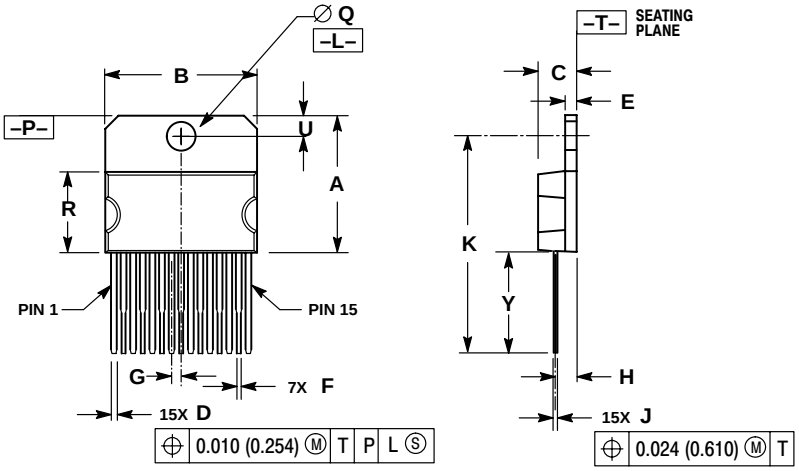
PLCC–44
CASE 777–02
ISSUE C



NOTES:
1. DATUMS –L–, –M–, AND –N– ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	---	1.02	---

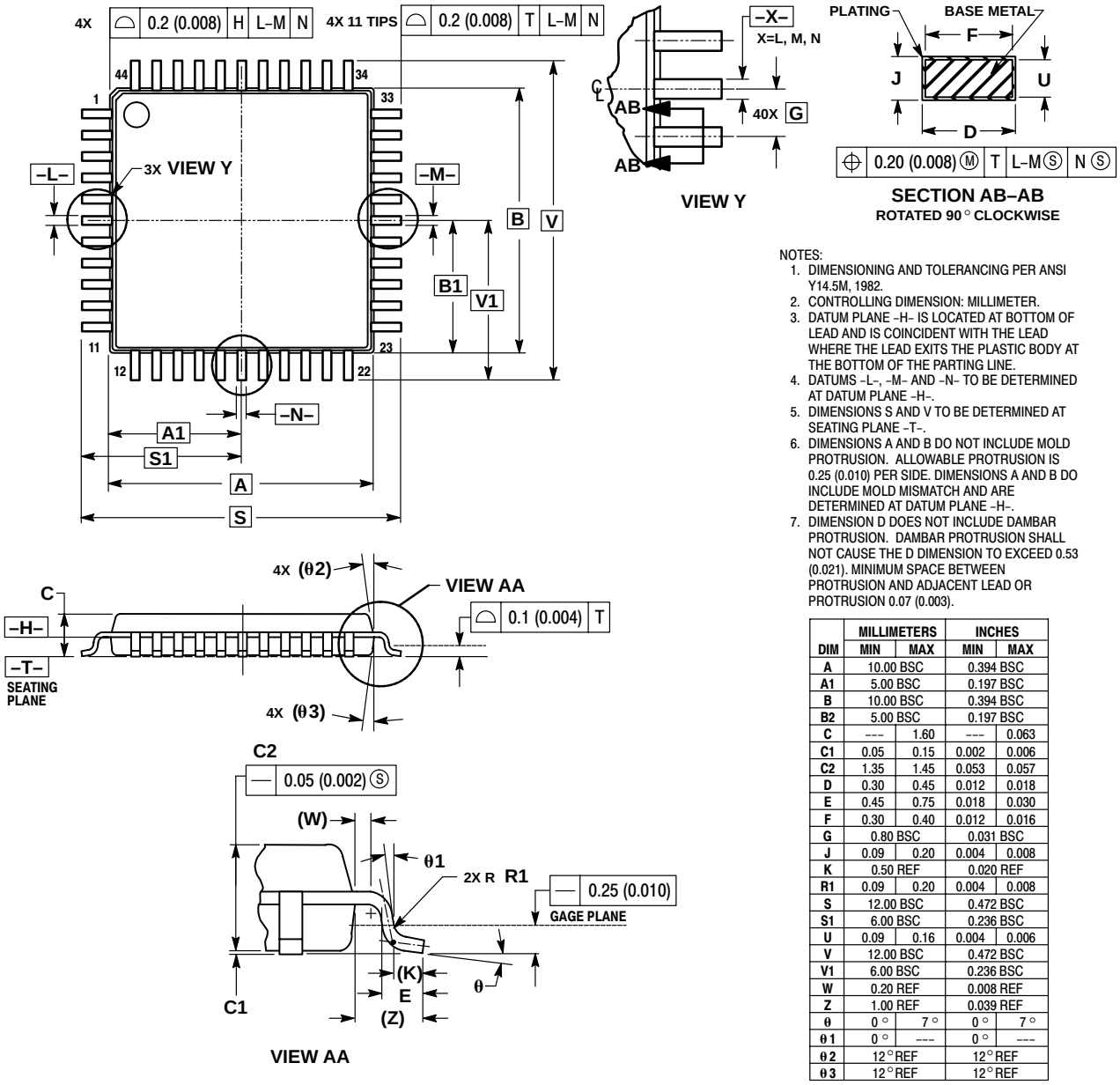
SIP–15
CASE 821D–03
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DELETED
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION. AT MAXIMUM MATERIAL CONDITION.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.681	0.694	17.298	17.627
B	0.784	0.792	19.914	20.116
C	0.173	0.181	4.395	4.597
D	0.024	0.031	0.610	0.787
E	0.058	0.062	1.473	1.574
F	0.016	0.023	0.407	0.584
G	0.050 BSC		1.270 BSC	
H	0.110 BSC		2.794 BSC	
J	0.018	0.024	0.458	0.609
K	1.078	1.086	27.382	27.584
Q	0.148	0.151	3.760	3.835
R	0.416	0.426	10.567	10.820
U	0.110 BSC		2.794 BSC	
Y	0.503 REF		12.776 REF	

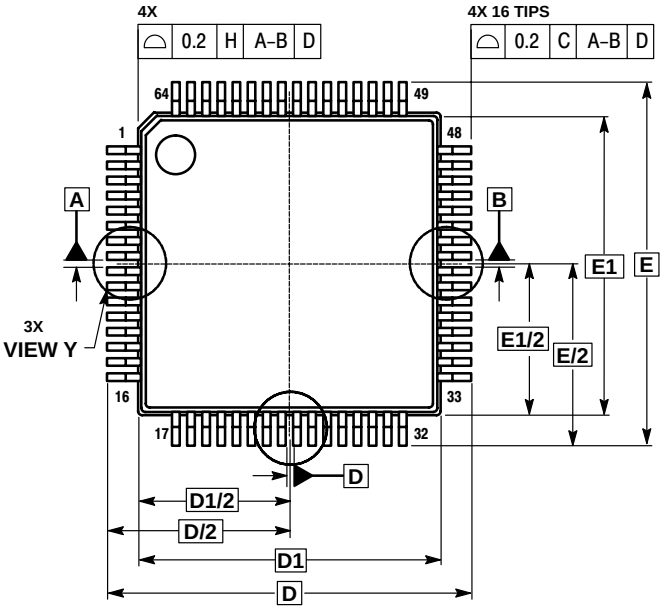
TQFP–44
CASE 824D–02
ISSUE A

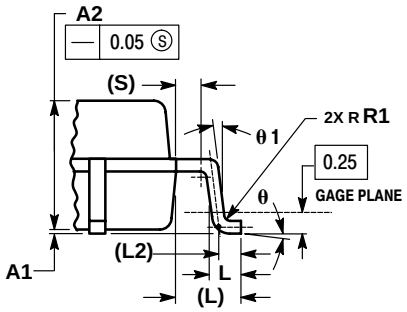


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.53 (0.021). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

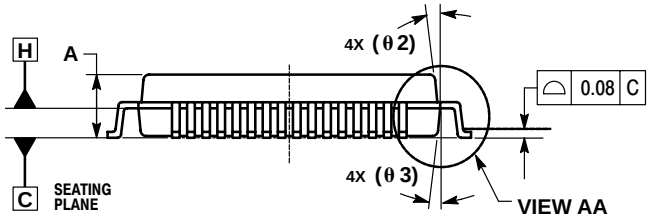
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B2	5.00 BSC		0.197 BSC	
C	---	1.60	---	0.063
C1	0.05	0.15	0.002	0.006
C2	1.35	1.45	0.053	0.057
D	0.30	0.45	0.012	0.018
E	0.45	0.75	0.018	0.030
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
J	0.09	0.20	0.004	0.008
K	0.50 REF		0.020 REF	
R1	0.09	0.20	0.004	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0 °	7 °	0 °	7 °
θ1	0 °	---	0 °	---
θ2	12° REF		12° REF	
θ3	12° REF		12° REF	

QFP–64
CASE 840F–02
ISSUE B



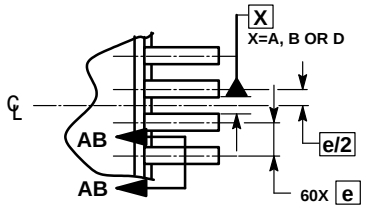


VIEW AA

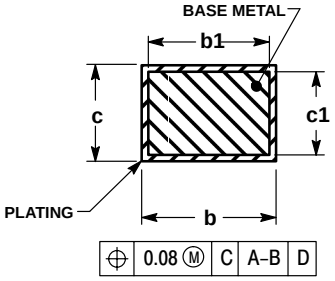


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE DATUM H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE DATUM C.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM C.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE.
7. DIMENSION bDOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
e	0.50 BSC	
E	12.00 BSC	
E1	10.00 BSC	
L	0.45	0.75
L1	1.00 REF	
L2	0.50 REF	
R1	0.10	0.20
S	0.20 REF	
θ	0 °	7 °
θ 1	0 °	---
θ 2	12° REF	
θ 3	12° REF	

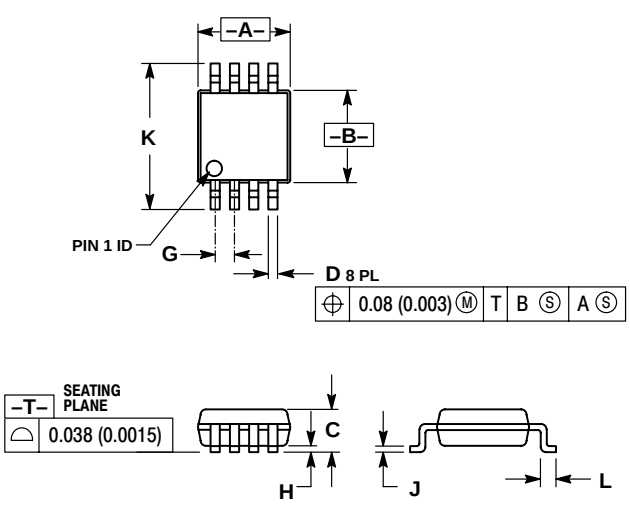


VIEW Y



SECTION AB–AB
ROTATED 90 ° CLOCKWISE

Micro8™
CASE 846A–02
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

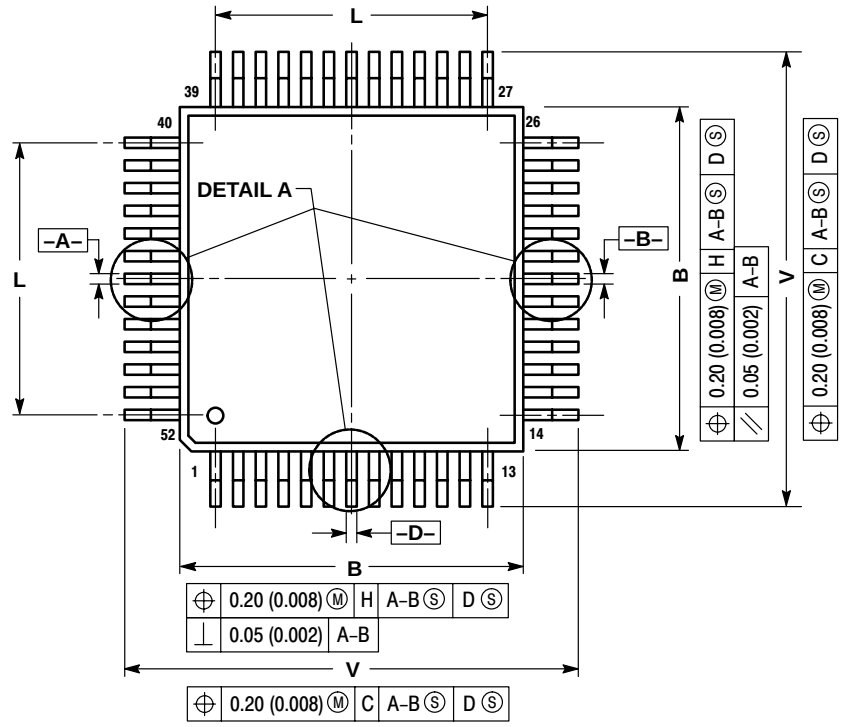
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

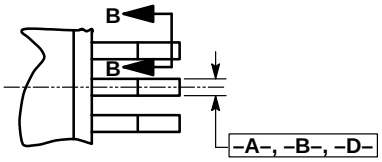
STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

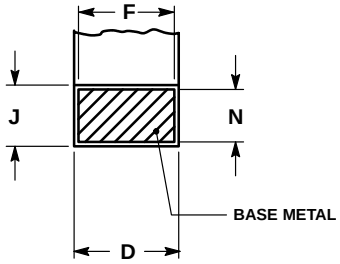
STYLE 3:
PIN 1. N–SOURCE
2. N–GATE
3. P–SOURCE
4. P–GATE
5. P–DRAIN
6. P–DRAIN
7. N–DRAIN
8. N–DRAIN

TQFP–52
CASE 848B–04
ISSUE C

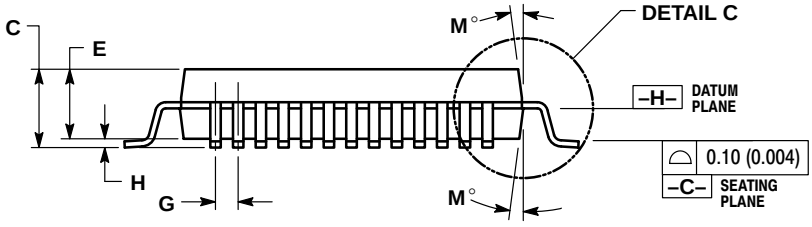


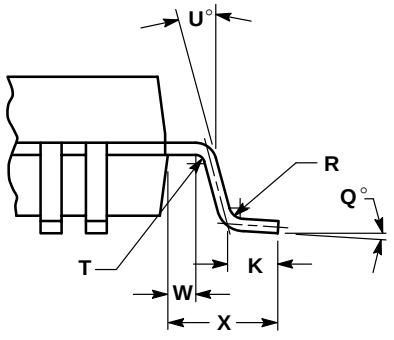


DETAIL A



SECTION B–B



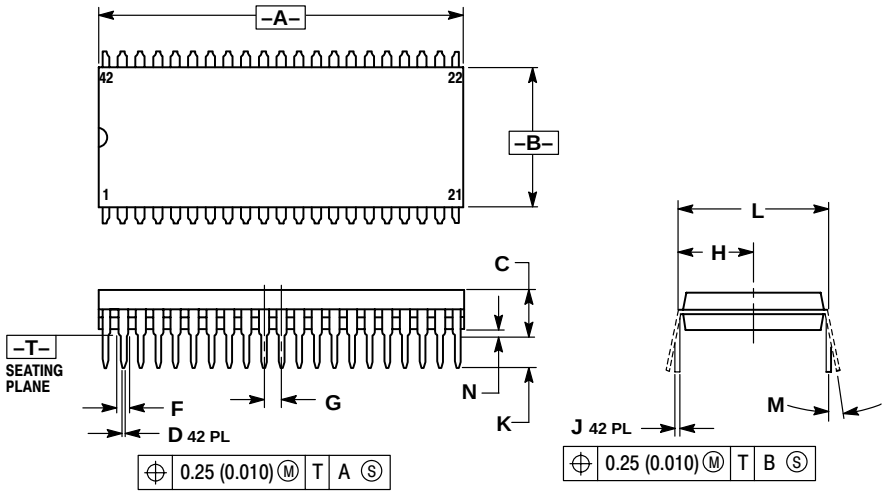


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	---	0.25	---	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	---	0.005	---
U	0°	---	0°	---
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

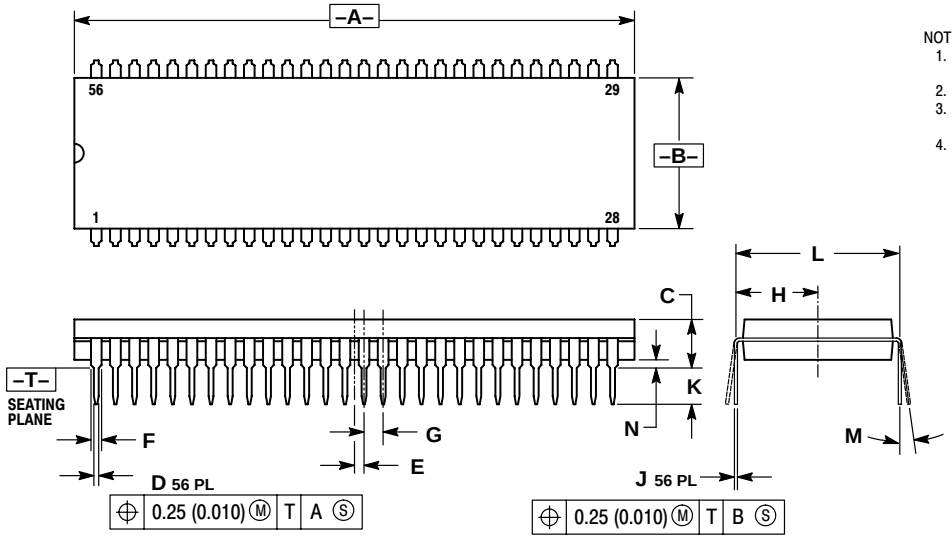
DIP–42 WIDE BODY
CASE 858–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.02

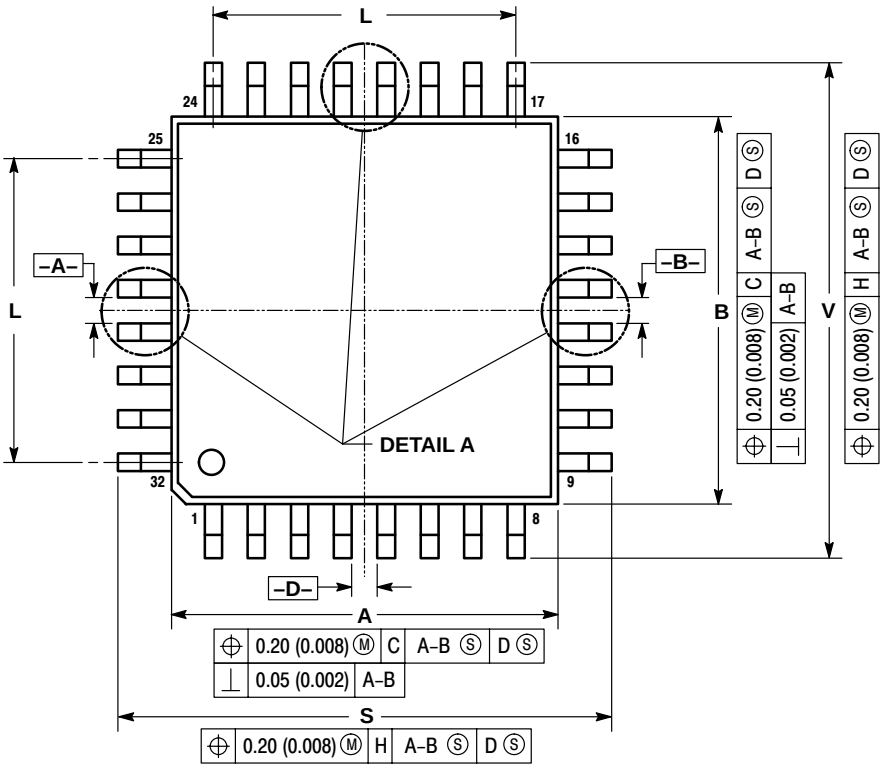
DIP–56 WIDE BODY
CASE 859–01
ISSUE O

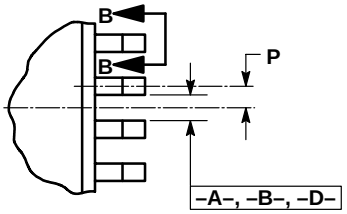


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010)

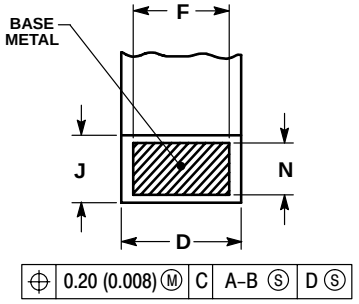
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.035	2.065	51.69	52.45
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
E	0.035 BSC		0.89 BSC	
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.02

TQFP–32
CASE 873–01
ISSUE A

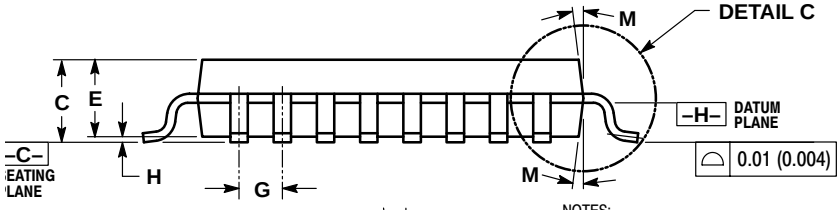


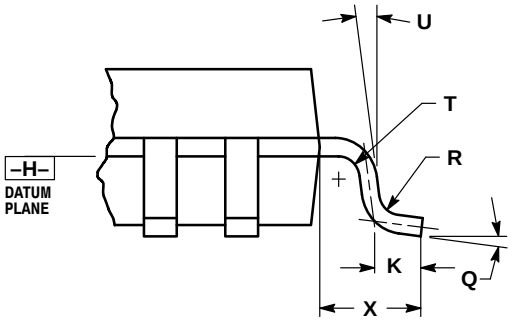


DETAIL A



SECTION B–B
VIEW ROTATED 90 ° CLOCKWISE



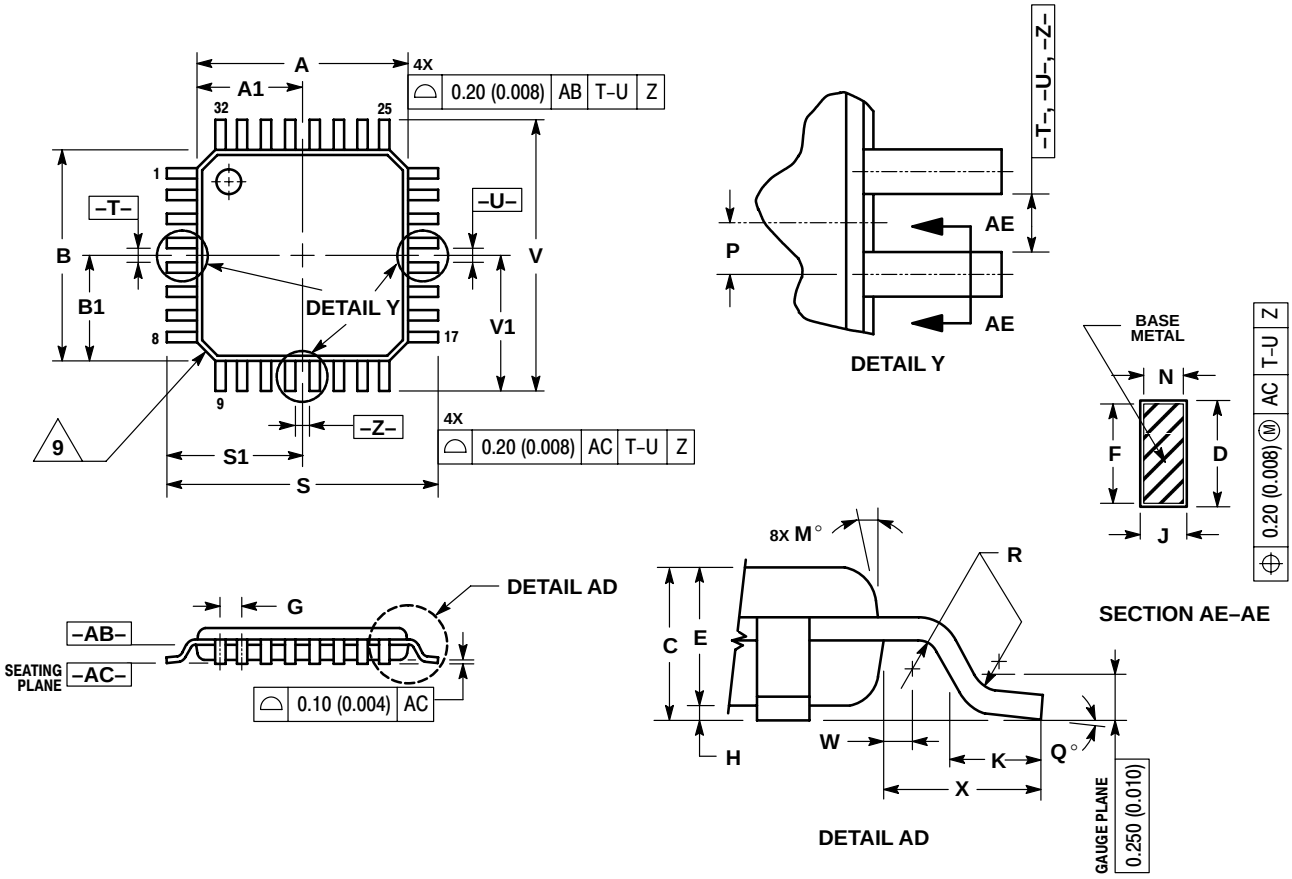


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	---	0.010	---
G	0.80 BSC		0.031 BSC	
H	---	0.20	---	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6 °	8 °	6 °	8 °
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5 °	10°	5 °	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5 °	11°	5 °	11°
V	8.85	9.15	0.348	0.360
X	1.00 REF		0.039 REF	

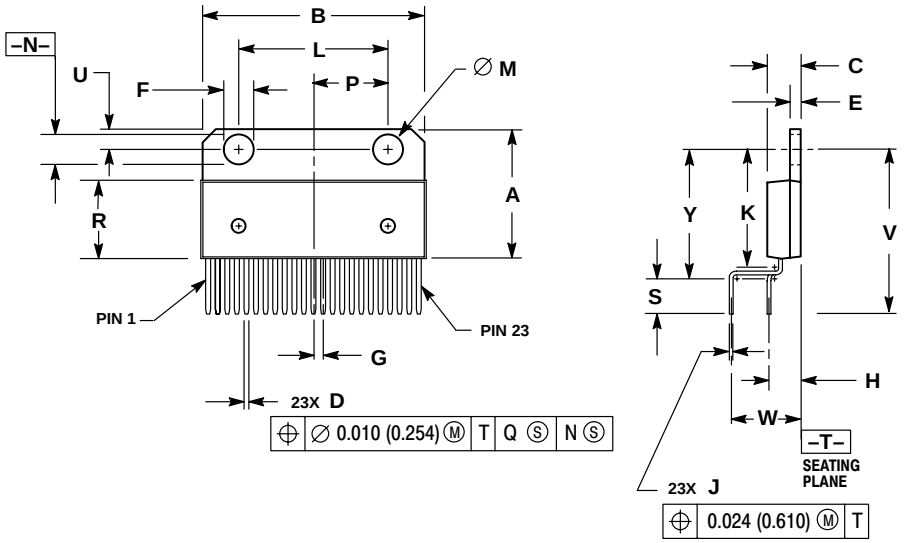
LQFP–32
CASE 873A–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

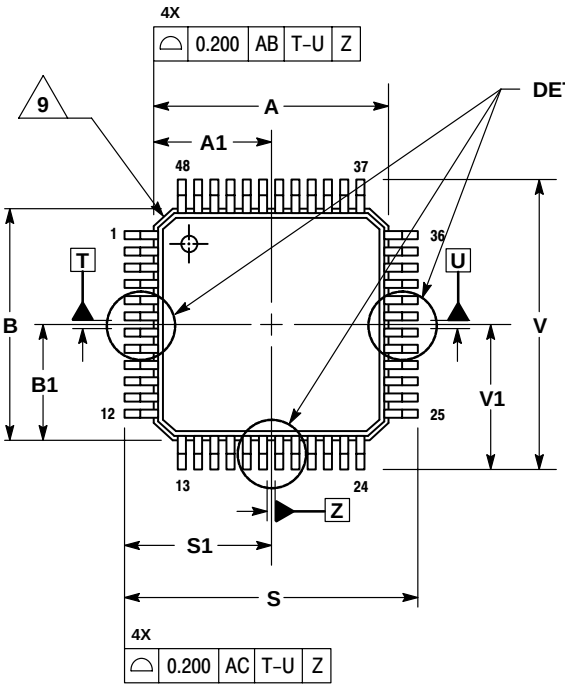
SZIP–23
CASE 894–03
ISSUE B

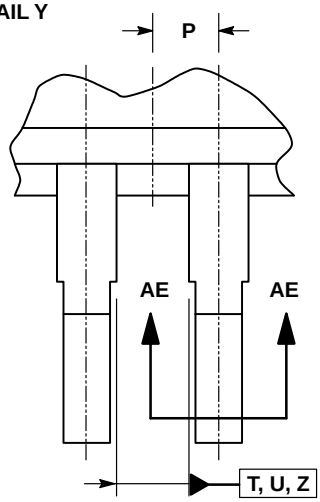


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.684	0.694	17.374	17.627
B	1.183	1.193	30.048	30.302
C	0.175	0.179	4.445	4.547
D	0.026	0.031	0.660	0.787
E	0.058	0.062	1.473	1.574
F	0.165	0.175	4.191	4.445
G	0.050 BSC		1.270 BSC	
H	0.169 BSC		4.293 BSC	
J	0.014	0.020	0.356	0.508
K	0.625	0.639	15.875	16.231
L	0.770	0.790	19.558	20.066
M	0.148	0.152	3.760	3.861
N	0.148	0.152	3.760	3.861
P	0.390 BSC		9.906 BSC	
R	0.416	0.424	10.566	10.770
S	0.157	0.167	3.988	4.242
U	0.105	0.115	2.667	2.921
V	0.868 REF		22.047 REF	
W	0.200 BSC		5.080 BSC	
Y	0.700	0.710	17.780	18.034

TQFP–49
CASE 932–02
ISSUE E

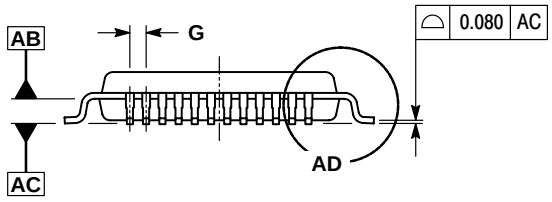


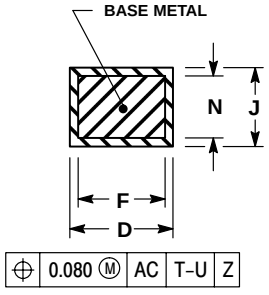


DETAIL Y

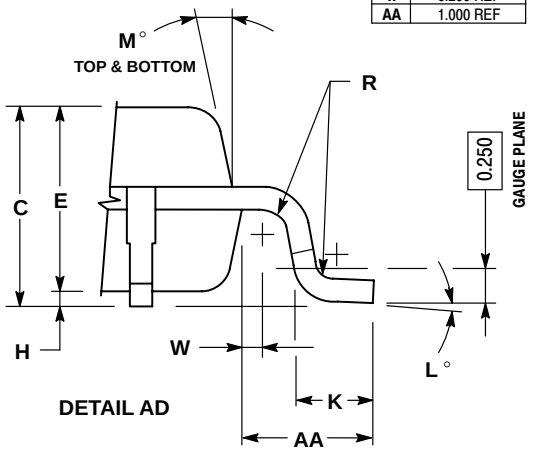
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	1°	5°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	



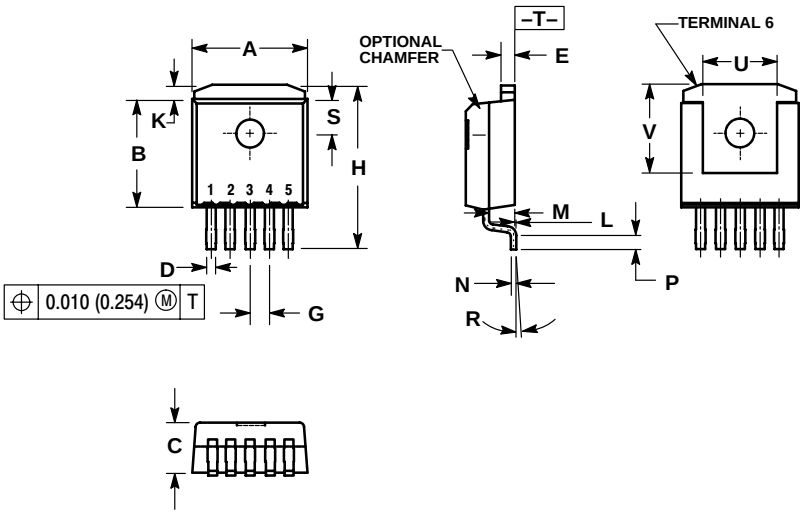


SECTION AE–AE



DETAIL AD

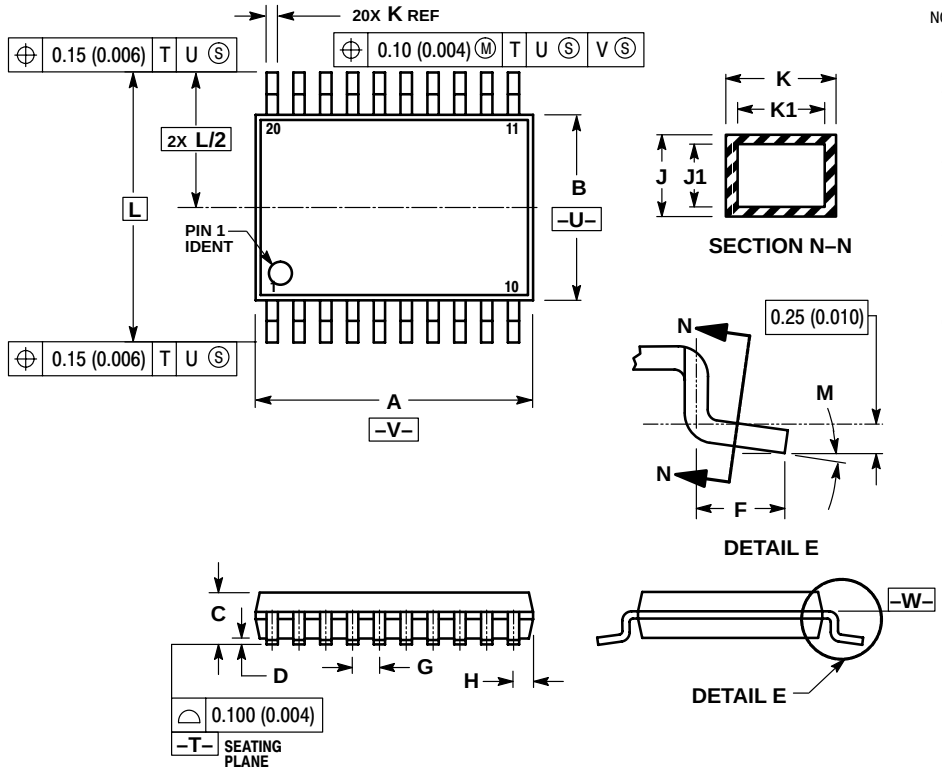
D²PAK 5–PIN
CASE 936A–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5 ° REF		5 ° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

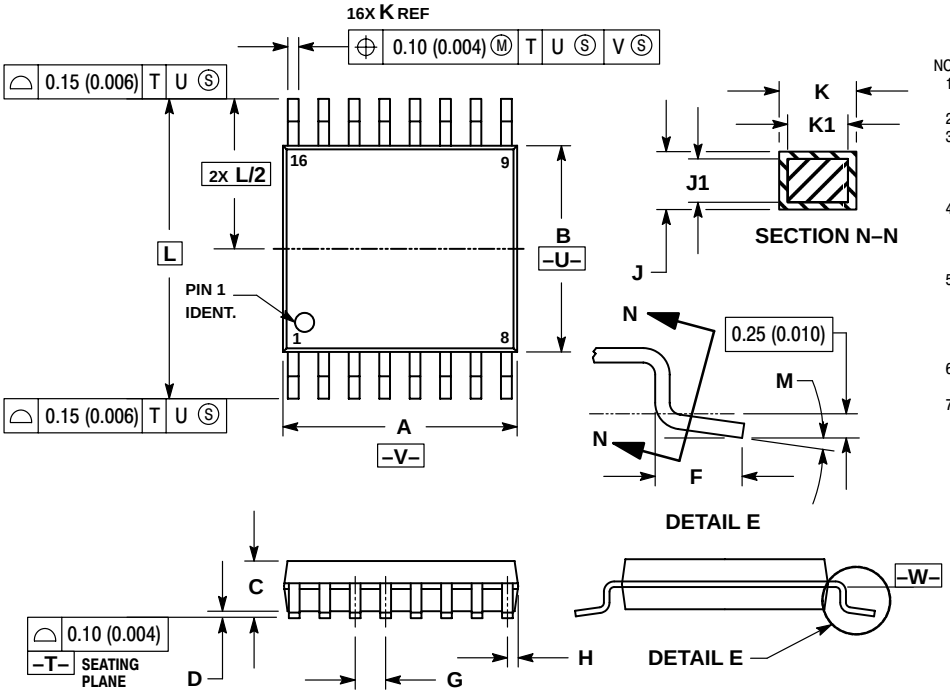
TSSOP–20
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

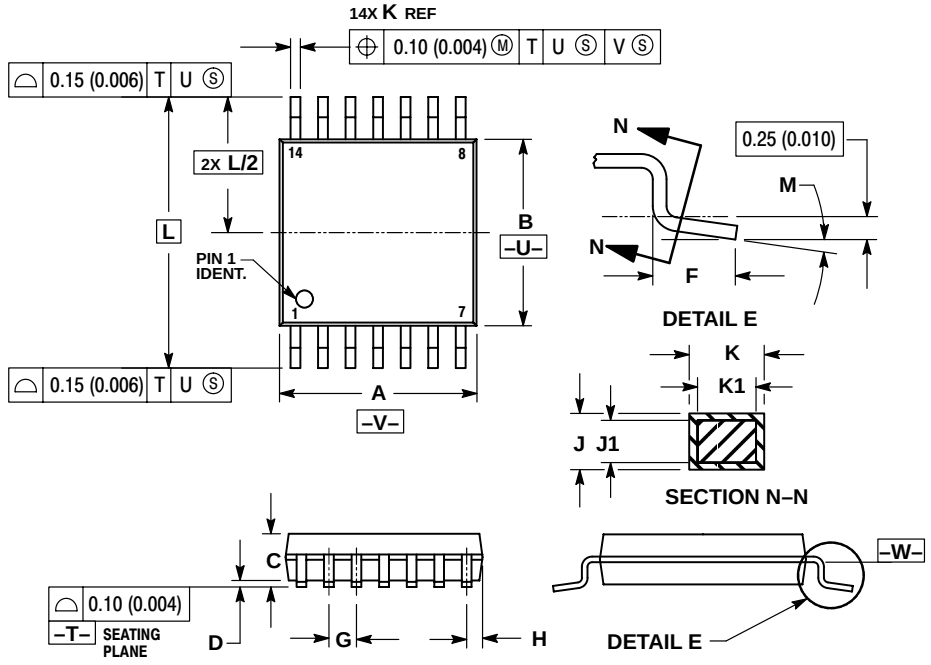
TSSOP–16
CASE 948F–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

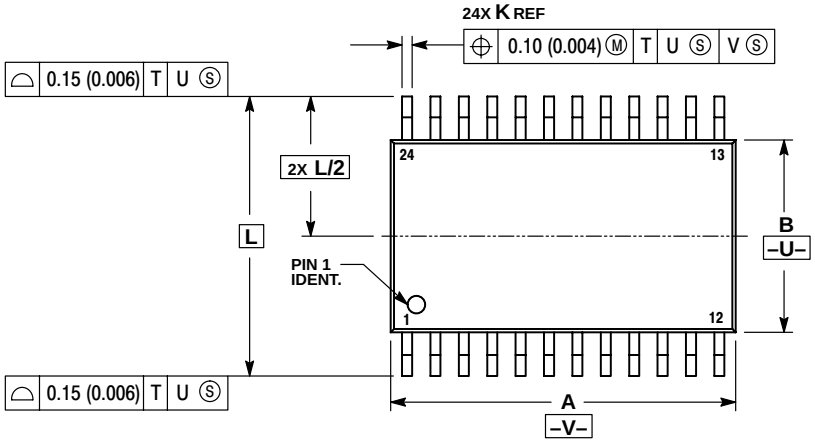
TSSOP–14
CASE 948G–01
ISSUE O

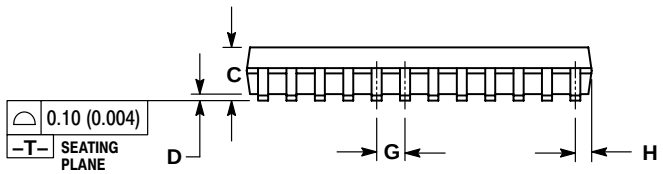


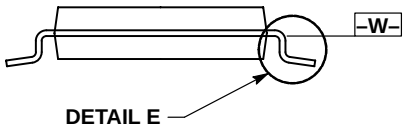
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

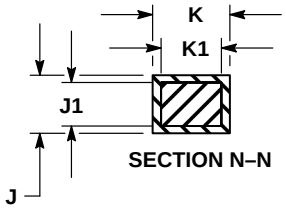
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

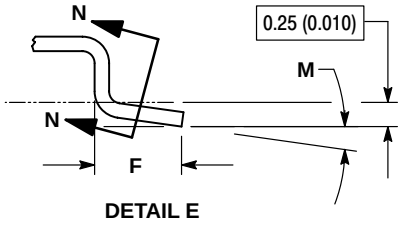
TSSOP–24
CASE 948H–01
ISSUE O







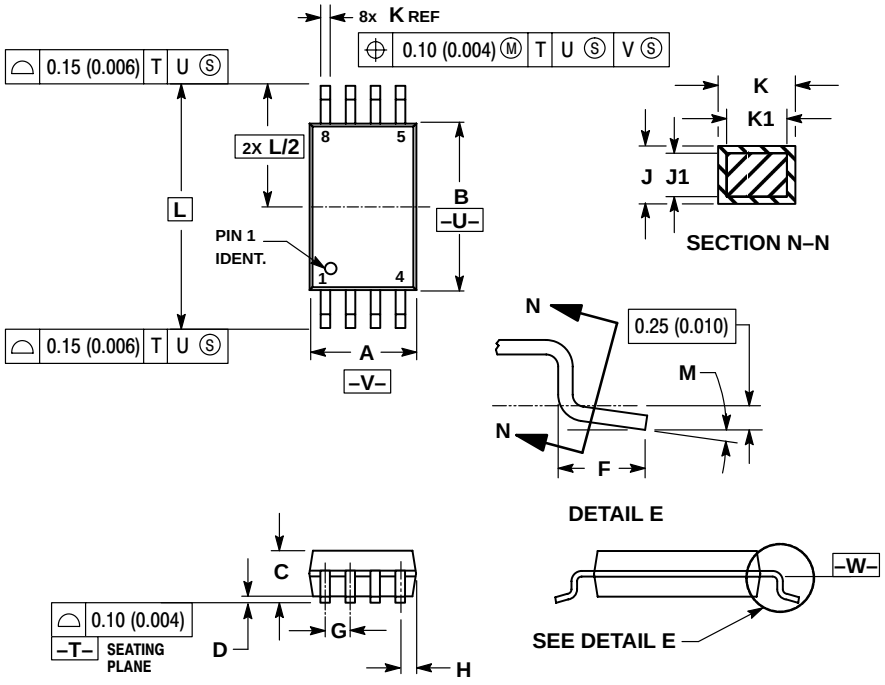




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
   1. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

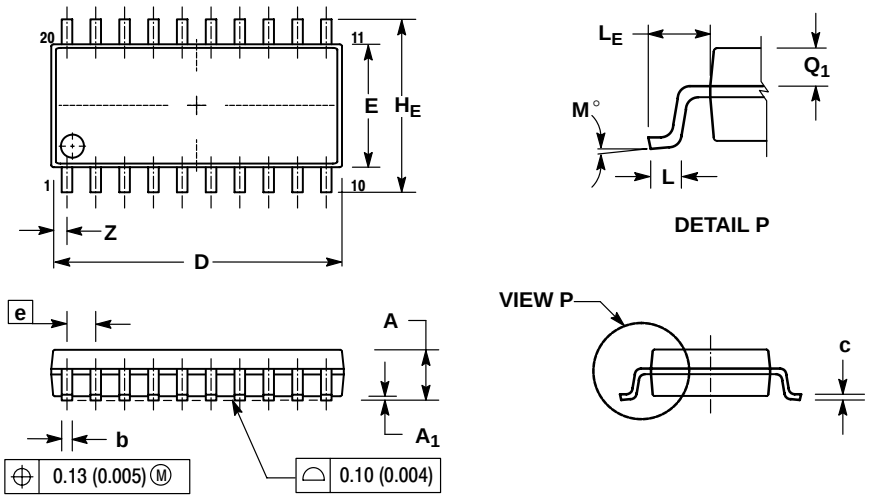
TSSOP–8
CASE 948J–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

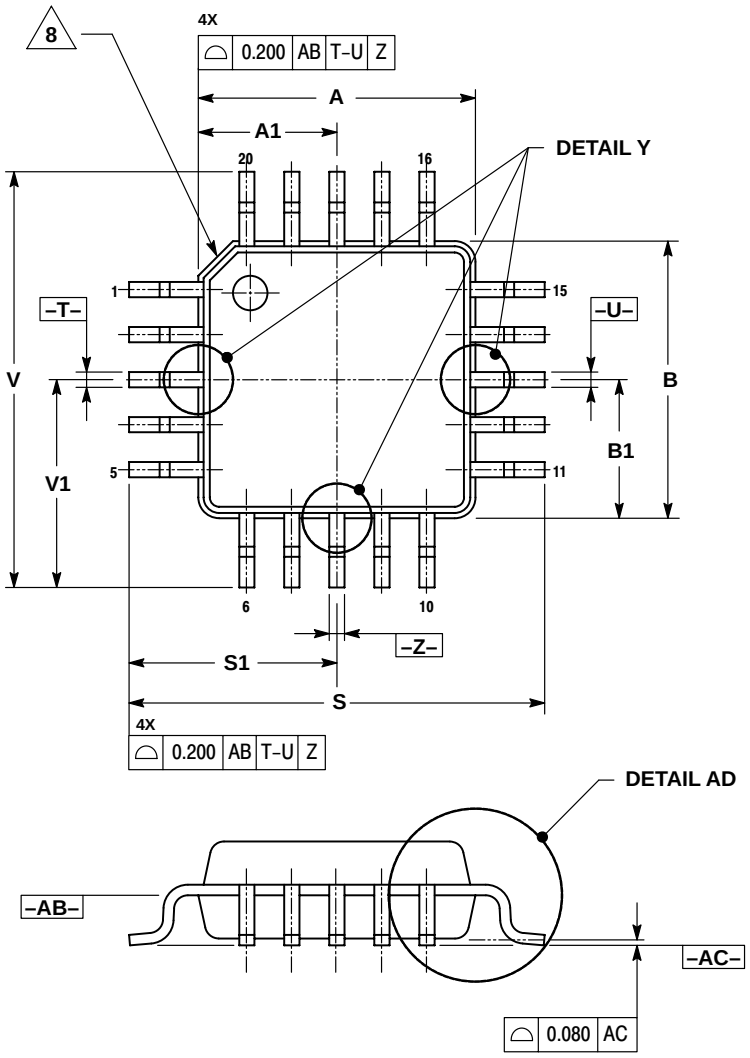
EIAJ–20
CASE 967–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

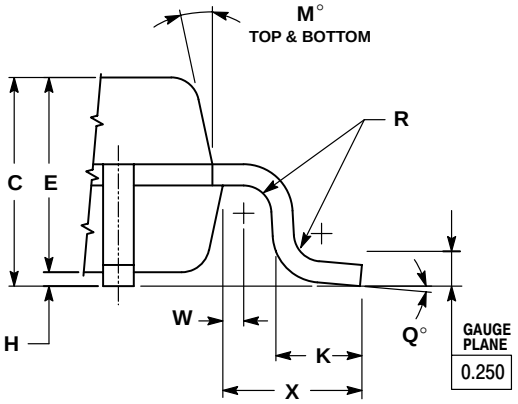
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

TQFP–20
CASE 976–02
ISSUE A

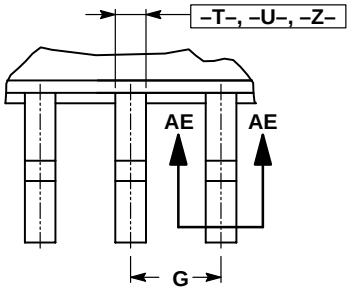


NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. A AND B ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM D DIMENSION BY MORE THAN 0.08 mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

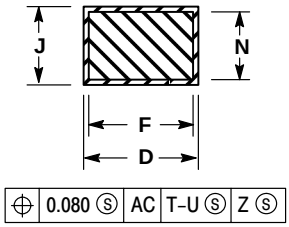
	MILLIMETERS	
DIM	MIN	MAX
A	4.000 BSC	
A1	2.000 BSC	
B	4.000 BSC	
B1	2.000 BSC	
C	1.400	1.600
D	0.220	0.380
E	1.350	1.450
F	0.220	0.330
G	0.650 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
Q	2°	7°
R	0.080	0.200
S	6.000 BSC	
S1	3.000 BSC	
V	6.000 BSC	
V1	3.000 BSC	
W	0.200 REF	
X	1.000 REF	



DETAIL AD

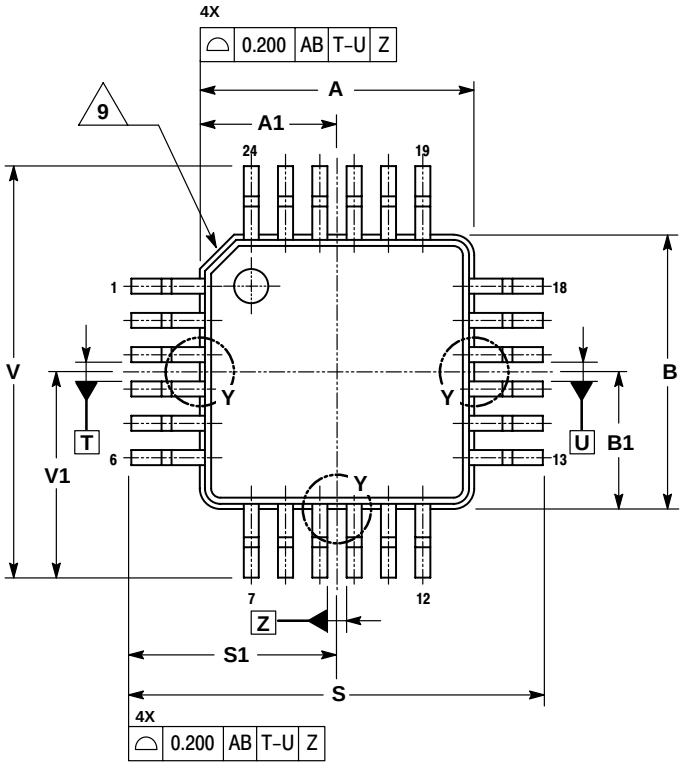


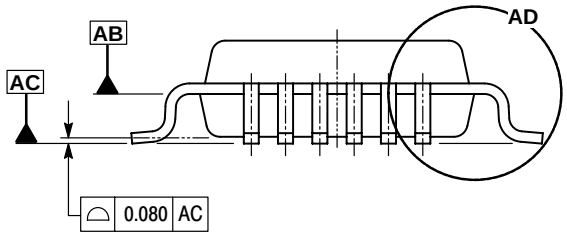
DETAIL Y



SECTION AE–AE

TQFP–24
CASE 977–02
ISSUE A

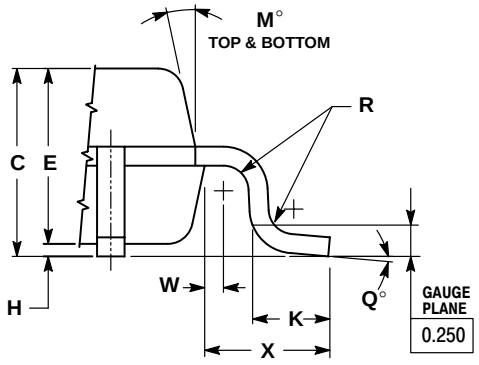




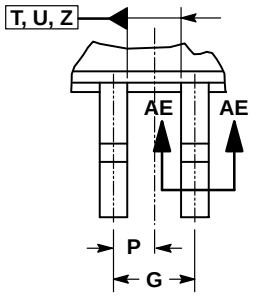
NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.

9 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

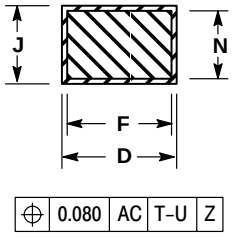
	MILLIMETERS	
DIM	MIN	MAX
A	4.000 BSC	
A1	2.000 BSC	
B	4.000 BSC	
B1	2.000 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
Q	0°	7°
R	0.150	0.250
S	6.000 BSC	
S1	3.000 BSC	
V	6.000 BSC	
V1	3.000 BSC	
W	0.200 REF	
X	1.000 REF	



DETAIL AD

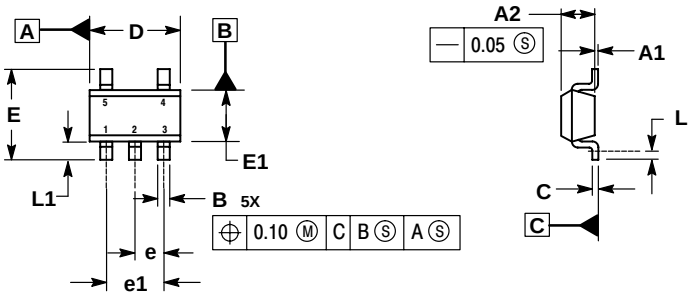


DETAIL Y



SECTION AE–AE

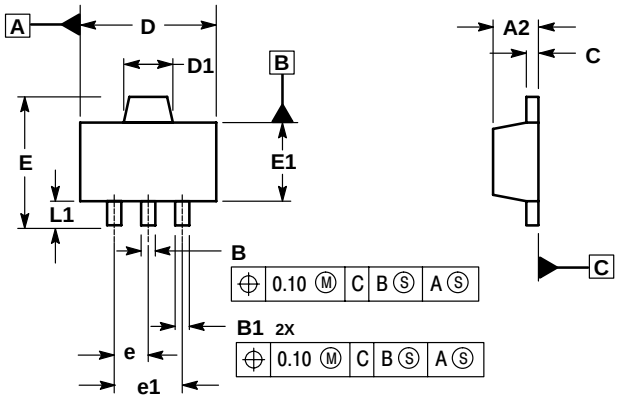
SOT−23 FIVE LEAD
CASE 1212−01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A1	0.00	0.10
A2	1.00	1.30
B	0.30	0.50
C	0.10	0.25
D	2.80	3.00
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
e1	1.90 BSC	
L	0.20	---
L1	0.45	0.75

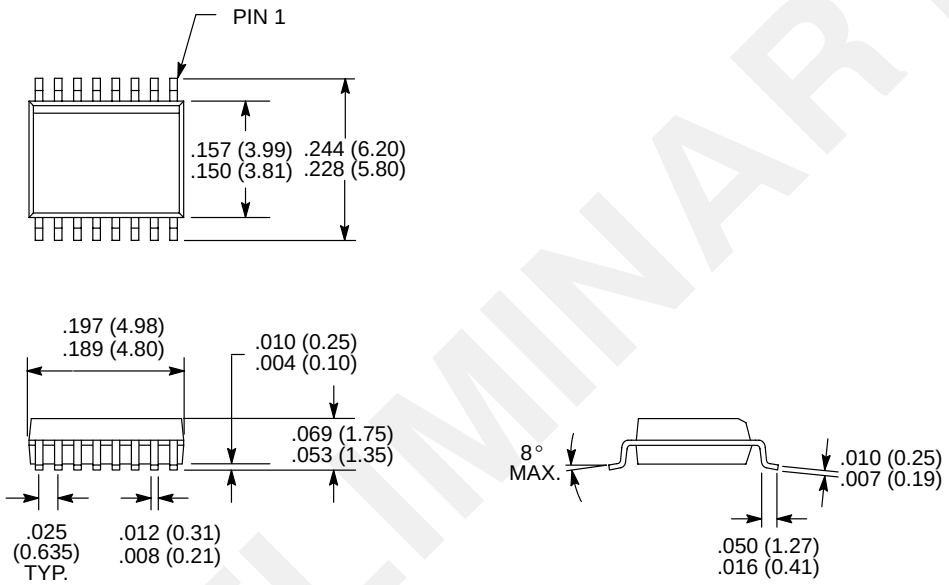
SOT−89
CASE 1213−01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A2	1.40	1.60
B	0.37	0.57
B1	0.32	0.52
C	0.30	0.50
D	4.40	4.60
D1	1.50	1.70
E	---	4.25
E1	2.40	2.60
e	1.50 BSC	
e1	3.00 BSC	
L1	0.80	---

QSOP−16
CASE TO BE DETERMINED
ISSUE X



Dimensions: inches (mm)

Section 3

Thermal Considerations

Basic Semiconductor Thermal Measurement

Gary E. Dashney
ON Semiconductor
Phoenix, Arizona

INTRODUCTION

This paper will provide the reader with a basic understanding of power semiconductor thermal parameters, how they are measured, and how they are used. With this knowledge, the reader will be able to better describe power semiconductors and answer many common questions relating to their power handling capability.

This paper will cover the following key topics.

- Understanding basic semiconductor thermal parameters
- Semiconductor thermal test equipment
- Thermal parameter test procedures
- Using thermal parameters to solve often asked thermal questions

Understanding Basic Semiconductor Thermal Parameters

Heat flows from a higher to a lower temperature region. The quantity that resists or impedes this flow of heat energy is called thermal resistance or thermal impedance.

When the quantity of heat being generated by a device is equal to the quantity of heat being removed from it, a steady state condition is achieved.

To describe the thermal capability of a device, several key parameters and terms are used. They describe the steady state thermal capability of a power semiconductor device.

Key Parameters, Terms, and Definitions

T_J = *junction* temperature

T_C = *case* temperature

T_A = *ambient* temperature

TSP = **T**emperature **S**ensitive **P**arameter

T_R = *reference* temperature (i.e., *case* or *ambient*)

R_{thjr} = junction–to–*reference* thermal resistance

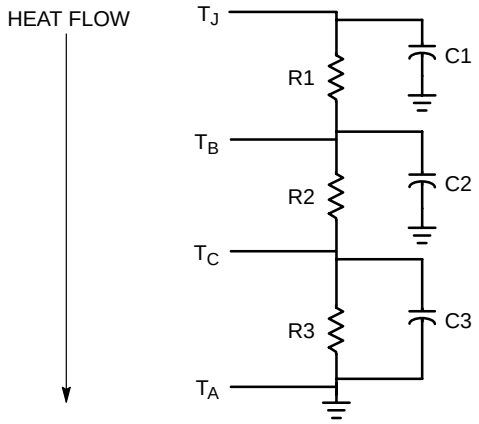
R_{thjc} = junction–to–*case* thermal resistance

R_{thja} = junction–to–*ambient* thermal resistance

$R_{thjr(t)}$ = junction–to–*reference* transient thermal resistance

P_D = power dissipation

The thermal behavior of a device can be described, for practical purposes, by an electrical equivalent circuit. This circuit consists of a resistor–capacitor network as shown.



Heat generated in a device's junction flows from a higher temperature region through each resistor–capacitor pair to a lower temperature region.

Figure 1. Thermal Electrical Equivalent Circuit

Resistors R1, R2, and R3 are all analogous to individual thermal resistance, or quantities that impede heat flow. Resistor R1 is the thermal resistance from the device's junction to its die–bond. Resistor R2 is the thermal resistance from the die–bond to the device's case. Resistor R3 is the thermal resistance from the device's case to ambient. The thermal resistance from the junction to some reference point is equal to the sum of the individual resistors between the two points. For instance, the thermal resistance R_{thjc} from junction–to–case is equal to the sum of resistors R1 and R2. The thermal resistance R_{thja} from junction–to–ambient, therefore, is equal to the sum of resistors R1, R2 and R3.

The capacitors shown help model the transient thermal response of the circuit. When heat is instantaneously applied and or generated, there is a charging effect that takes place. This response follows an RC time constant determined by

the resistor–capacitor thermal network. Thermal resistance, at a given time, is called transient thermal resistance, $R_{thjr(t)}$.

To further understand transient thermal response, refer to ON Semiconductor Application Note AN569, "Transient Thermal Resistance – General Data And Its Use." [4] A detailed discussion of this will not be included here.

Using the key parameters and terms shown earlier, only a few equations are necessary to solve often asked thermal questions.

$$R_{thjr} = (T_J - T_R) / \text{power} \quad (1)$$

$$P_D = (\text{max. device temp.} - T_R) / R_{thjr} \quad (2)$$

$$T_J = P_D * R_{thjr} + T_R \quad (3)$$

Semiconductor Thermal Test Equipment

The procedure used determines the test equipment needed for measurement. Below you will find the equipment used for both a manual and an automated approach to thermal measurement.

Manual Technique:

Power supply	*(supplies power to the device under test)*
Thermocouple	*(measures T_R)*
Multimeter	*(measures current and voltage)*
Heat exchanger	*(needed to mount device to and remove heat)*
Chiller	*(needed to remove heat from device)*
Test fixture	*(provides power and sampling pulse train)*

Automated Systems Available:

Analysis Tech	*(Phase 6, 7, 8, and 9)*
Sage	*(Star 150)*
TESEC	*(DV240)*

The automated systems shown above each provide different levels of automation. Analysis Tech has the most complete automation and TESEC the least. One nice feature of the Analysis Tech system is that it will output the 3 resistor–capacitor values for the electrical equivalent circuit.

These values are very useful for modeling the thermal effects in computer simulation software such as SPICE. The level of automation you need depends both on your thermal measurement goals and available budget.

The main advantages of an automated approach are;

- Ease of use
- Less operator dependence on measurement
- Consistency
- Accuracy
- System network capability for data transfer

Thermal Parameter Test Procedure

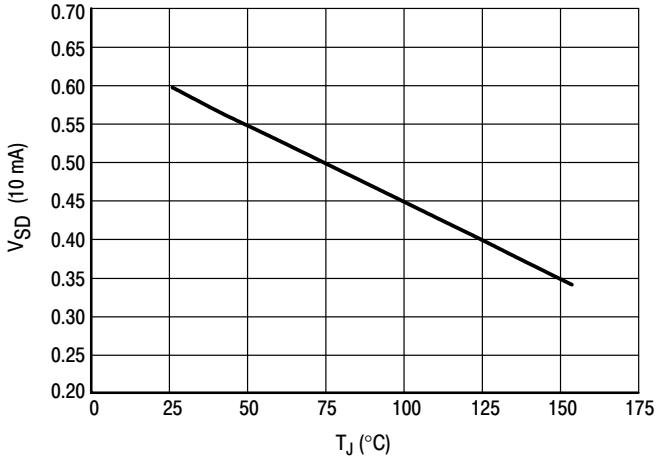
The basic procedure for measuring thermal parameters is as follows.

1. Calibrate the TSP (Temperature Sensitive Parameter).
2. Apply continuous power and TSP sampling pulses.
3. Measure T_J, T_R, and applied test power.
4. Calculate thermal resistance, $R_{thj(r)}$, and Maximum Power, P_D.

1. Calibrating the TSP, Temperature Sensitive Parameter

Since it is basically impossible to put a physical thermometer onto a device's junction to measure its temperature while under power, we must find another approach. Fortunately, we can use the device's forward junction voltage to tell us its temperature. The forward voltage drop of a diode's pn junction has a very linear relationship with temperature. We can use this relationship to tell us what the junction temperature is under any power condition.

To determine the actual voltage temperature relationship of a TSP for a given device, simply calibrate the TSP at a constant sense current over temperature as shown in Figure 2. The TSP sense current used should be small so as to not cause additional heating during calibration.



The forward voltage drop of a MOSFET body diode decreases linearly over temperature at rate of about 2 millivolts per degree Celsius when measured at a sense current of 10ma.

Figure 2. Typical Temperature Calibration Curve for a TMOS™ body diode.

Other device electrical parameters have similar linear relationships to temperature as well. The following are several other temperature sensitive parameters used in the industry to determine a device's junction temperature.

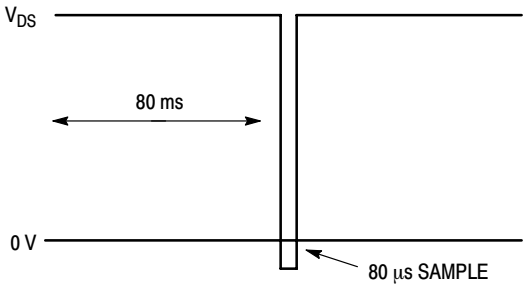
Common TSP:	Device Type:
V_{TH}, $V_{DS(on)}$, $R_{DS(on)}$	MOSFET
V_{TH}, $V_{CE(s)}$	IGBT
V_{BE}, $V_{CE(s)}$	Bipolar
V_F	Diode

Make sure to develop the actual electrical to thermal correlation of the TSP and check it for linearity prior to its use. The linearity of this parameter is critical for accurate thermal measurement.

2. Applying Continuous Power and TSP Sampling Pulses

With a properly chosen and calibrated TSP, we can now provide test signals to the device and make thermal measurements.

We begin by applying a continuous power of known current and voltage to the device. A continuous train of sampling pulses monitors the TSP, and thus the junction temperature. The TSP sampling pulse must provide a sense current equal to that used during calibration. While monitoring the TSP, adjust the applied power so as to insure a sufficient rise in T_J. Adjusting the applied power to achieve a T_J rise of about 100° above the reference temperature will generate enough temperature delta to insure good measurement resolution.



A continuous pulse train consisting of an 80 ms power pulse followed by an 80 μs diode sample is used to apply both power to the device as well as a sample pulse for TSP measurement.

Figure 3. Example of a power and sample pulse train during R_{thjc} measurement of a TMOS device.

The TSP sample time must be very short so as to not allow for any appreciable cooling of the junction prior to re–applying power. The power and sample pulse train shown in Figure 3 has a duty cycle of 99.9% which for all practical purposes is considered continuous power.

Obviously, with this much power being applied to the device under test, the device's case will get very hot. To keep the device cool while under test, we need to mount it to a heat sink of some sort. A heat exchanger with chilled water flowing through it provides a good heat sink. In this way, we can keep the device's case temperature down (i.e., near 25°C) and maintain good measurement resolution (i.e., large temperature delta between the junction and reference location).

3. Measuring T_J, T_R, and Applied Power

After T_J has stabilized, we must record its value along with the reference temperature, T_R, and applied power. To calculate the devices maximum power rating, P_D, and thermal resistance, R_{thjr}, we need to have these measurements.

The devices junction temperature, T_J, is taken from the TSP electrical measurement. With the correlation between the TSP electrical measurement and temperature already established, determining T_J is pretty much straight forward.

A thermocouple placed at the reference location measures the reference temperature, T_R. Most power semiconductor manufacture's use the devices' case, however, the lead, ambient, or all three can be used as reference locations.

Key elements to insure accurate reference temperature measurement are:

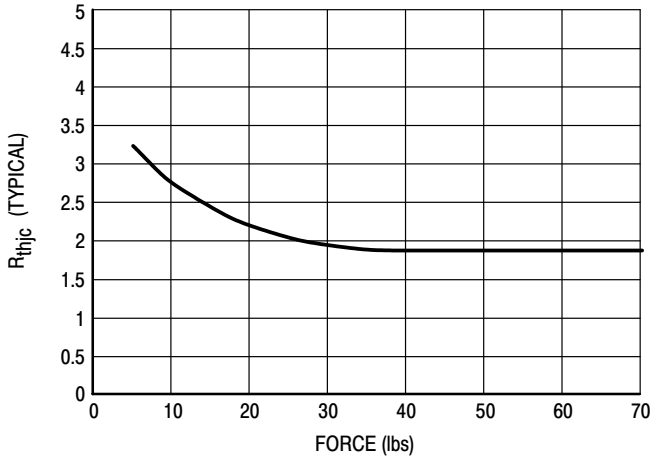
- Good thermocouple to reference contact
- Consistent thermocouple placement location

The reference thermocouple needs to make a good thermal contact to its reference location. This applies to reference locations other than ambient. Without a good thermal contact, measurement error will occur. To improve this contact, use both thermal grease and device clamping pressure as suggested.

Use thermal grease to insure good thermal conductivity and to eliminate air gaps. Applying thermal grease between the device and the heat sink used to keep the case temperature near 25°C will help in two ways. First, it will help keep the case temperature down during measurement by improving the thermal contact to the heat sink. Second, it will also improve the thermocouple to case contact as well. As stated earlier, the case is usually used as the reference location for thermal measurements. Thermal grease helps to maintain good thermal contact and insure measurement accuracy.

Applying about 40 lb of force (85 to 90 PSI) between the thermocouple and the reference location (i.e., device's case) also improves the thermal contact as shown in Figure 4. The application of pressure to the device seems to smooth out thermal grease thickness variations and eliminate air gaps at the contact interface.

Taking these precautions into consideration will help insure a good thermal contact to the reference location surface (i.e., device case).



The value of measured thermal resistance drops and becomes consistent at about 40 lb. of clamp force (85–90 PSI) insuring good thermal contact between the thermal couple and the devices case. [1]

Figure 4. R_{thjc} vs. Clamp Force for a ON Semiconductor MJF10012 TO–218 Fullpak device with uncontrolled thermal grease thickness.

The reference thermocouple needs to be placed at the same location for every device. Any change in the placement of this thermocouple will result in error or at the very least inconsistencies between measurements. A different thermal resistance exists between the junction and the location of each thermocouple placement. Usually for the best readings, the reference thermocouple should be placed at the hottest location on the package (i.e. for TO–220 devices, at the center of the die on the back side of the devices metal case). In any event, to be accurate and consistent, always place the reference thermocouple in the same location for each device measured.

4. Calculating Thermal Resistance, $R_{thj(r)}$, and Maximum Power, P_D

We can use equations (1) and (2) presented earlier, along with our measurements, to calculate the devices thermal resistance and maximum power capability.

Assuming we measured the following; T_J = 100°C, applied test power = 50 W, T_C = 25°C, and maximum device temperature rating = 150°C, we use equation (1) to calculate R_{thjc}.

$$R_{thjc} = (100 – 25)/50$$
$$= 1.5°C/W \text{ (measured value)}$$

Most manufacturer's will guardband the measured R_{thjr} reading to establish their device limits. This helps take into consideration all of the variables involved which cause inconsistencies in readings. A guardband of 25% for thermal measurements is considered good practice.

Multiplying the measured thermal resistance from above by 1.25 to guardband it by 25%, we get the following specified R_{thjc}.

$$R_{thjc} = 1.5 * 1.25$$
$$= 1.9°C/W \text{ (manufacturer's guaranteed limit)}$$

As shown in the Figure 5, the thermal resistance from junction to case is largely dependent on the die size of the device. This implies that silicon has a much larger thermal resistance, or opposition to heat flow, than that of the copper header to which it is bonded to.

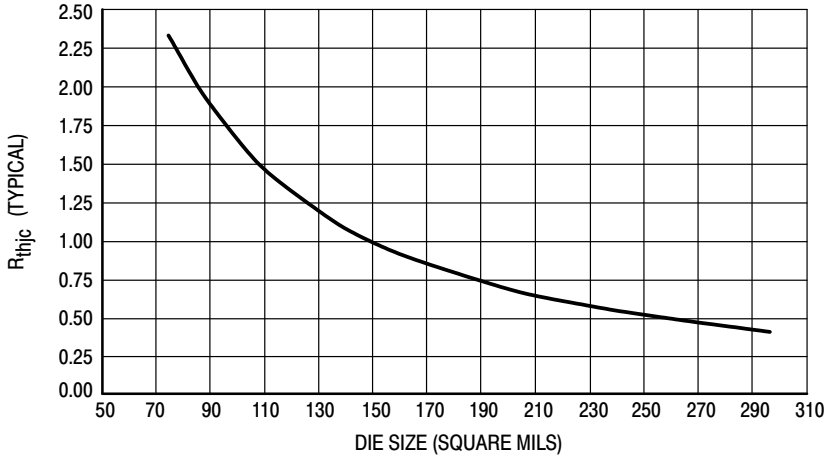


Figure 5. R_{thjc} vs. die size for TMOS® devices in TO–220, D^2PAK, DPAK & TO–247 Packages.

To determine a devices power handling capability, P_D, we use the specified R_{thjc} taken from above along with equation (2).

$$P_D = (150 – 25)/1.9$$
$$= 66 \text{ W (manufacturer's guaranteed limit)}$$

Using Thermal Parameters to Solve Often Asked Thermal Questions

One can use measured or specified thermal parameters to solve many common questions asked about power semiconductor devices. The two examples shown below use thermal parameters to solve frequently asked questions.

Example #1

Calculate the device's junction temperature: Using equation (3) with a known R_{thjc} of 1.25°C/W, case temperature of 85°C, and applied power of 35 W.

$$T_J = 35 * 1.25 + 85$$
$$= 128.8°C$$

Example #2

Calculate the power handling capability : Using equation (2) with a known R_{thjc} of 1.0°C/W, a starting case temperature of 75°C and a maximum rated T_J of 150°C.

$$P_D = (150 – 75)/1.0$$
$$= 75 \text{ W}$$

SUMMARY

This paper presents a description of basic semiconductor thermal measurement as well as the use of thermal data in real world examples. Included are terms, definitions, equations and test equipment required. This provides the reader with information useful in answering many common questions regarding the basic thermal capabilities of power semiconductor devices.

REFERENCES

[1] Billings, Dave, 1992, "Thermal Performance of the TO–218 Fullpak MFJ10012 under Force Loading", ON Semiconductor.

[2] Gottlieb, Irving M., 1992, *Regulated Power Supplies*, 4th Edition, Blue Ridge Summit, Pennsylvania, TAB BOOKS: (92–105).

[3] Pshaenich, Al, "Basic Thermal Management of Power Semiconductors", ON Semiconductor Application Note *AN1083*.

[4] Roehr, Bill and Bryce Shiner, "Transient Thermal Resistance — General Data and its Use", AN569 in ON Semiconductor *Power Applications Manual*, 1990: (23–38), ON Semiconductor Literature Distribution Center, Ph. # 1 (800) 344–3860.

This data was collected using thermal test die in 20-pin PLCC packages on PLCC test boards (2.24″ x 2.24″ x .062″ glass epoxy, type FR-4, with solder coated 1 oz./sq. ft. copper).

LS: 12MRM 93831A

Integrated Circuit Package Thermal Management

Circuit performance and long–term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit – from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\overline{\theta}_{JC} + \overline{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\overline{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).
$\overline{\theta}_{JC}$ = average thermal resistance, junction to case
$\overline{\theta}_{CA}$ = average thermal resistance, case to ambient
$\overline{\theta}_{JA}$ = average thermal resistance, junction to ambient

This ON Semiconductor recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL–M–38510 (JAN) MECL 10K devices.

Only two terms on the right side of equation (1) can be varied by the user – the ambient temperature, and the device case–to–ambient thermal resistance, $\overline{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\theta}_{CA}$ thermal resistance term. $\overline{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

Table 1. Thermal Resistance Values for Standard MECL I/C Packages

Thermal Resistance in Still Air										
Package Description							θ_{JA} (°C/Watt)		θ_{JC} (°C/Watt)	
No. Leads	Body Style	Body Material	Body WxL	Die Bond	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	Avg.	Max.	Avg.	Max.
8	DIL	EPOXY	1/4″×3/8″	EPOXY	2496	8100	102	133	50	80
8	DIL	ALUMINA	1/4″×3/8″	SILVER/GLASS	2496	N/A	140	182	35	56
14	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	6400	84	109	38	61
14	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
16	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	12100	70	91	34	54
16	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
20	PLCC	EPOXY	0.35″×0.35″	EPOXY	4096	14,400	74	82	N/A (6)	N/A (6)
24	DIL (4)	EPOXY	1/2″×1–1/4″	EPOXY	8192	22500	67	87	31	50
24	DIL (5)	ALUMINA	1/2″×1–1/4″	SILVER/GLASS	8192	N/A	50	65	10	16
28	PLCC	EPOXY	0.45″×0.45″	EPOXY	7134	28,900	65	68	N/A (6)	N/A (6)

NOTES:
1. All plastic packages use copper lead frames – ceramic packages use alloy 42 frames.
2. Body style DIL is "Dual–In–Line."
3. Standard Mounting Methods:
   a. Dual–In–Line In Socket or P/C board with no contact between bottom of package and socket or P/C board.
   b. PLCC packages solder attached to traces on 2.24″ × 2.24″ × 0.062″ FR4 type glass epoxy board with 1 oz./S.F. copper (solder coated) mounted to tester with 3 leads of 24 gauge copper wire.
4. Case Outline 649
5. Case Outline 623
6. $\theta_{JC} = \theta_{JA} - \left(\frac{T_C - T_A}{P_D}\right)$

T_C = Case Temperature (determined by thermocouple)

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature–controlled heatsink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D (\overline{\theta}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Table 1. In , this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life ($\geq$ 100,000 hours for ceramic packages).

AIR FLOW

The effect of air flow over the packages on $\overline{\theta}_{JA}$ (due to a decrease in $\overline{\theta}_{CA}$) is illustrated in the graphs of Figure 1 through Figure 3. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual–in–line packaged MECL 10K quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 4, $\overline{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$$T_J = P_D (\overline{\theta}_{JA}) + T_A$$

$$T_J = (0.195\ W)\ (50°C/W) + 25°C = 34.8°C$$

Under the above operating conditions, the MECL 10K quad gate has its junction elevated above ambient temperature by only 9.8°C.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

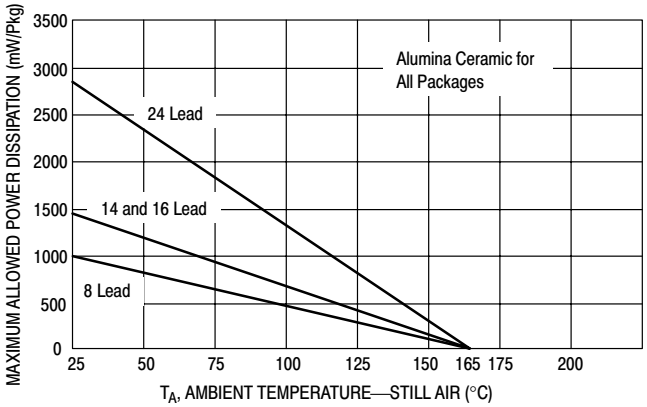


Figure 1. Ambient Temperature Derating Curves
(Ceramic Dual–In–Line Pkg)

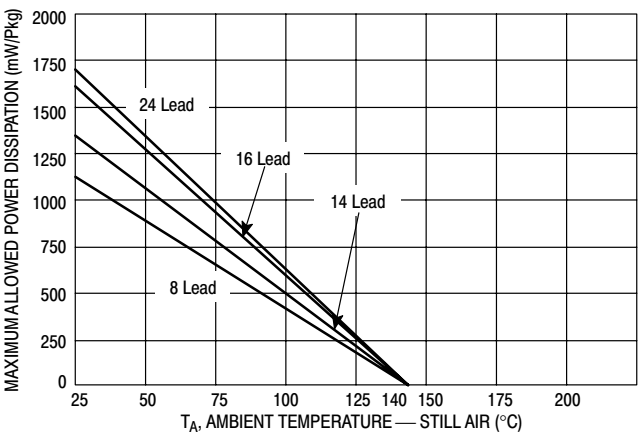


Figure 2. Ambient Temperature Derating Curves
(Plastic Dual–In–Line Pkg)

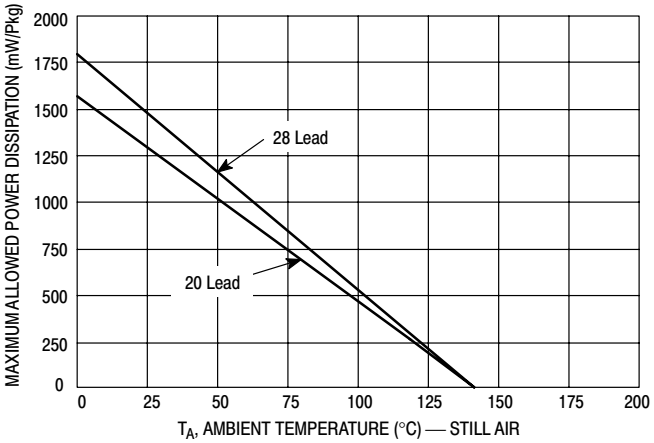


Figure 3. Ambient Temperature Derating Curves
(PLCC Pkg)

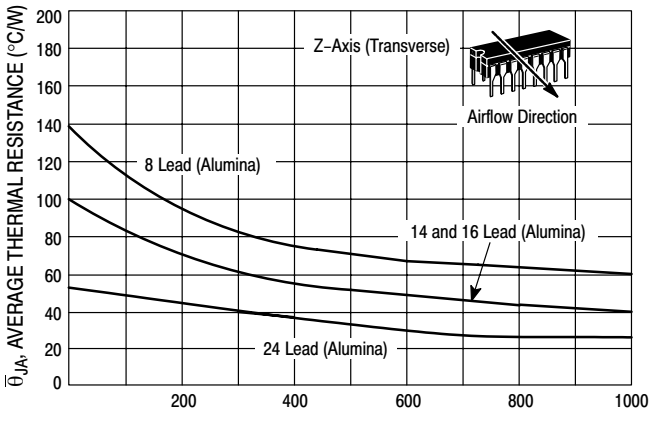


Figure 4. Airflow versus Thermal Resistance (Ceramic Dual–In–Line Pkg)

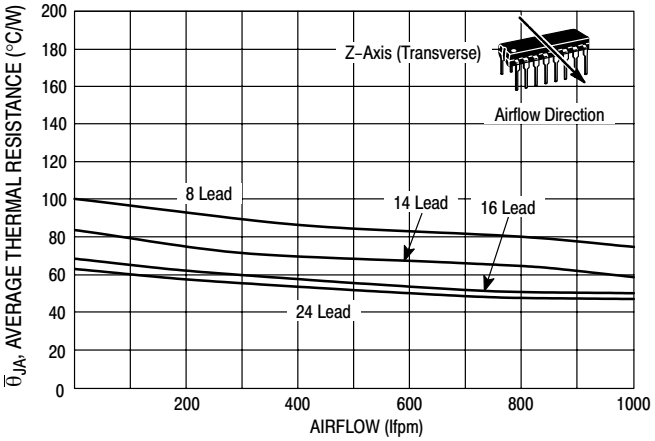


Figure 5. Airflow versus Thermal Resistance (Plastic Dual–In–Line Pkg)

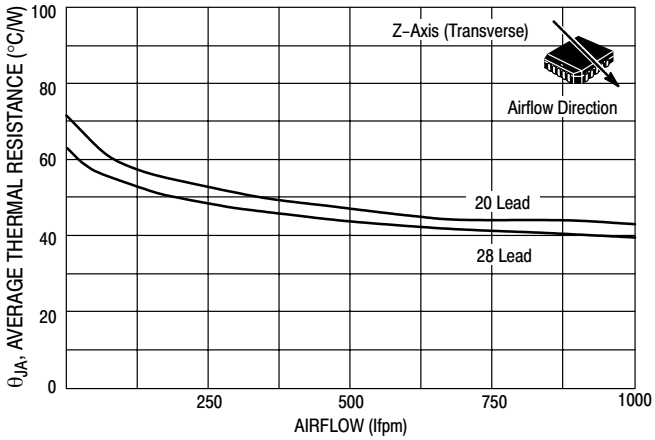


Figure 6. Airflow versus Thermal Resistance (PLCC Pkg)

Table 2. Thermal Gradient of Junction Temperature (16–Pin MECL Dual–In–Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062″ PC board with Z axis spacing 0.5″. Air flow is 500 lfpm along the Z axis.

The majority of MECL 10H, MECL 10K, and MECL III users employ some form of air–flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Table 2 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual–in–line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Todays plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$(1)\ T = (6.376 \times 10^{-9})\, e \left[\frac{11554.267}{273.15 + T_J} \right]$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).

T_J = Device junction temperature, °C.

And:

$$(2)\ T_J = T_A + P_D\theta_{JA} = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.

T_A = Ambient temperature, °C.

P_D = Device power dissipation in watts.

θ_{JA} = Device thermal resistance, junction to air, °C/Watt.

ΔT_J = Increase in junction temperature due to on–chip power dissipation.

Table 3 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

Table 3. Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temp °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 3 is graphically illustrated in Figure 7 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid–life failure rates of plastic devices are not effected by this intermetallic mechanism.

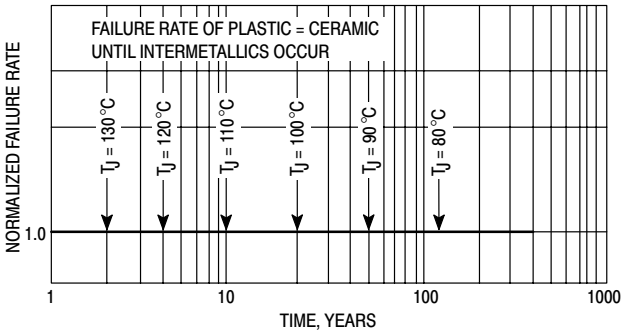


Figure 7. Failure Rate versus Time Junction Temperature

MECL Junction Temperatures:

Power levels have been calculated for a number of MECL 10K and MECL 10H devices in 20 pin plastic leaded chip carriers and translated to the resulting increase of junction temperature (ΔT_J) for still air and moving air at 500 LFPM using equation 2 and are shown in Table 4.

Table 4. Increase in Junction Temperature Due to I/C Power Dissipation.
20 Pin Plastic Leaded Chip Carrier

MECL 10K Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air	MECL 10H Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air
MC10101	21.8	14.1	MC10H016	48.0	30.0
MC10102	17.6	11.4	MC10H100	16.6	10.8
MC10103	17.6	11.4	MC10H101	22.1	14.5
MC10104	20.8	13.4	MC10H102	18.0	11.8
MC10105	17.2	11.2	MC10H103	18.0	11.8
MC10106	13.0	8.4	MC10H104	21.0	13.5
MC10107	19.8	12.8	MC10H105	17.8	11.7
MC10109	11.7	7.7	MC10H106	13.2	8.7
MC10110	24.7	16.1	MC10H107	20.0	12.9
MC10111	24.7	16.1	MC10H109	11.9	7.8
MC10113	22.2	14.3	MC10H113	22.8	14.8
MC10114	22.6	14.6	MC10H115	16.7	10.9
MC10115	16.7	10.9	MC10H116	17.8	11.7
MC10116	17.2	11.1	MC10H117	16.7	11.0
MC10117	16.2	10.5	MC10H121	13.9	9.1
MC10121	13.5	8.5	MC10H123	23.1	15.0
MC10123	37.6	24.0	MC10H124	44.2	28.4
MC10124	42.9	27.3	MC10H125	–	–
MC10125	–	–	MC10H130	28.2	18.2
MC10131	26.9	17.1	MC10H135	33.2	21.4
MC10133	34.4	21.9	MC10H136	61.7	38.5
MC10134	27.0	17.2	MC10H141	44.3	28.0
MC10135	31.9	20.3	MC10H158	25.3	16.4
MC10136	52.3	32.6	MC10H159	27.3	17.7
MC10138	37.0	23.2	MC10H160	32.1	20.5
MC10141	42.7	26.7	MC10H161	41.5	26.7
MC10153	34.4	21.9	MC10H162	41.5	26.7
MC10158	23.9	15.2	MC10H164	31.9	20.6
MC10159	25.8	16.4	MC10H165	56.3	35.8
MC10160	32.0	20.4	MC10H166	44.4	28.3
MC10161	40.7	26.0	MC10H171	41.9	26.9
MC10162	40.7	26.0	MC10H172	41.9	26.9
MC10164	31.3	20.1	MC10H173	32.6	21.1
MC10165	53.7	33.6	MC10H174	32.5	21.0
MC10166	43.5	27.6	MC10H175	45.9	29.6
MC10168	34.4	21.9	MC10H176	50.9	32.3
MC10170	29.9	18.9	MC10H179	35.0	22.6
MC10171	41.1	26.2	MC10H180	42.4	27.2
MC10172	41.1	26.2	MC10H181[4]	64.4	38.6
MC10173	30.5	19.3	MC10H186	50.2	31.8
MC10174	31.9	20.5	MC10H188	25.8	16.7
MC10175	43.7	27.6	MC10H189	25.8	16.7
MC10176	49.6	31.3	MC10H209	18.9	12.5
MC10178	38.1	23.9	MC10H210	25.0	16.4
MC10186	49.6	31.1	MC10H211	25.0	16.4
MC10188	25.4	16.4	MC10H330[4]	65.8	36.1
MC10189	24.6	15.9	MC10H332	52.2	33.5
MC10192	67.0	43.0	MC10H334	77.8	49.3
MC10195	46.7	29.9	MC10H350	–	–
MC10197	27.7	17.7	MC10H351	27.2	18.1
MC10198	21.2	13.4	MC10H352	27.2	18.1
MC10210	24.5	16.0	MC10H424	37.7	24.3
MC10211	24.6	16.0			
MC10212	24.3	15.8			
MC10216	24.1	15.6			
MC10231	30.6	19.5			

NOTES:
(1) All ECL outputs are loaded with a 50 Ω resistor and assumed operating at 50% duty cycle.
(2) ΔT_J for ECL to TTL translators are excluded since the supply current to the TTL section is dependent on frequency, duty cycle and loading.
(3) Thermal Resistance (θ_{JA}) measured with PLCC packages solder attached to traces on 2.24″ x 2.24″ x 0.062″ FR4 type glass epoxy board with 1 oz./sq. ft. copper (solder–coated) mounted to tester with 3 leads of 24 gauge copper wire.
(4) 28 lead PLCC.

Case Example:

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each plastic device in the system should be evaluated for maximum junction temperature using Table 4. Knowing the maximum junction temperature refer to Table 3 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 7.

To illustrate, assume that system ambient air temperature is 55°C (an accepted industry standard for evaluating system failure rates). Reference is made to Table 4 to determine the maximum junction temperature for each device for still air and transverse air flow of 500 LFPM.

Adding the 55°C ambient to the highest, ΔT_J listed, 77.8°C (for the MC10H334 with no air flow), gives a maximum junction temperature of 132.8°C. Reference to Table 3 indicates a departure from the desired failure rate after about 2 years of constant exposure to this junction temperature. If 500 LFPM of air flow is utilized, maximum junction temperature for this device is reduced to 104.3°C for which Table 3 indicates an increased failure rate in about 15 years.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10K and MECL III devices are given for an operating temperature range from –30°C to +85°C (0° to +75°C for MECL 10H and memories). These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heatsinking (i.e., dual–in–line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non–metalized area of P/C board).

The designer may want to use MECL devices under conditions other than those given above. The majority of the low–power device types may be used without air and with higher $\overline{\theta}_{JA}$. However, the designer must bear in mind that junction temperatures will be higher for higher $\overline{\theta}_{JA}$, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual–in–line ceramic device operated at $\overline{\theta}_{JA}$ = 100°C/W (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a $\overline{\theta}_{JA}$ = 50°C/W. (Level shift = $\Delta T_J \times 1.4$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heatsinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEATSINK SUGGESTIONS

With large high–speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two–sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two–ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 8, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug–in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

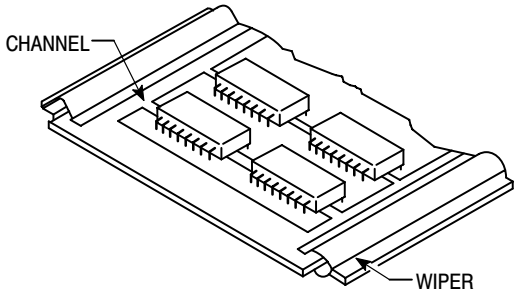


Figure 8. Channel/Wiper Heatsinking on Double Layer Board

For operating some of the higher power device types* in 16 lead dual–in–line packages in still air, requiring $\overline{\theta}_{JA}$ <100°C/W, a suitable heatsink is the IERC LIC–214A2WCB shown in Figure 9. This sink reduces the still air $\overline{\theta}_{JA}$ to around 55°C/W. By mounting this heatsink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, $\overline{\theta}_{JA}$ is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for MECL 10H memories) or in lowering T_J for improved reliability.

It should be noted that the use of a heatsink on the top surface of the dual–in–line package is not very effective in lowering the $\overline{\theta}_{JA}$. This is due to the location of the die near the bottom surface of the package. Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

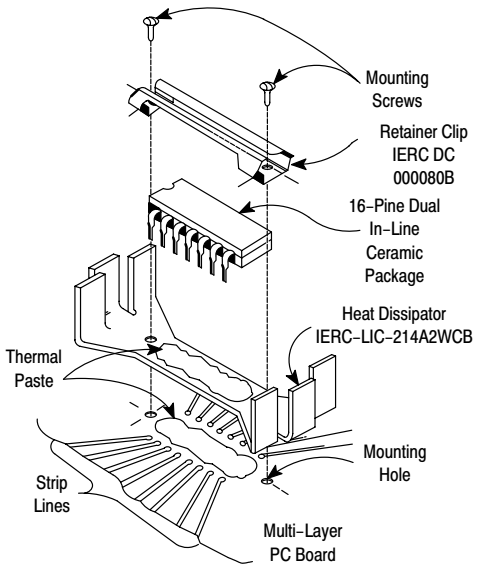


Figure 9. MECL High–Power Dual–in–Line Package Mounting Method

New Models and Techniques for Analyzing the Power Transistor and its Thermal Environment

By Kim Gauen
ON Semiconductor

INTRODUCTION

In many electronic systems, power transistors perform critical system functions. They also can account for a significant portion of the total system cost. Better performance can come at a higher price, but balancing this price/performance tradeoff has not been easy for designers. Thermal issues are involved, and the tools for analyzing the electrical/thermal environment have not been available. Recently, new tools have become available and techniques are now appearing for sophisticated analysis of the power transistor and its thermal environment.

This paper describes one set of tools and some techniques for thermal/electrical analysis. Because the power MOSFET is so popular, it is one of the first devices to be characterized for such evaluations and it is the focus of this paper.

Know Your Transistor's Operating Temperature

Probably the two most important parameters for keeping a power MOSFET within its safe operating area are its silicon temperature, often referred to as its "junction temperature (T_J)," and the voltages appearing across its terminals. Steady state current handling capability is certainly important, but it is usually bounded by the maximum rated junction temperature and not by effects such as wirebond limitations, metal migration of the source metal, or insufficient gate voltage.

There are several reasons why it is important to know a power MOSFET's junction temperature. First, junction temperature affects reliability. High temperature and the associated thermal cycling accelerate several failure mechanisms. Second, parameters that affect junction temperature also influence system cost. An overly conservative designer might use a power transistor that is unnecessarily large and expensive for the application. On the other hand, using a transistor that is undersized might result in the designer selecting a heat sink that is larger and more expensive than necessary. Third, knowing T_J will help the designer understand how the system will operate under various loading conditions and temperatures. MOSFET junction temperature affects its breakdown voltage, on–resistance, threshold voltage, switching speed, and transfer characteristics — all of which can cause changes in system level performance. For example, changing a MOSFET's switching speed is likely to affect the system's noise performance, and the MOSFET is certainly less efficient at higher temperatures due to a significant increase in $R_{DS(on)}$. With cost, system performance, and reliability at stake, the designer needs good tools for determining junction temperature and evaluating design tradeoffs.

Traditional Method of System Design

The traditional way to size a power transistor is to estimate the on–resistance requirements and the associated on–state losses and switching losses and then to estimate the size of the heat sink needed for the anticipated load currents and ambient temperature. The system is then assembled and tested and (sometimes) the transistor's case temperature is measured under "worst case" conditions. Heat sink or transistor size is then modified, and the system is retested and refined until the results are acceptable.

The limitations of this approach are well known. First, system complexity and lack of time often limit the engineer's ability to completely analyze the system prior to assembling hardware. Therefore, the first prototype is based on calculations, educated guesses, and intuition. Good analysis tools and techniques can produce a much better first pass implementation in hardware.

Second, determining "worst case" conditions might not be easy. For example, the highest junction temperature usually occurs at the maximum anticipated ambient temperature, but sometimes that is not the case. For some loads, currents are significantly higher at cold temperatures. If a large load such as a motor has a very long thermal time constant, the power transistor could see high currents for a long time relative to the thermal time constant of it and its heat sink. It would be helpful to have a method of quickly evaluating the effects of these and other changing conditions.

The third problem with the traditional approach is that it is cumbersome to evaluate system trade–offs with hardware. Heat sinks must be built and changed, the system must be tested under various conditions, loads must be built, ambient temperatures must be controlled, etc.

Other difficulties are related directly to analyzing the thermal system. The first problem is that junction temperature is not easy to measure. Using an infrared camera to view an unencapsulated die would be ideal, but few designers have this option.

More likely, a designer places a thermocouple on the heat sink next to the MOSFET or directly on the MOSFET's tab. But under transient conditions or at high power, these measurements are probably at least several degrees lower than the actual junction temperature.

The most accurate way to monitor the junction temperature of a plastic encapsulated MOSFET is to use one of its temperature sensitive parameters, or TSPs. The MOSFET's TSPs are its on–resistance, the forward voltage drop of its body diode, its threshold voltage, and its breakdown voltage. All four require that each test device be calibrated over temperature, which is time consuming. The first two TSPs are the ones most commonly used.

In circuits where the MOSFET is on continuously, using $R_{DS(on)}$ as the TSP works fairly well. A low voltage MOSFET, however, may give a signal that is too low for accurate measurement. Therefore, this method works best for high on–resistance (high voltage) devices. Monitoring the forward voltage drop of the body diode gives very good results, but it is difficult to build the circuitry that interrupts the normal drain to source load current and forces a small source to drain sense current in the body diode. The technique of using the body diode is discussed in detail in References [1] and [2].

Even if the system is characterized perfectly, there are remaining roadblocks to accurately predicting junction temperature. Power waveforms are often complex, making analysis very difficult. The graphical methods described in Reference [3] can help, but they are unwieldy with complex waveforms. Next, there is the issue of how to monitor junction temperature to verify simulation results. Finally, it is important to provide power inputs to the thermal network and thermal inputs to the electrical system. Until recently, the only way to provide thermal feedback was to do it iteratively with successive simulation runs, one for each new junction temperature estimate. That approach suffices for steady state conditions, but it is not accurate for transient analysis since it cannot track junction temperature variations throughout the simulation.

Requirements for Accurate Models

To accurately model the electrical/thermal system a designer needs:

1. an accurate model of the MOSFET that is temperature dependent
2. a model of the MOSFET that supports passing information between the electrical and thermal environments during the simulation (these models are "dynamically" temperature dependent)
3. an accurate model of the MOSFET's thermal environment
4. tools that support the above models for easy simulation and analysis

Each of the above requirements can now be met, and the pieces have been assembled into a very effective analysis tool.

The first requirement is an accurate and robust model of the power MOSFET that is also temperature dependent. This model should accurately predict the I–V characteristics for the forward range of operation, as well as leakage, reverse recovery and breakdown characteristics of the drain–source body diode. The electrical model must also describe the nonlinear gate drain (and gate source for negative V_{GS}) capacitances that are key to accurate transient simulations.

In the language of simulation a "robust" model is one that does not cause convergence problems, which are most commonly the result of discontinuities in the model. Many SPICE based subcircuit models have been introduced over the years in an attempt to describe the non linear power MOSFET capacitances; however, the macro modeling approach introduces discontinuities. Although such discontinuities may be acceptable in a purely electrical simulation environment, the complexity of the dynamic electro–thermal system requires models with superior convergence qualities.

So far, the model we have discussed is a "static" thermal model. This means that the designer can assign any reasonable temperature to the model prior to simulation. However, device temperature will remain constant throughout the simulation, regardless of power dissipation. Instead of this static model, we require a "dynamic" thermal model that allows the device temperature to change as electrical energy is converted to heat, as it does in a real device. To accomplish this, the temperature parameter, used inside the MOSFET model to adjust the electrical parameters for thermal effects, must now become an independent variable solved by the simulator. When temperature is an independent variable, the simulator must solve a set of simultaneous nonlinear differential equations for temperature and heat flow as well as for voltage and current for each node and each time step.

The third requirement, having accurate models of the thermal environment, is a bit tricky to meet because there is no standard methodology for obtaining such models. The system designer has difficulty obtaining thermal models of heat sinks and extracting thermal models of the MOSFET from the information provided on the MOSFET data sheets. Neither the power transistor user nor the semiconductor manufacturer has a very good handle on characterizing the thermal interface between the case and the heat sink. However, techniques are available to get such models. The best technique depends on the pulse width of interest.

Transient thermal response curves for power transistors have been around for a couple of decades. A curve like the one shown in Figure 1 is generated by observing the response of the transistor's junction temperature to a step function of power dissipation. One can develop a thermal R–C network from a transient thermal response curve.

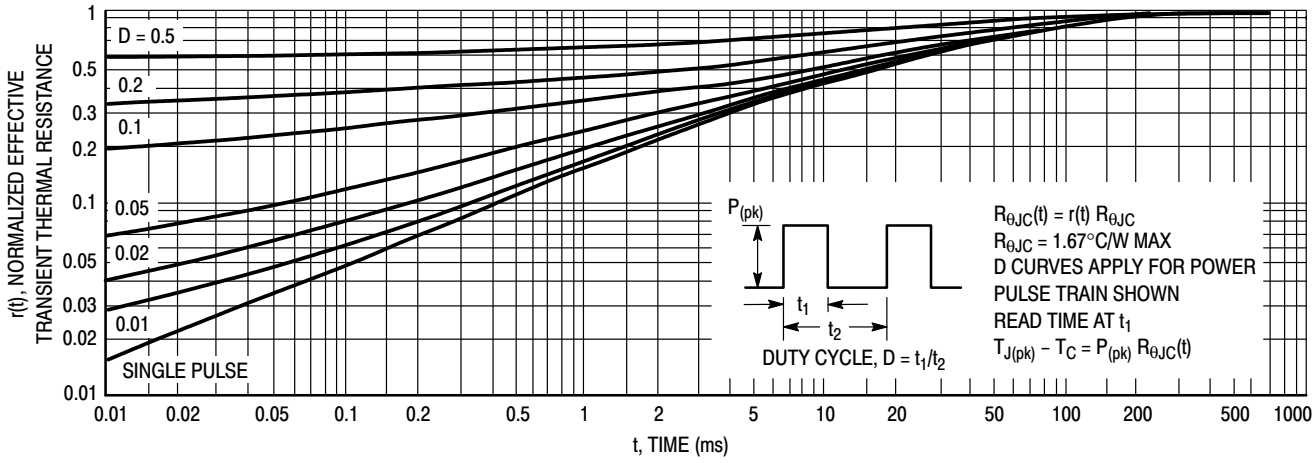


Figure 1. It is possible to generate thermal models from transient thermal response curves such as this one for a 4 A, 500 V MOSFET in a TO–220 package.

These curves are perfectly adequate for analysis — if the power transistor's case temperature is known and the power dissipation waveform is relatively simple. The accepted definition of "case temperature" is the temperature of the hottest part of the transistor's tab, which is the spot on the tab just behind the power transistor die, as shown in Figure 2. Unfortunately, monitoring this temperature is not easy and a tab or heat sink temperature is often measured instead. So, the situation that is easiest to analyze is one where the case temperature doesn't change, as would happen under brief transient conditions or when the tab is attached to a known and constant temperature — an "infinite heat sink."

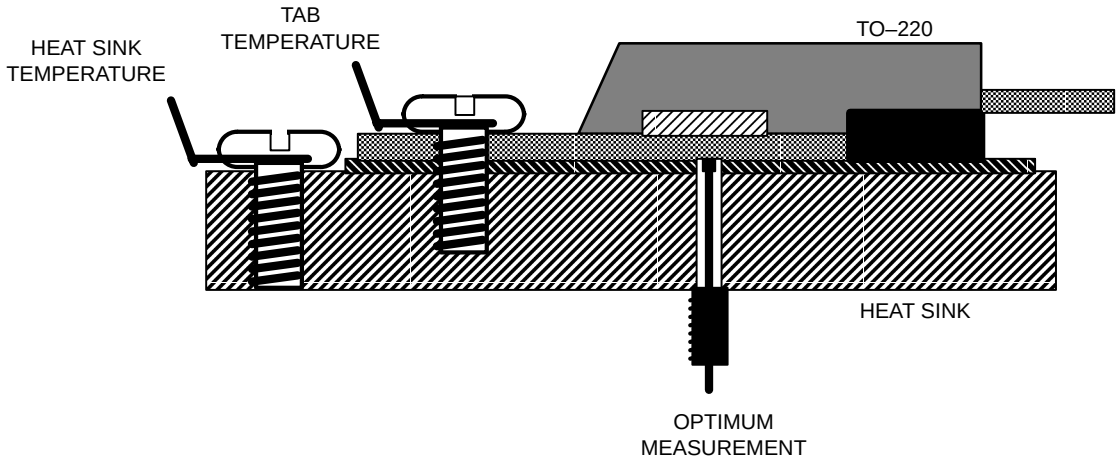


Figure 2. The standard way to measure the heat sink of a power transistor is to place a thermocouple through the heat sink and against the back of the transistor's tab, just opposite the center of the die.

Steady state conditions are also fairly easy to characterize and then model. One could characterize the system's thermal resistances (junction to tab, tab to heat sink, heat sink to ambient), put the steady state models into the simulator, and again the modeling should go smoothly. But for many cases, i.e., for power pulses more than a few milliseconds yet not DC, an approach that defines the entire thermal system is needed.

An effective method is to treat the power transistor and its heat sink as a unit and characterize the assembly just as one would characterize a power transistor — in effect, developing a transient thermal response curve for the entire thermal system. This method inherently addresses the thorny problem of trying to define the thermal interface if the power transistor and the heat sink are characterized separately. The interface is simply one part of the network, and the empirical tests automatically include its effects. The last circuit example in this paper shows how to use this technique.

The fourth and final requirement is for a simulator that can support thermal as well as electrical models, allowing the electrical system to affect the thermal and visa versa. In system simulators such as SPICE the system variables are constrained to voltage and current. In order to simulate

non–electrical systems in these types of simulators, the non electrical system must be written in terms of equivalent electrical elements, or macro–models. Macro modeling techniques of electro–thermal systems suffer from their inability to directly adjust the internal electrical model parameters for the non–electrical changes in the system. To circumvent this limitation, the user is forced to make gross adjustments to the external nodes of the circuit through controlled sources or other elements.

Simulators such as Analogy's SABER provide a modeling language which separates the simulation "engine" from the models. (Analogy's hardware description language is MASTTM.) This allows the user to develop models as a system of through and across variables that are not constrained to voltage and current. Thus, the relationship between electrical and thermal energy can be described directly in the model. The SABER simulator uses a dynamic thermal version of the MPV3 MOSFET model (MPV3X), which is the basis of the library of ON Semiconductor MOSFET models provided with the 4.0 release of SABER.

A Simple Example

A simple example illustrates the basic modeling concepts and some of the analysis possibilities. Assume that the desired load current conducted by a pair of MTP75N05HDs is 35 A and that the load current lasts for an indefinite time. Also assume that the heat sink is a 40 mm by 20 mm by 12 mm piece of aluminum with no fins. Such a heat sink has a large thermal capacity and low cost, but poor thermal resistance. So, the question might be, "In a 25°C environment, how hot do the power transistors get and how long does it take to reach steady state conditions?" Without good evaluation tools or actual hardware, it is difficult to tell if the transistors will slip into a thermal runaway condition.

The first step is to characterize the heat sink. A single MOSFET was mounted to the heat sink and was controlled to step its power dissipation from 0 to a constant and continuous 7.87 W. The MOSFET's tab was monitored until the system became stable. From the power dissipation and the difference between the tab and ambient temperatures, the thermal resistance is easily calculated. For this heat sink in a 30°C environment:

$$T_{tab} - T_{amb} = P_D * R_{th\_hs}$$

$$152°C - 30°C = 7.87 * R_{th\_hs}$$

Therefore, $R_{th\_hs} = 15.5°C/W$

Like all others, this heat sink consists of a network of distributed thermal resistances and capacitances. The construction and complexity of a heat sink determines how to select the lumped elements that model its thermal network. In cases like this, a single thermal resistance and capacitance model the heat sink well enough for purposes here.

With the assumption that a single R–C network is adequate, the task is now to determine the heat sink's thermal capacitance. Figure 3 shows how the transistor's tab temperature varies with time, and the data suggest a tau of about 420 seconds. That sets the thermal capacitance to 27 J/°C. Simulating with an Rth_hs of 15.5°C/W, a Cth of 27 J/°C and a power dissipation of 7.87 W yields a response that is within measurement error of the actual system response. This system is relatively easy to model since the power dissipation in the MOSFET is held constant by gate drive circuitry and the thermal network is quite simple.

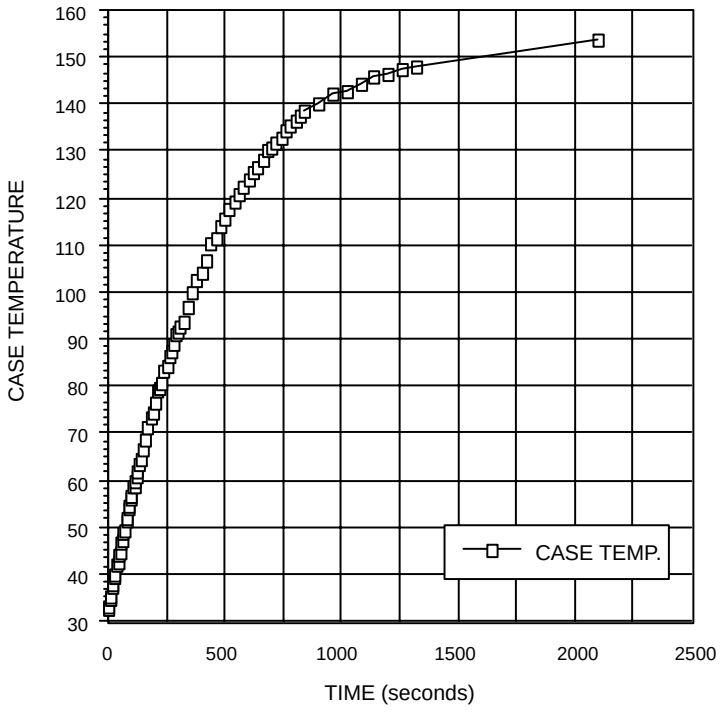


Figure 3. Thermal response of 40 x 20 x 12 mm Al heat sink

A more difficult test of the models and the simulation methodology is to revisit the conditions and requirements of the initial application. In this case, two MOSFETs were mounted to the same heat sink and they were forced to conduct 17.5 A continuously at an ambient and initial heatsink temperatures of 20.7°C. The added difficulty of this simulation is that the power dissipation of the MOSFET causes the heat sink and junction temperatures to increase, which increases on–resistance and further increases power dissipation. The change in $R_{DS(on)}$ cannot be ignored because it increases by about 70% for a 100°C rise in junction temperature. The first simulation was simpler because the power dissipation was held constant since the MOSFET was forced by gate drive circuitry to operate as a constant current source.

The results of the simulated $V_{DS(on)}$ and the actual tab temperature data are shown in Figure 4. Again, the empirical and simulated curves are the same within a couple of degrees and about 10 mV. For this example, the tab temperature is very close to the junction temperature since the MOSFET's power dissipation is less than 3.5 W. The results track nicely only because SABER's MOSFET model is dynamically temperature dependent. The model correctly predicted the final junction temperature and that the system would not go into thermal runaway. Additionally, the MOSFET's $V_{DS(on)}$ in simulation matched the empirical results even as junction temperature changed, further validating the model.

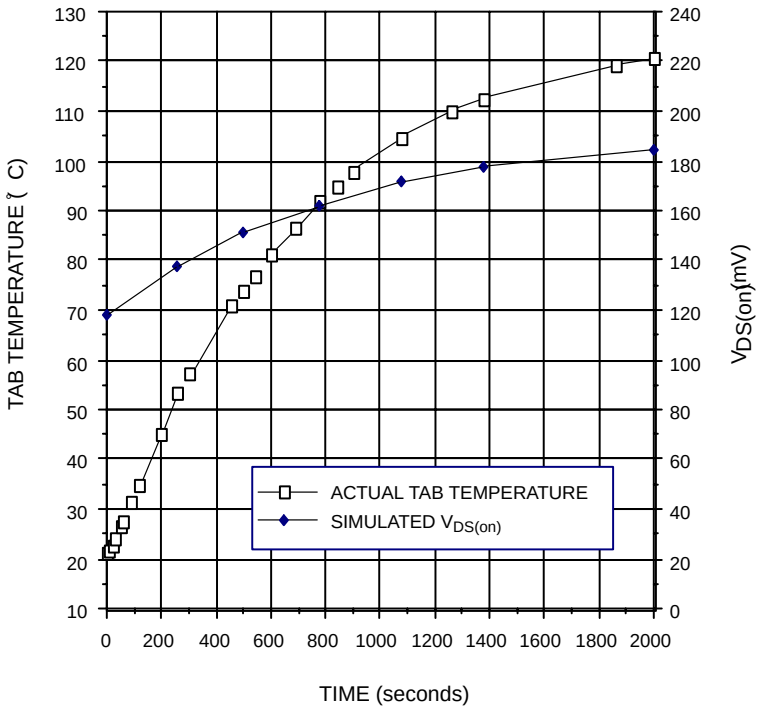


Figure 4. One of two MTP75N06HDs conducting a total continuous current of 35 A. Simulation results closely matched empirical results.

A More Complex Example

The above example validates the general concept for a relatively simple circuit. Adding pulse width modulation to the circuit further illustrates the technique's strengths, but it also uncovers some limitations. This final example also validates the technique of developing and using a transient thermal response curve for a MOSFET attached to a heat sink.

Like the other examples, the first step in this analysis is to determine the system's thermal model. But this time we are interested in the system's thermal response to very narrow power pulses that occur during switching transitions as well as the comparatively very long response of the heat sink. In fact, we are interested in responses to pulse widths varying about nine orders of magnitude; so it's likely that there are new measurement challenges.

Until recently, thermal response test equipment had maximum pulse width capability of at most a few seconds. The advent of surface mount power devices and the much longer thermal response time of the transistor/circuit board combination bought about the need for equipment that can apply a power pulse and measure the response for several minutes. One vendor of this new equipment is Analysis Tech, and their Phase 9 automatic transient thermal response tester was used in this study.

The Analysis Tech Phase 9 can be used to measure the thermal response of the system of interest here, i.e., a power transistor mounted to moderate size heat sink. For this

exercise an MTP15N06V (a 15 A, 60 V MOSFET) was mounted to a Wakefield 667–10ABPP heat sink. The Wakefield heat sink is finned and is 1″ tall, 1.35″ wide, and 0.5″ deep.

For MOSFET data sheet characterization, the transient thermal response is normally taken with the device mounted to an infinite (water cooled) heat sink. The infinite heat sink fixes the MOSFET's case temperature to a known value which serves as the reference temperature for the characterization. Instead of a water cooled heat sink, the Wakefield heat sink was used, and the reference temperature was the ambient temperature.

The thermal response of the MOSFET on the water cooled heat sink and the response on the Wakefield 667–10ABPP heat sink are shown in Figure 5. Note that at narrow pulse widths the two curves are very similar, as there is insufficient time to transfer enough power into the heat sink to raise its temperature. At about 0.3 seconds, the two curves begin to diverge as the temperature of the Wakefield heat sink begins to rise while the water cooled heat sink maintains a steady case temperature.

RC networks for both thermal circuits are included in Figure 5. They were automatically generated by the Analysis Tech Phase 9. Off the shelf programs such as Sauna™ can extract the thermal Rs and Cs from transient thermal response curves. The dashed lines, which are for the most part hidden by the empirical data points, indicate the response of the suggested RC equivalent networks.

Note that the final data point is taken around 600 s, before the MOSFET/Wakefield heat sink system is completely stable. At the time of the test this was thought to be the pulse width limitation of the tester. (The actual limitation is 10,000 seconds.) An alternate test using simple equipment that is only good for steady state produced a reading of 18.1°C/W for the total thermal resistance from junction to ambient. Therefore, in the final model of the MOSFET/ Wakefield heat sink, Rth_3 was changed from 11.44 to 15.66°C/W. (The Wakefield 667–10ABPP is specified to be 12.66°C/W in still air at 6 W.)

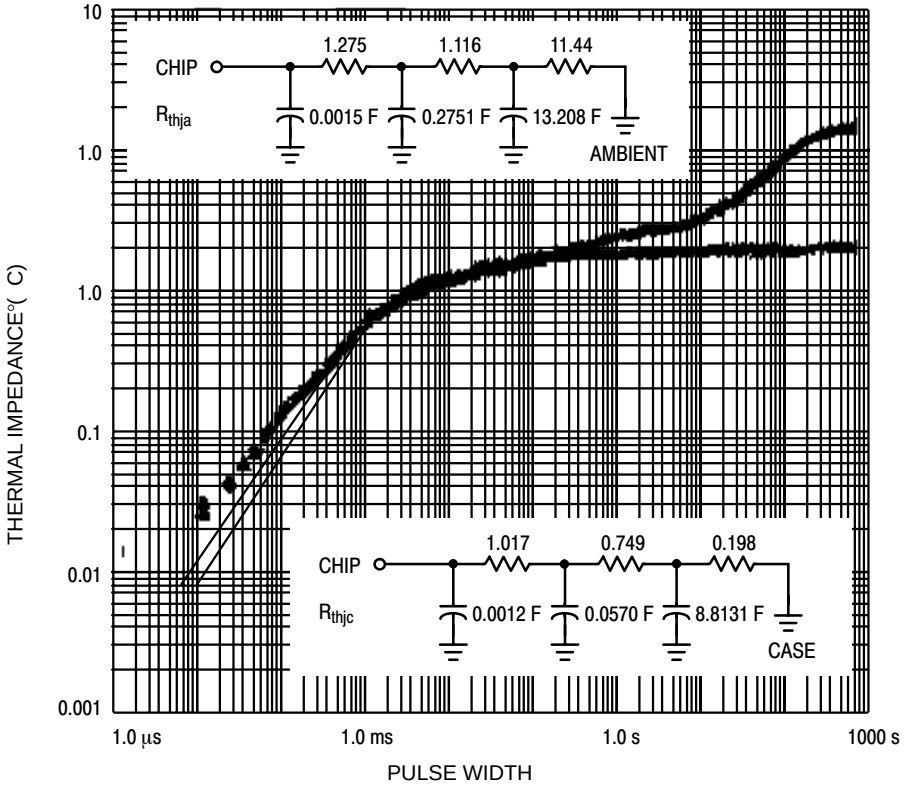


Figure 5. Thermal response of the MOSFET on a water cooled heatsink and on a Wakefield heatsink.

Figure 6 shows the entire thermal/electrical system. The MOSFET's gate was driven by a 10 V, 100 Hz, 50% duty cycle voltage source. A brute force attempt at simulating hundreds of seconds of operation unveils a limitation of the tools and this methodology. The simulation proceeds rapidly as long as the MOSFET is on or off, but during switching, the simulator slows down to accurately model the transitions. Even though the circuit is very simple and the switching frequency is low by most standards, it took several minutes on an HP 9000 Model 735 to simulate each second of operation. To get useful data without excessive simulation times, the simulation was conducted in two runs, one to obtain the circuit's response during the first fourteen seconds and the other to determine its steady state response.

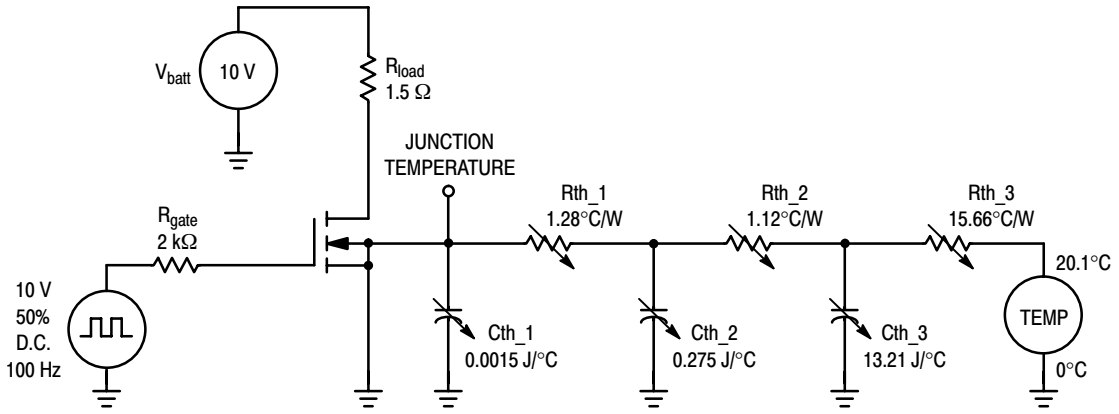


Figure 6. Schematic of electrical/thermal system. The values of the discrete thermal Rs and Cs shown are chosen to give a response most similar to that of the system's distributed elements.

Figure 7 shows the junction temperature variation during the first 1.1 s of operation. Two features are clear: the junction temperature swings about five degrees each period and the average temperature within a cycle begins to increase more slowly at around 300 ms as the heat sink's large thermal capacitance comes into play. The junction temperature during the first 14 seconds of simulation is shown in Figure 8. The junction temperature swing within a cycle, the rise in the average temperature during the first second, and the gradual rise thereafter are controlled by the three thermal capacitances.

Figure 9 shows the temperature appearing at Cth_2 and Cth_3. This graph clearly illustrates the initial charging of the heat sink's large thermal capacity. It also shows that temperature ripple on Cth_2 is in the 0.1°C range and that there is essentially no ripple on Cth_3. Heat flow from the heat sink and into the environment is shown in Figure 10. As would be excepted, no heat flows initially and heat flow steadily increases as the heat sink's temperature rises.

A test lasting 14 seconds lends itself to methods of verification. A thermocouple placed on the MOSFET's tab read 25.0°C at 14 seconds. The model's discrete thermal capacitances and resistances are chosen to provide a response similar to the actual response of the distributed Rs and Cs of the heat sink. They do not represent physically discrete capacitances associated with specific elements of the circuit. Therefore, the tab temperature should not be expected to be equal to the temperature appearing at any of the three thermal capacitances. However, the change in the tab temperature can be tracked, and it should follow the temperature rise of the body of the MOSFET and the heat sink. That indeed proves to be the case, because between 5 and 14 seconds the simulated tab temperature increases at the same rate as the temperature of Cth_2 and Cth_3.

A second simulation and an alternate method is needed to get results at steady state without very long simulation times. The trick is to decrease the size of the thermal capacitances so that they are more easily charged to their final temperatures. Keeping some thermal capacity in the system keeps the junction temperature from swinging wildly with variations in power dissipation. Without any capacitance, variations in power dissipation generate unrealistically large swings about the steady state value. These swings might be high enough to cause problems in the simulation. The waveforms in Figure 11 represent the system's performance with Cth_2 set to 0.03°J/C and Cth_3 set to zero. The steady state value of the empirical test was 63.4 degrees, which matches very well with the simulation.

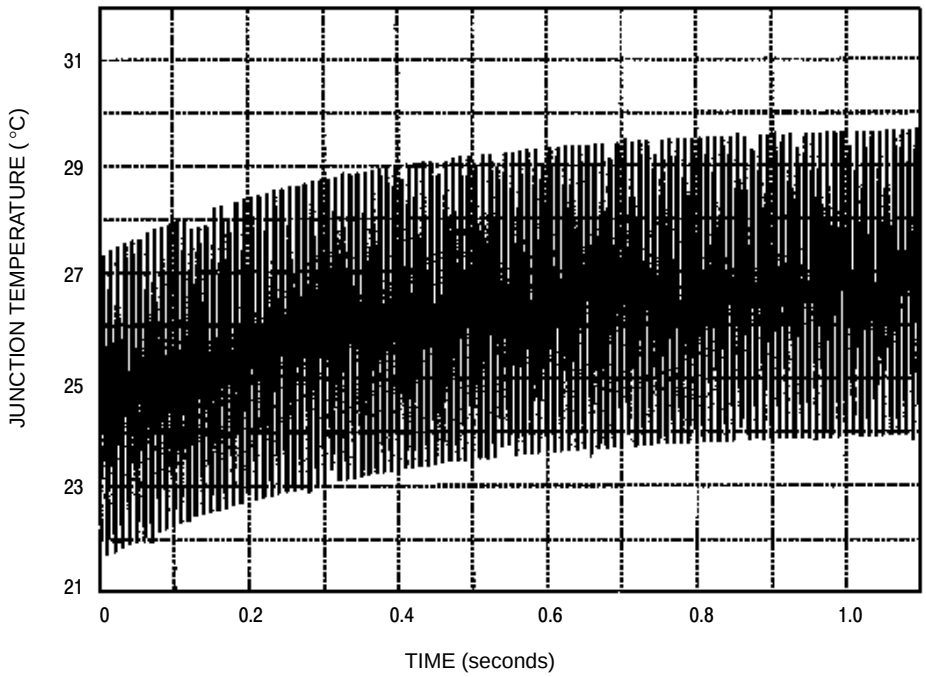


Figure 7. Junction temperature during the first 1.1 seconds of operation

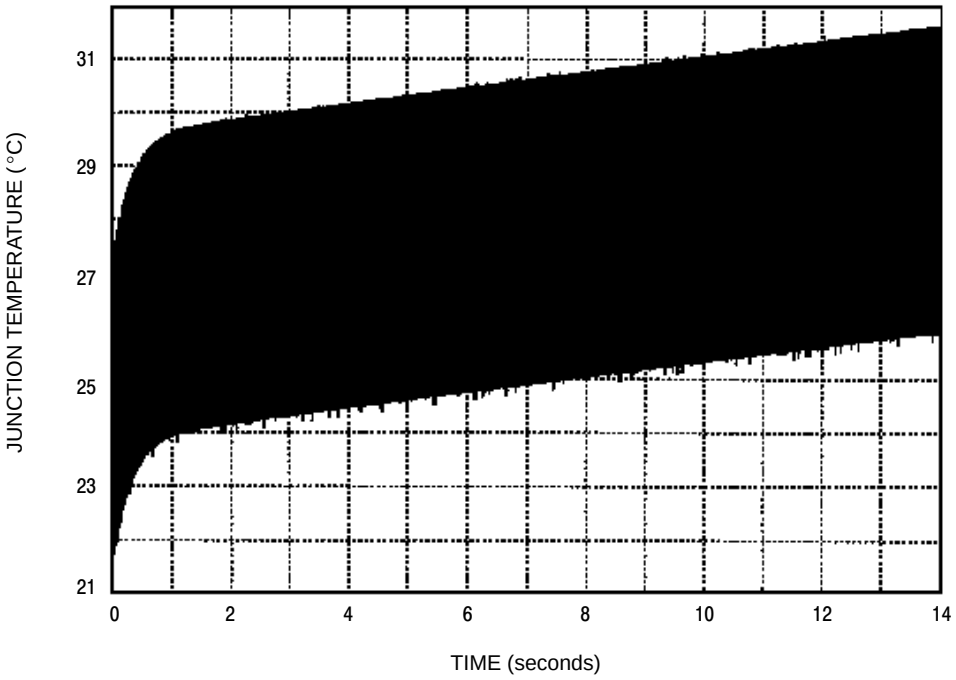


Figure 8. Junction temperature during the first 14 seconds of operation

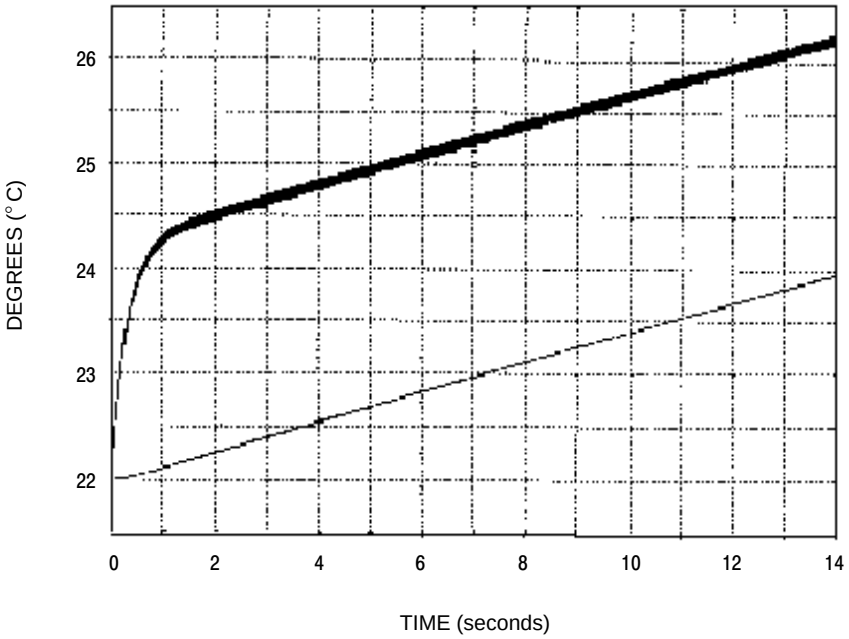


Figure 9. Temperature rise at Cth_2 and Cth_3 clearly show the different thermal time constants that make up the thermal response

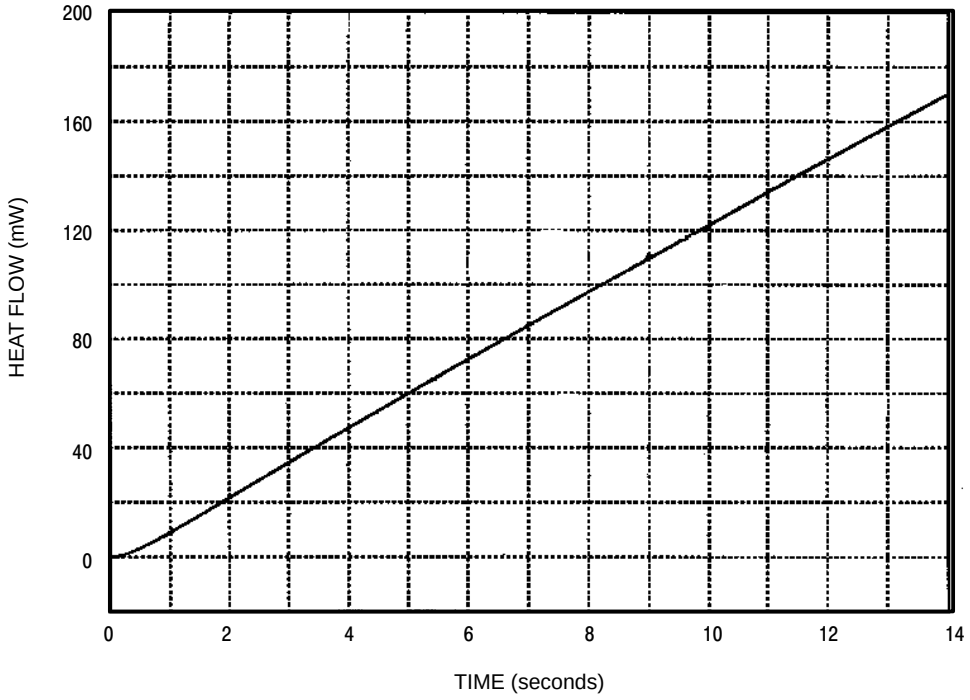


Figure 10. Simulation shows that little heat flows into the environment during the first 14 seconds of operation.

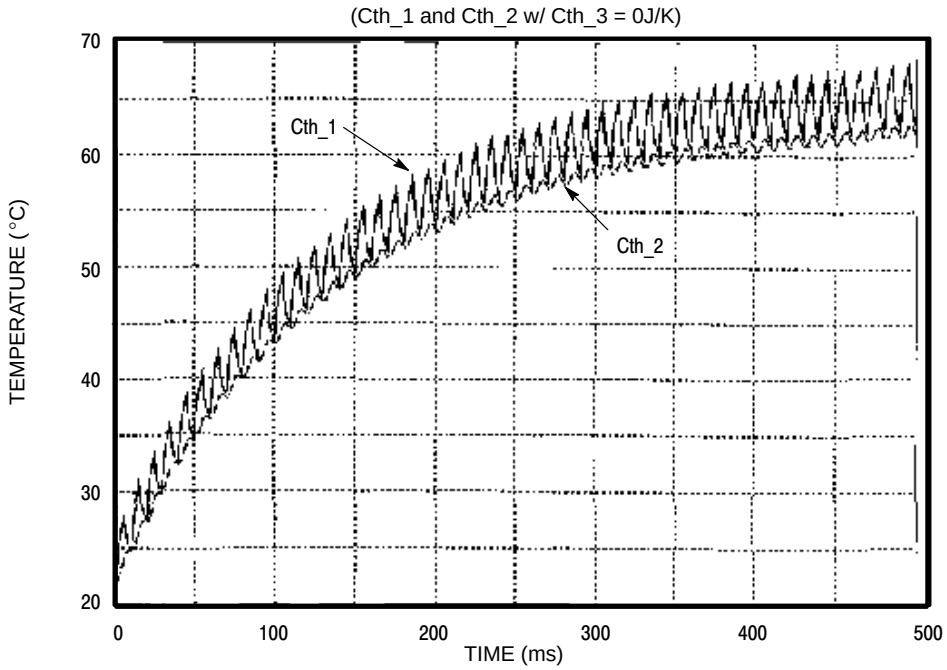


Figure 11. Dramatically reducing the size of the largest thermal capacitances allows the simulator to quickly find solutions for steady state conditions.

Other Tips

When using Analogy's SABER program, it is good to know how the program assigns default values of thermal resistance. The program looks to see if the user specifies Rth_hs or Rth_jc. If the user defines Rth_hs, SABER uses that value and the value of Rth_jc specified on the manufacturer's data sheet. If Rth_hs is not specified, SABER uses the value of Rth_ja specified on the manufacturer's data sheet in place of Rth_jc and Rth_hs. Rth_ja is the device's junction to ambient thermal resistance without a heat sink, and its value for a TO–220, for example, is quite large, 62.5°C/W. Defaulting to such a large thermal resistance might cause unrealistic junction temperatures and invalid results or even convergence problems.

In release 4.0 of SABER, Analogy's thermal models do not contain thermal capacitance. To add your own thermal network, including thermal capacitance, set the MOSFET's Rth_hs and Rth_jc to very small values (0.001 °C/W was used in these simulations) and then add your own thermal network, including thermal capacitances and thermal resistances.

SUMMARY

The tools and techniques described here proved to be an effective means of predicting power transistor junction temperature of two different MOSFETs operating in three types of circuits with two different heat sinks. This methodology is also useful for understanding how circuit performance varies with changes in the power transistor, the thermal interface between it and the heat sink, and the heatsink itself. The uniqueness of the approach is the use of a combination of newly developed tools, all of which are readily available to the power electronics community.

ACKNOWLEDGMENTS

Special thanks to Gary Dashney, Tanya Fowler, and Larry Walker of ON Semiconductor for developing the technique of measuring transient thermal response of systems with very long thermal response times and for characterizing the MOSFET/heatsink assembly used in this study.

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Transient Thermal Resistance of Semiconductor Packages

Edited and Updated

USING TRANSIENT THERMAL RESISTANCE DATA IN HIGH POWER PULSED THYRISTOR APPLICATIONS

INTRODUCTION

For a certain amount of dc power dissipated in a semiconductor, the junction temperature reaches a value which is determined by the thermal conductivity from the junction (where the power is dissipated) to the air or heat sink. When the amount of heat generated in the junction equals the heat conducted away, a steady–state condition is reached and the junction temperature can be calculated by the simple equation:

$$T_J = P_D R_{\theta JR} + T_R \quad (1a)$$

where T_J = junction temperature
T_R = temperature at reference point
P_D = power dissipated in the junction
$R_{\theta JR}$ = steady–state thermal resistance from junction to the temperature reference point.

Power ratings of semiconductors are based upon steady–state conditions, and are determined from equation (1a) under worst case conditions, i.e.:

$$P_{D(max)} = \frac{T_{J(max)} - T_R}{R_{\theta JR(max)}} \quad (1b)$$

$T_{J(max)}$ is normally based upon results of an operating life test or serious degradation with temperature of an important device characteristic. T_R is usually taken as 25°C, and $R_{\theta JR}$ can be measured using various techniques. The reference point may be the semiconductor case, a lead, or the ambient air, whichever is most appropriate. Should the reference temperature in a given application exceed the reference temperature of the specification, P_D must be correspondingly reduced.

Thermal resistance allows the designer to determine power dissipation under steady state conditions. Steady state conditions between junction and case are generally achieved in one to ten seconds while minutes may be required for junction to ambient temperature to become stable. However, for pulses in the microsecond and millisecond region, the use of steady–state values will not yield true power capability because the thermal response of the system has not been taken into account.

Note, however, that semiconductors also have pulse power limitations which may be considerably lower – or even greater – than the allowable power as deduced from thermal response information. For transistors, the second breakdown portion of the pulsed safe operating area defines power limits while surge current or power ratings are given for diodes and thyristors. These additional ratings must be used in conjunction with the thermal response to determine power handling capability.

To account for thermal capacity, a time dependent factor r(t) is applied to the steady–state thermal resistance. Thermal resistance, at a given time, is called transient thermal resistance and is given by:

$$R_{\theta JR(t)} = r(t) \cdot R_{\theta JR} \quad (2)$$

The mathematical expression for the transient thermal resistance has been determined to be extremely complex. The response is, therefore, plotted from empirical data. Curves, typical of the results obtained, are shown in Figure 1. These curves show the relative thermal response of the junction, referenced to the case, resulting from a step function change in power. Observe that the total percentage difference is about 10:1 in the short pulse ($\sqrt{t}$) region. However, the values of thermal resistance vary over 20:1.

Many ON Semiconductor data sheets have a graph similar to that of Figure 2. It shows not only the thermal response to a step change in power (the D = 0, or single pulse curve) but also has other curves which may be used to obtain an effective r(t) value for a train of repetitive pulses with different duty cycles. The mechanics of using the curves to find T_J at the end of the first pulse in the train, or to find $T_{J(pk)}$ once steady state conditions have been achieved, are quite simple and require no background in the subject. However, problems where the applied power pulses are either not identical in amplitude or width, or the duty cycle is not constant, require a more thorough understanding of the principles illustrated in the body of this report.

USE OF TRANSIENT THERMAL RESISTANCE DATA

Part of the problem in applying thermal response data stems from the fact that power pulses are seldom rectangular, therefore to use the r(t) curves, an equivalent rectangular model of the actual power pulse must be determined. Methods of doing this are described near the end of this note.

Before considering the subject matter in detail, an example will be given to show the use of the thermal response data sheet curves. Figure 2 is a representative graph which applies to a 2N5886 transistor.

Pulse power P_D = 50 Watts
Duration t = 5 milliseconds
Period τ_p = 20 milliseconds
Case temperature, T_C = 75°C
Junction to case thermal resistance,
$R_{\theta JC}$ = 1.17°C/W

The temperature is desired, a) at the end of the first pulse b) at the end of a pulse under steady state conditions.

For part (a) use:

$$T_J = r(5\ ms)\ R_{\theta JC} P_D + T_C$$

The term r(5 ms) is read directly from the graph of Figure 2 using the D = 0 curve,

$$\therefore T_J = 0.49 \times 1.17 \times 50 + 75 = 28.5 + 75 = 103.5$$

The peak junction temperature rise under steady conditions is found by:

$$T_J = r(t, D)\ R_{\theta JC}\ P_D + T_C$$

$D = t/\tau_p = 5/20 – 0.25$. A curve for D= 0.25 is not on the graph; however, values for this duty cycle can be interpolated between the D = 0.2 and D = 0.5 curves. At 5 ms, read $r(t) \approx 0.59$.

$$T_J = 0.59 \times 1.17 \times 50 + 75 = 34.5 + 75 = 109.5°C$$

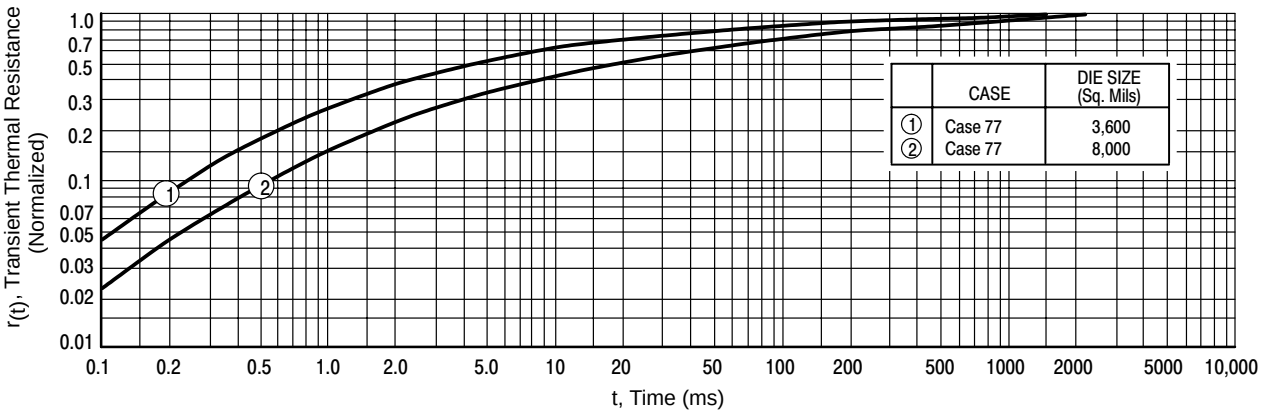


Figure 1. Thermal Response, Junction to Case, of Case 77 Types For a Step of Input Power

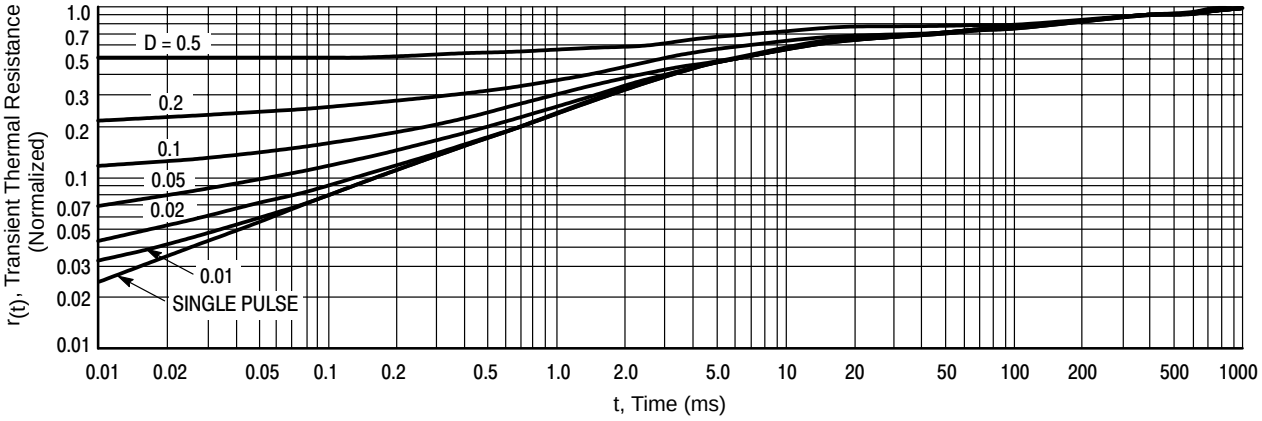


Figure 2. Thermal Response Showing the Duty Cycle Family of Curves

The average junction temperature increase above ambient is:

$$T_{J(average)} - T_C = R_{\theta JC} P_D D$$
$$= (1.17)\ (50)\ (0.25) \qquad (3)$$
$$= 14.62°C$$

Note that T_J at the end of any power pulse does not equal the sum of the average temperature rise (14.62°C in the example) and that due to one pulse (28.5°C in example), because cooling occurs between the power pulses.

While junction temperature can be easily calculated for a steady pulse train where all pulses are of the same amplitude and pulse duration as shown in the previous example, a simple equation for arbitrary pulse trains with random variations is impossible to derive. However, since the heating and cooling response of a semiconductor is essentially the same, the superposition principle may be used to solve problems which otherwise defy solution.

Using the principle of superposition each power interval is considered positive in value, and each cooling interval negative, lasting from time of application to infinity. By multiplying the thermal resistance at a particular time by the magnitude of the power pulse applied, the magnitude of the junction temperature change at a particular time can be obtained. The net junction temperature is the algebraic sum of the terms.

The application of the superposition principle is most easily seen by studying Figure 3.

Figure 3(a) illustrates the applied power pulses. Figure 3(b) shows these pulses transformed into pulses lasting from time of application and extending to infinity; at t_o, P_1 starts and extends to infinity; at t_1, a pulse ($-P_1$) is considered to be present and thereby cancels P_1 from time t_1, and so forth with the other pulses. The junction temperature changes due to these imagined positive and negative pulses are shown in Figure 3(c). The actual junction temperature is the algebraic sum as shown in Figure 3(d).

Problems may be solved by applying the superposition principle exactly as described; the technique is referred to as Method 1, the pulse–by–pulse method. It yields satisfactory results when the total time of interest is much less than the time required to achieve steady state conditions, and must be used when an uncertainty exists in a random pulse train as to which pulse will cause the highest temperature. Examples using this method are given in Appendix A under Method 1.

For uniform trains of repetitive pulses, better answers result and less work is required by averaging the power pulses to achieve an average power pulse; the temperature is calculated at the end of one or two pulses following the average power pulse. The essence of this method is shown in Figure 6. The duty cycle family of curves shown in Figure 2 and used to solve the example problem is based on this method; however, the curves may only be used for a uniform train after steady state conditions are achieved. Method 2 in Appendix A shows equations for calculating the temperature at the end of the n_{th} or n + 1 pulse in a uniform train. Where a duty cycle family of curves is available, of course, there is no need to use this method.

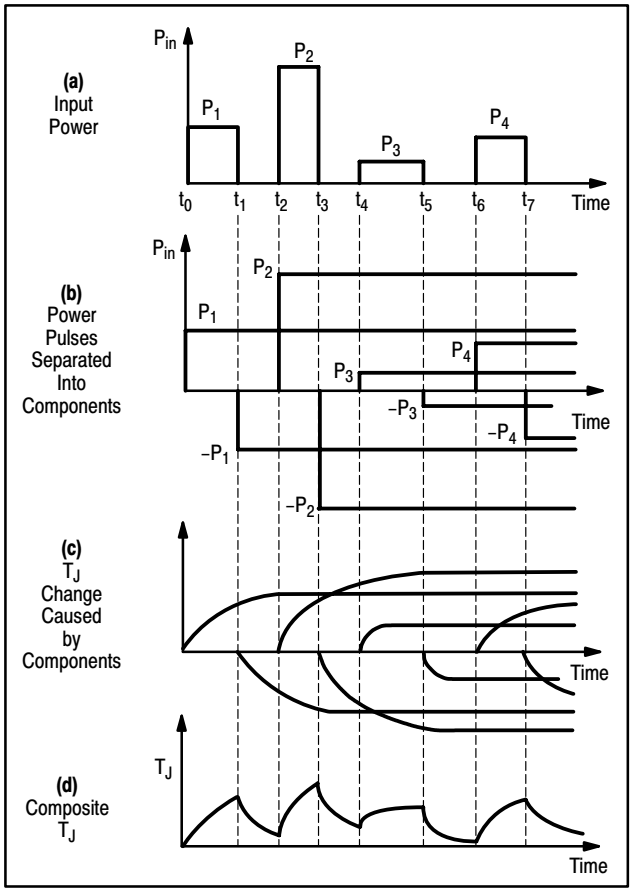


Figure 3. Application of Superposition Principle

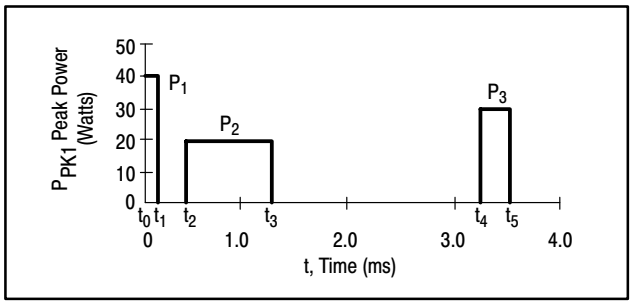


Figure 4. Non–Repetitive Pulse Train (Values Shown Apply to Example in Appendix)

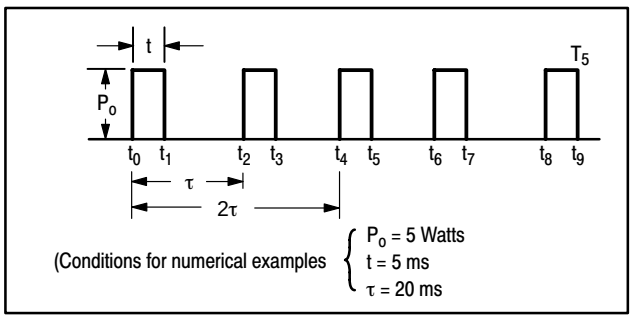


Figure 5. A Train of Equal Repetitive Pulses

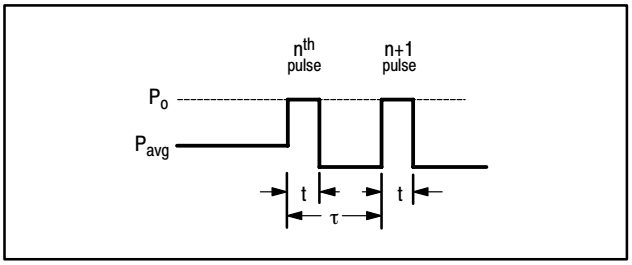


Figure 6. Model For a Repetitive Equal Pulse Train

Temperature rise at the end of a pulse in a uniform train before steady state conditions are achieved is handled by Method 3 (a or b) in the Appendix. The method is basically the same as for Method 2, except the average power is modified by the transient thermal resistance factor at the time when the average power pulse ends.

A random pulse train is handled by averaging the pulses applied prior to situations suspected of causing high peak temperatures and then calculating junction temperature at the end of the n_{th} or n + 1 pulse. Part c of Method 3 shows an example of solving for temperature at the end of the 3rd pulse in a three pulse burst.

HANDLING NON–RECTANGULAR PULSES

The thermal response curves, Figure 1, are based on a step change of power; the response will not be the same for other waveforms. Thus far in this treatment we have assumed a rectangular shaped pulse. It would be desirable to be able to obtain the response for any arbitrary waveform, but the mathematical solution is extremely unwieldy. The simplest approach is to make a suitable equivalent rectangular model of the actual power pulse and use the given thermal response curves; the primary rule to observe is that the energy of the actual power pulse and the model are equal.

Experience with various modeling techniques has lead to the following guidelines:

For a pulse that is nearly rectangular, a pulse model having an amplitude equal to the peak of the actual pulse, with the width adjusted so the energies are equal, is a conservative model. (See Figure 7(a)).

Sine wave and triangular power pulses model well with the amplitude set at 70% of the peak and the width adjusted to 91% and 71%, respectively, of the baseline width (as shown on Figure 7(b)).

A power pulse having a $\sin^2$ shape models as a triangular waveform.

Power pulses having more complex waveforms could be modeled by using two or more pulses as shown in Figure 7(c).

A point to remember is that a high amplitude pulse of a given amount of energy will produce a higher rise in junction temperature than will a lower amplitude pulse of longer duration having the same energy.

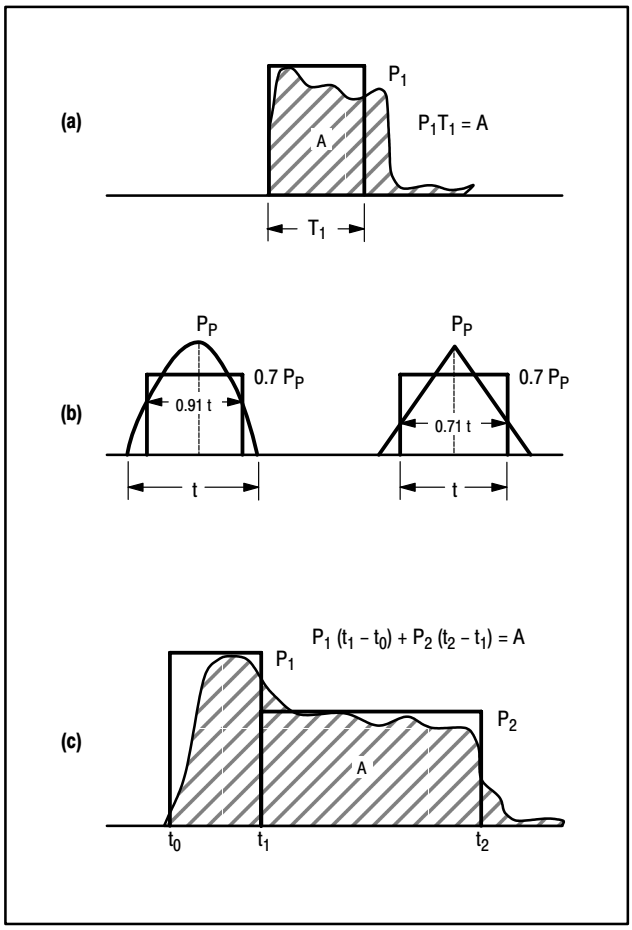


Figure 7. Modeling of Power Pulses

As an example, the case of a transistor used in a dc to ac power converter will be analyzed. The idealized waveforms of collector current, I_C, collector to emitter voltage, V_{CE}, and power dissipation P_D, are shown in Figure

A model of the power dissipation is shown in Figure 8(d). This switching transient of the model is made, as was suggested, for a triangular pulse.

For example, T_J at the end of the rise, on, and fall times, T_1, T_2 and T_3 respectively, will be found.

Conditions:

TO–3 package,

$R_{\theta JC}$ = 0.5°C/W, I_C = 60A, $V_{CE(off)}$ = 60 V
T_A = 50°C
t_f = 80 μs, t_r = 20 μs
$V_{CE(sat)}$ = 0.3 V @ 60 A
Frequency = 2 kHz ∴ τ = 500 μs
P_{on} = (60) (0.3) = 18 W
P_f = 30 × 30 = 900 W = P_r

Assume that the response curve in Figure 1 for a die area of 58,000 square mils applies. Also, that the device is mounted on an MS–15 heat sink using Dow Corning DC340 silicone compound with an air flow of 1.0 lb/min flowing across the heat–sink. (From MS–15 Data Sheet, $R_{\theta CS}$ = 0.1°C/W and $R_{\theta SA}$ = 0.55°C/W).

Procedure: Average each pulse over the period using equation 1–3 (Appendix A, Method 2), i.e.,

$$P_{avg} = 0.7\,P_r\,0.71\,\frac{t_r}{\tau} + Pon\,\frac{ton}{\tau} + 0.7\,P_f\,0.71\,\frac{t_f}{\tau}$$

$$= (0.7)(900)(0.71)\,\frac{(20)}{500} + (18)\,\frac{(150)}{500}$$

$$+ (0.7)(900)(0.71)\,\frac{80}{500}$$

$$= 17.9 + 5.4 + 71.5$$

$$= 94.8\ W$$

From equation 1–4, Method 2A:

$$T_1 = [P_{avg} + (0.7\,P_r - P_{avg}) \cdot r(t_1 - t_o)]\,R_{\theta JC}$$

At this point it is observed that the thermal response curves of Figure 1 do not extend below 100 μs. Heat transfer theory for one dimensional heat flow indicates that the response curve should follow the $\sqrt{t}$ law at small times. Using this as a basis for extending the curve, the response at 14.2 μs is found to be 0.023.

We then have:

$$T_1 = [94.8 + (630 - 94.8).023]\,(0.5)$$

$$= (107.11)(0.5) = 53.55°C$$

For T_2 we have, by using superposition:

$$T_2 = [P_{avg} - P_{avg} \cdot r(t_2 - t_o) + 0.7\,P_r \cdot r(t_2 - t_o) - 0.7\,P_r \cdot r(t_2 - t_1) + Pon \cdot r(t_2 - t_1)]\,R_{\theta JC}$$

$$= [P_{avg} + (0.7\,P_r - P_{avg}) \cdot r(t_2 - t_o) + (Pon - 0.7\,P_r) \cdot r(t_2 - t_1)]\,R_{\theta JC}$$

$$= [94.8 + (630 - 94.8) \cdot r(164\ \mu s) + (18 - 630) \cdot r(150\ \mu s)]\,(0.5)$$

$$= [94.8 + (535.2)(.079) - (612)(.075)]\,(0.5)$$

$$= [94.8 + 42.3 - 45.9]\,(0.5)$$

$$= (91.2)(0.5) = 45.6°C$$

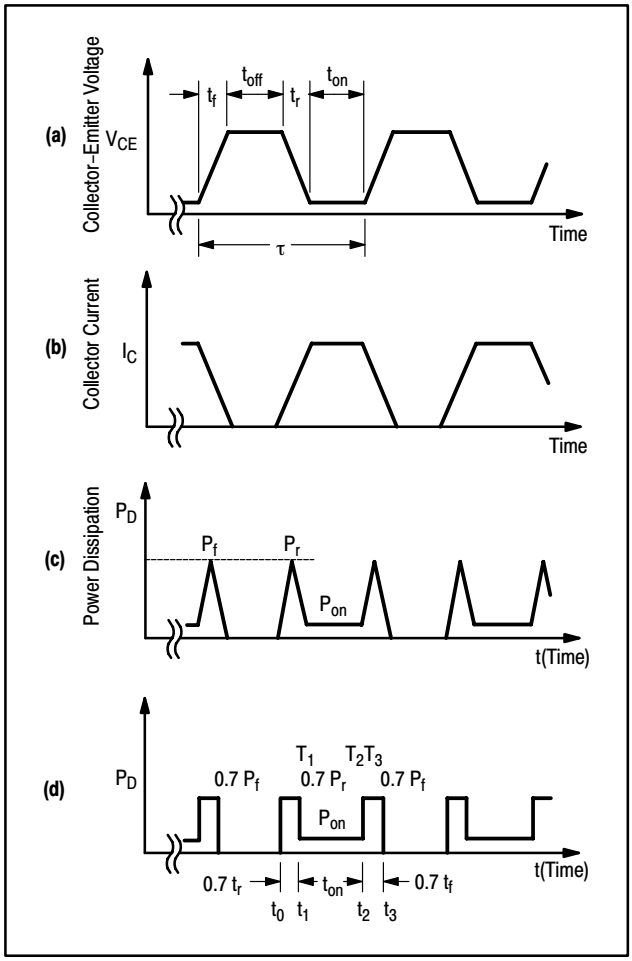


Figure 8. Idealized Waveforms of I_C, V_{CE} and P_D in a DC to AC Inverter

For the final point T_3 we have:

$$T_3 = [P_{avg} - P_{avg} \cdot r(t_3 - t_o) + 0.7\,P_r \cdot r(t_3 - t_o) - 0.7\,P_r \cdot r(t_3 - t_1) + Pon \cdot r(t_3 - t_1) - Pon \cdot r(t_3 - t_2) + 0.7\,P_f \cdot r(t_3 - t_2)]\,R_{\theta JC}$$

$$[P_{avg} + (0.7\,P_r - Pavg) \cdot r(t_3 - t_o) + (Pon - 0.7\,P_r) \cdot r(t_3 - t_1) + (0.7\,P_f - Pon) \cdot r(t_3 - t_2)]\,R_{\theta JC}$$

$$= [94.8 + (535.2) \cdot r(221\ \mu s) + (-612) \cdot r(206.8\ \mu s) + (612) \cdot r(56.8 \mu s)]\,(0.5)$$

$$= [94.8 + (535.2)(0.09) - (612)\,(0.086) + (612)(0.045)]\,(0.5)$$

$$= [94.8 + 481.7 - 52.63 + 27.54]\,(0.5)$$

$$= (117.88)(0.5) = 58.94°C$$

The junction temperature at the end of the rise, on, and fall times, T_{J1}, T_{J2}, and T_{J3}, is as follows:

$$T_{J1} = T_1 + T_A + R_{\theta CA} \cdot P_{avg}$$
$$R_{\theta CA} = R_{\theta CS} = R_{\theta SA} = 0.1 + 0.55$$
$$T_{J1} = 53.55 + 50 + (0.65)(94.8) = 165.17°C$$
$$T_{J2} = T_2 + T_A + R_{\theta CA} \cdot P_{avg}$$
$$= 45.6 + 50 + (0.65)(94.8)$$
$$= 157.22°C$$
$$T_{J3} = T_3 + T_A + R_{\theta CA} \cdot P_{avg}$$
$$= 58.94 + 50 + (0.65)(94.8)$$
$$= 170.56°C$$
$$T_{J(avg)} = P_{avg} (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A$$
$$= (94.8)(0.5 + 0.1 + 0.55) + 50$$
$$= (94.8)(1.15) + 50 = 159.02°C$$

Inspection of the results of the calculations T_1, T_2, and T_3 reveal that the term of significance in the equations is the average power. Even with the poor switching times there was a peak junction temperature of 11.5°C above the average value. This is a 7% increase which for most applications could be ignored, especially when switching times are considerably less. Thus the product of average power and steady state thermal resistance is the determining factor for junction temperature rise in this application.

SUMMARY

This report has explained the concept of transient thermal resistance and its use. Methods using various degrees of approximations have been presented to determine the junction temperature rise of a device. Since the thermal response data shown is a step function response, modeling of different wave shapes to an equivalent rectangular pulse of pulses has been discussed.

The concept of a duty cycle family of curves has also been covered; a concept that can be used to simplify calculation of the junction temperature rise under a repetitive pulse train.

APPENDIX A METHODS OF SOLUTION

In the examples, a type 2N3647 transistor will be used; its steady state thermal resistance, $R_{\theta JC}$, is 35°C/W and its value for r(t) is shown in Figure A1.

Definitions:

P_1, P_2, P_3 ... P_n = power pulses (Watts)

T_1, T_2, T_3 ... T_n = junction to case temperature at end of P_1, P_2, P_3 ... P_n

t_0, t_1, t_2, ... t_n = times at which a power pulse begins or ends

$r(t_n - t_k)$ = transient thermal resistance factor at end of time interval $(t_n - t_k)$.

Table 1. Several Possible Methods of Solutions

1. Junction Temperature Rise Using Pulse–By–Pulse Method
   - A. Temperature rise at the end of the n_{th} pulse for pulses with unequal amplitude, spacing, and duration.
   - B. Temperature rise at the end of the n_{th} pulse for pulses with equal amplitude, spacing, and duration.
2. Temperature Rise Using Average Power Concept Under Steady State Conditions For Pulses Of Equal Amplitude, Spacing, And Duration
   - A. At the end of the n_{th} pulse.
   - B. At the end of the (n + 1) pulse.
3. Temperature Rise Using Average Power Concept Under Transient Conditions.
   - A. At the end of the n_{th} pulse for pulses of equal amplitude, spacing and duration.
   - B. At the end of the n + 1 pulse for pulses of equal amplitude, spacing and duration.
   - C. At the end of the n_{th} pulse for pulses of unequal amplitude, spacing and duration.
   - D. At the end of the n + 1 pulse for pulses of unequal J amplitude, spacing and duration.

METHOD 1A – FINDING T_J AT THE END OF THE Nth PULSE IN A TRAIN OF UNEQUAL AMPLITUDE, SPACING, AND DURATION

General Equation:

$$T_n = \sum_{i=1}^{n} P_i [r(t_{2n-1} - t_{2i-2}) - r(t_{n-1} - t_{2i-1})] R_{\theta JC} \quad (1–1)$$

where n is the number of pulses and P_i is the peak value of the i^{th} pulse.

To find temperature at the end of the first three pulses, Equation 1–1 becomes:

$$T_1 = P_1 r(t_1) R_{\theta JC} \quad (1–1A)$$
$$T_2 = [P_1 r(t_3) – P_1 r(t_3 – t_1) + P_2 r(t_3 – t_2)] R_{\theta JC} \quad (1–1B)$$
$$T_3 = [P_1 r(t_5) – P_1 r(t_5 – t_1) + P_2 r(t_5 – t_2) – P_2 r(t_5 – t_3) + P_3 r(t_5 – t_4)] R_{\theta JC} \quad (1–1C)$$

Example:

Conditions are shown on Figure 4 as:

P_1 = 40 W	t_0 = 0	t_3 = 1.3 ms
P_2 = 20 W	t_1 = 0.1 ms	t_4 = 3.3 ms
P_3 = 30 W	t_2 = 0.3 ms	t_5 = 3.5 ms

Therefore,

$t_1 - t_0 = 0.1$ ms $t_3 - t_1 = 1.2$ ms
$t_2 - t_1 = 0.2$ ms $t_5 - t_1 = 3.4$ ms
$t_3 - t_2 = 1$ ms $t_5 - t_2 = 3.2$ ms
$t_4 - t_3 = 2$ ms $t_5 - t_3 = 2.2$ ms
$t_5 - t_4 = 0.2$ ms

Procedure:

Find $r(t_n - t_k)$ for preceding time intervals from Figure 2, then substitute into Equations 1–1A, B, and C.

$$T_1 = P_1\, r(t_1)\, R_{\theta JC} = 40 \cdot 0.05 \cdot 35 = 70°C$$

$$T_2 = [P_1\, r(t_3) - P_1\, r(t_3 - t_1) + P_2\, r(t_3 - t_2)]\, R_{\theta JC}$$
$$= [40\,(0.175) - 40\,(0.170) + 20\,(0.155)]\,35$$
$$= [40\,(0.175 - 0.170) + 20\,(0.155)]\,35$$
$$= [0.2 + 3.1]\,35 = 115.5°C$$

$$T_3 = [P_1\, r(t_5) - P_1\, r(t_5 - t_1) + P_2\, r(t_5 - t_2) - P_2\, r(t_5 - t_3) + P_3\, r(t_5 - t_4)]\, \theta_{JC}$$
$$T_3 = [40\,(0.28) - 40\,(0.277) + 20\,(0.275) - 20\,(0.227) + 30\,(0.07)]\,35$$
$$= [40\,(0.28 - 0.277) + 20\,(0.275 - 0.227) + 30\,(0.07)]\,35$$
$$= [0.12 + 0.96 + 2.1]\dagger\,35 = 3.18 \cdot 35 = 111.3°C$$

Note, by inspecting the last bracketed term in the equations above that very little residual temperature is left from the first pulse at the end of the second and third pulse. Also note that the second pulse gave the highest value of junction temperature, a fact not so obvious from inspection of the figure. However, considerable residual temperature from the second pulse was present at the end of the third pulse.

METHOD 1B – FINDING T_J AT THE END OF THE Nth PULSE IN A TRAIN OF EQUAL AMPLITUDE, SPACING, AND DURATION

The general equation for a train of equal repetitive pulses can be derived from Equation 1–1. $P_i = P_D$, $t_i = t$, and the spacing between leading edges or trailing edges of adjacent pulses is τ.

General Equation:

$$T_n = P_D R_{\theta JC} \sum_{i=1}^{n} r[(n - i)\,\tau + t] - r[(n - i)\,\tau] \qquad (1–2)$$

Expanding:

$$T_n = P_D\, R_{\theta JC}\, r[(n-1)\,\tau + t] - r[(n-1)\,\tau] + r[(n-2)\,\tau + t) - r[(n-2)\,\tau] + r[(n-3)\,\tau + t] - r[(n-3)\,\tau] + \ldots + r[(n-i)\,\tau + t] - r[(n-i)\,\tau] \ldots\ldots + r(t)] \qquad (1–2A)$$

†Relative amounts of temperature residual from P_1, P_2, and P_3 respectively are indicated by the terms in brackets.

For 5 pulses, equation 1–2A is written:

$$T_5 = P_D\, R_{\theta JC}\, [r(4\,\tau + t) - r(4\tau) + r(3\tau + t)] - r(3\tau) + r(2\tau + t) - r(2\tau) + r(\tau + t) - r(\tau) + r(t)]$$

Example:

Conditions are shown on Figure 5 substituting values into the preceding expression:

$$T_5 = (5)\,(35)\,[r(4.20 + 5) - r(4.20) + r(3.20 + 5) + r(3.20) + r(2.20 + 5) - r(2.20) + r(20 + 5) - r(20) + r(5)]$$
$$T_5 = (5)\,(35)\,[0.6 - 0.76 + 0.73 - 0.72 + 0.68 - 0.66 + 0.59 - 0.55 + 0.33] - (5)(35)(0.40)$$
$$T_5 = 70.0°C$$

Note that the solution involves the difference between terms nearly identical in value. Greater accuracy will be obtained with long or repetitive pulse trains using the technique of an average power pulse as used in Methods 2 and 3.

METHOD 2 – AVERAGE POWER METHOD, STEADY STATE CONDITION

The essence of this method is shown in Figure 6. Pulses previous to the n_{th} pulse are averaged. Temperature due to the n_{th} or n + 1 pulse is then calculated and combined properly with the average temperature.

Assuming the pulse train has been applied for a period of time (long enough for steady state conditions to be established), we can average the power applied as:

$$P_{avg} = P_D \frac{t}{\tau} \qquad (1–3)$$

METHOD 2A – FINDING TEMPERATURE AT THE END OF THE N_{th} PULSE

Applicable Equation:

$$T_n = [P_{avg} + (P_D - P_{avg})\, r(t)]\, R_{\theta JC} \qquad (1–4)$$

or, by substituting Equation 1–3 into 1–4,

$$Tn = \left[\frac{t}{\tau} + \left(1 - \frac{t}{\tau}\right) r(t)\right] P_D\, R_{\theta JC} \qquad (1–5)$$

The result of this equation will be conservative as it adds a temperature increase due to the pulse $(P_D - P_{avg})$ to the average temperature. The cooling between pulses has not been accurately accounted for; i.e., T_J must actually be less than $T_{J(avg)}$ when the n^{th} pulse is applied.

Example: Find T_n for conditions of Figure 5.
Procedure: Find P_{avg} from equation (1–3) and substitute values in equation (1–4) or (1–5).

$$T_n = [(1.25) + (5.0 - 1.25)(0.33)]\,(35)$$
$$= 43.7 + 43.2 = 86.9°C$$

METHOD 2B – FINDING TEMPERATURE AT THE END OF THE N + 1 PULSE

Applicable Equation:

$$T_{n+1} = [P_{avg} + (P_D - P_{avg})\, r(t + \tau) + P_D\, r(t) - P_D\, r(\tau)]\, R_{\theta JC} \qquad (1–6)$$

or, by substituting equation 1–3 into 1–6,

$$T_{n+1} = \left[\frac{t}{\tau} + \left(1 - \frac{t}{\tau}\right) r(t + \tau) + r(t) - r(\tau)\right] P_D R_{\theta JC} \qquad (1–7)$$

Example: Find T_n for conditions of Figure 5.
Procedure: Find P_{avg} from equation (1–3) and substitute into equation (1–6) or (1–7).

$$T_{n+1} = [(1.25) + (5 - 1.25)(0.59) + (5)(0.33) - (5)(0.56)]\,(35) = 80.9°C$$

Equation (1–6) gives a lower and more accurate value for temperature than equation (1–4). However, it too gives a higher value than the true T_J at the end of the n + 1th pulse. The error occurs because the implied value for T_J at the end of the nth pulse, as was pointed out, is somewhat high. Adding additional pulses will improve the accuracy of the calculation up to the point where terms of nearly equal value are being subtracted, as shown in the examples using the pulse by pulse method. In practice, however, use of this method has been found to yield reasonable design values and is the method used to determine the duty cycle of family of curves – e.g., Figure 2.

Note that the calculated temperature of 80.9°C is 10.9°C higher than the result of example 1B, where the temperature was found at the end of the 5th pulse. Since the thermal response curve indicates thermal equilibrium in 1 second, 50 pulses occurring 20 milliseconds apart will be required to achieve stable average and peak temperatures; therefore, steady state conditions were not achieved at the end of the 5th pulse.

METHOD 3 – AVERAGE POWER METHOD, TRANSIENT CONDITIONS

The idea of using average power can also be used in the transient condition for a train of repetitive pulses. The previously developed equations are used but P_{avg} must be modified by the thermal response factor at time $t_{(2n-1)}$.

METHOD 3A – FINDING TEMPERATURE AT THE END OF THE N_{th} PULSE FOR PULSES OF EQUAL AMPLITUDE, SPACING AND DURATION

Applicable Equation:

$$T_n = \left[\frac{t}{\tau} r\, t_{(2n-1)} + \left(1 - \frac{t}{\tau}\right) r(t)\right] P_D R_{\theta JC} \qquad (1–8)$$

Conditions: (See Figure 5)
Procedure: At the end of the 5th pulse (See Figure 7) . . .

$$T_5 = [5/20 \cdot r(85) + (1 - 5/20) r(5)]\,(5)(35) = [(0.25)(0765) + (0.75)(0.33)]\,(175) = 77°C$$

This value is a little higher than the one calculated by summing the results of all pulses; indeed it should be, because no cooling time was allowed between P_{avg} and the nth pulse. The method whereby temperature was calculated at the n + 1 pulse could be used for greater accuracy.

METHOD 3B – FINDING TEMPERATURE AT THE END OF THE N + 1 PULSE FOR PULSES OF EQUAL AMPLITUDE, SPACING AND DURATION

Applicable Equation:

$$T_{n+1} = \left[\frac{t}{\tau} r(t_{2n-1}) + \left(1 - \frac{t}{\tau}\right) r(t + \tau) + r(t) - r(\tau)\right] P_D R_{\theta JC} \qquad (1–9)$$

Example: Conditions as shown on Figure 5. Find temperature at the end of the 5th pulse.

For n + 1 = 5, n = 4, $t_{2n-1} = t_7 = 65$ ms,

$$T_5 = \left[\frac{5}{20} r(65\text{ ms}) + \left(1 - \frac{5}{20}\right) r(25\text{ ms}) + r(5\text{ ms}) - r(20\text{ ms})\right](5)(35)$$

$$T_5 = [(0.25)(0.73) + (0.75)(0.59) + 0.33 - 0.55](5)(35)$$

$$T_5 = 70.8°C$$

The answer agrees quite well with the answer of Method 1B where the pulse–by–pulse method was used for a repetitive train.

METHOD 3C – FINDING T_J AT THE END OF THE N_{th} PULSE IN A RANDOM TRAIN

The technique of using average power does not limit itself to a train of repetitive pulses. It can be used also where the pulses are of unequal magnitude and duration. Since the method yields a conservative value of junction temperature rise it is a relatively simple way to achieve a first approximation. For random pulses, equations 1–4 through 1–7 can be modified. It is necessary to multiply P_{avg} by the thermal response factor at time $t_{(2n-1)}$. P_{avg} is determined by averaging the power pulses from time of application to the time when the last pulse starts.

Applicable Equations:

$$\text{General: } P_{avg} = \sum_{i=1}^{n} P_i \frac{t_{(2i-1)} - t_{(2i-2)}}{t_{(2n)} - t_{(2i-2)}} \qquad (1\text{–}10)$$

For 3 Pulses:

$$P_{avg} = P_1 \frac{t_1 - t_0}{t_4 - t_0} + P_2 \frac{t_3 - t_2}{t_4 - t_2} \qquad (1\text{–}11)$$

Example: Conditions are shown on Figure 4 (refer to Method 1A).

Procedure: Find P_{avg} from equation 1–3 and the junction temperature rise from equation 1–4.

Conditions: Figure 4

$$P_{avg} = 40 \cdot \frac{0.1}{3.3} + 20 \frac{1}{3} = 1.21 + 6.67$$
$$= 7.88 \text{ Watts}$$
$$T_3 = [P_{avg}\, r(t_5) + (P_3 - P_{avg})\, r(t_5 - t_4)]\, R_{\theta JC}$$
$$= [7.88\ (0.28) + (30 - 7.88) \cdot 0.07]\ 35$$
$$= [2.21 + 1.56]\ 35 = 132°C$$

This result is high because in the actual case considerable cooling time occurred between P_2 and P_3 which allowed T_J to become very close to T_C. Better accuracy is obtained when several pulses are present by using equation 1–10 in order to calculate $T_J - t_C$ at the end of the $n^{th} + 1$ pulse. This technique provides a conservative quick answer if it is easy to determine which pulse in the train will cause maximum junction temperature.

METHOD 3D – FINDING TEMPERATURE AT THE END OF THE N + 1 PULSE IN A RANDOM TRAIN

The method is similar to 3C and the procedure is identical. P_{avg} is calculated from Equation 1–10 modified by $r(t_{2n-1})$ and substituted into equation 1–6, i.e.,

$$T_{n+1} = [P_{avg}\, r(t_{2n-1}) + (P_D - P_{ave})\, r(t_{2n-1} - t_{2n-2}) + P_D\, r(t_{2n+1} - t_{2n}) - P_D\, r(t_{2n+1} - t_{2n-1})]\, R_{\theta JC}$$

The previous example cannot be worked out for the n + 1 pulse because only 3 pulses are present.

Table 2. Summary Of Numerical Solution For The Repetitive Pulse Train Of Figure 5

Temperature Desired	Temperature Obtained, °C		
	Pulse by Pulse	Average Power Nth Pulse	Average Power N + 1 Pulse
At End of 5th Pulse	70.0 (1B)	77 (3A)	70.8 (3B)
Steady State Peak	–	86.9 (2A)	80.9 (2B)

Note: Number in parenthesis is method used.

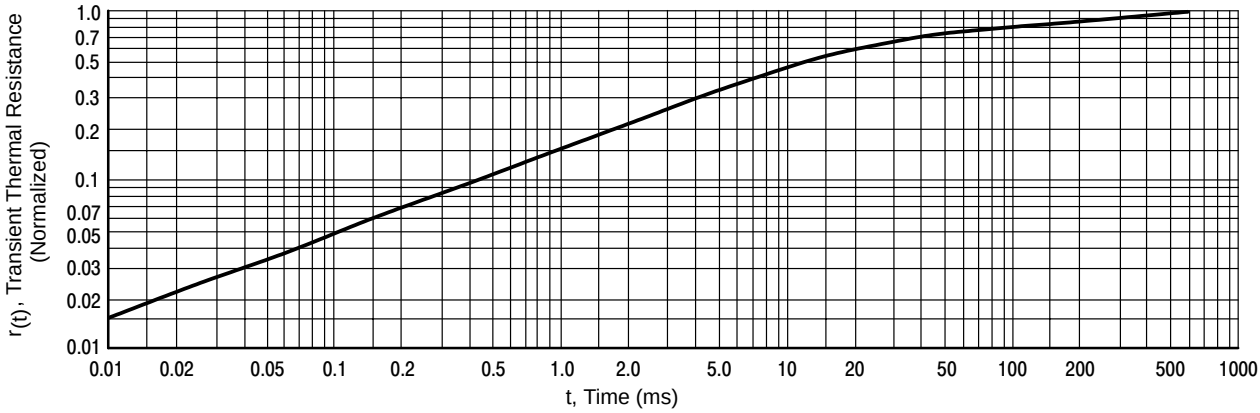


Figure 9. 2N3467 Transient Thermal Response

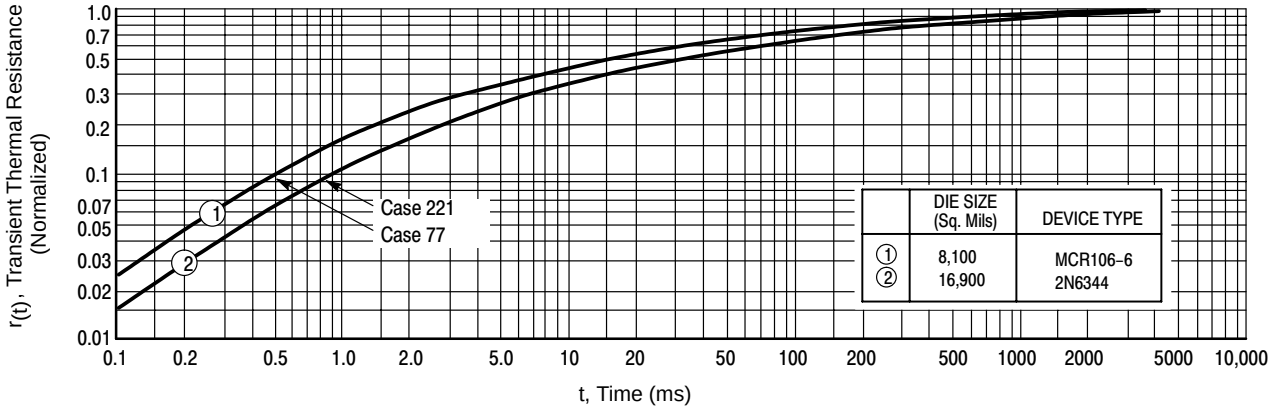


Figure 10. Case 77 and TO–220 Thermal Response

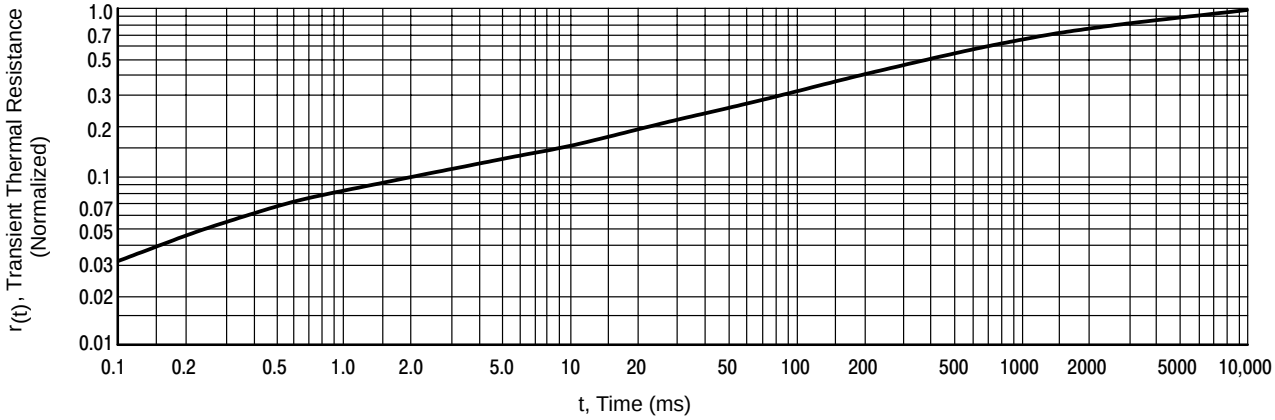


Figure 11. TO–92 Thermal Response, Applies to All Commonly Used Die

Section 4

Soldering / Mounting Techniques

Soldering Considerations for Surface Mount Packages

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain/collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for a SOT–223 device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain/collector pad. By increasing the area of the drain/collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 1.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

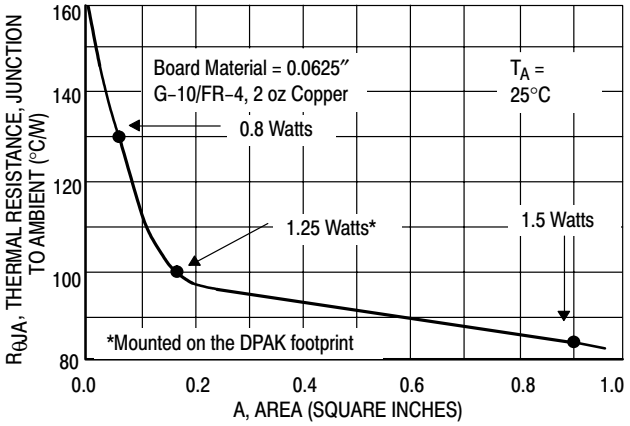


Figure 1. Thermal Resistance versus Drain Pad Area for the SOT–223 Package (Typical)

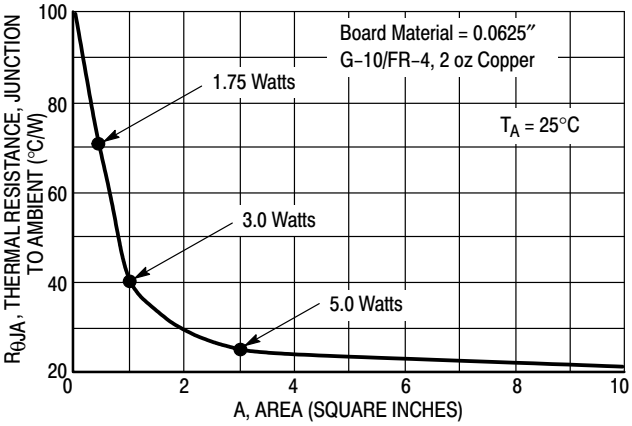


Figure 2. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

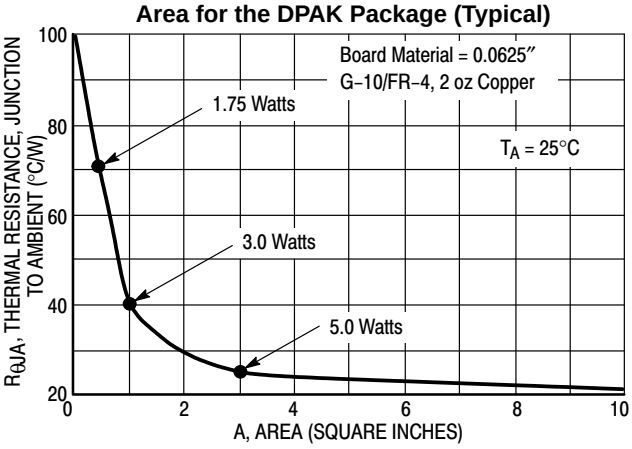


Figure 3. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SOT−23, SC−59, SC−70/SOT−323, SC−90/SOT−416, SOD−123, SOT−223, SOT−363, SO−14, SO−16, and TSOP−6 packages, the stencil opening should be the same as the pad size or a 1:1 registration.

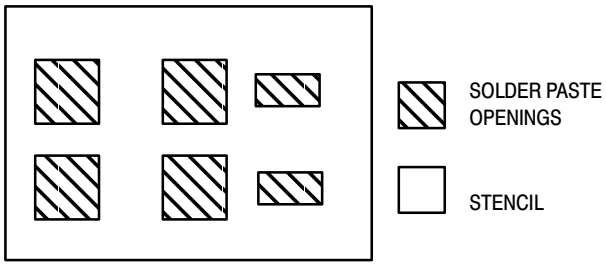


Figure 4. Typical Stencil for DPAK, D^2PAK and D^3PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK and D^3PAK are not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 2 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

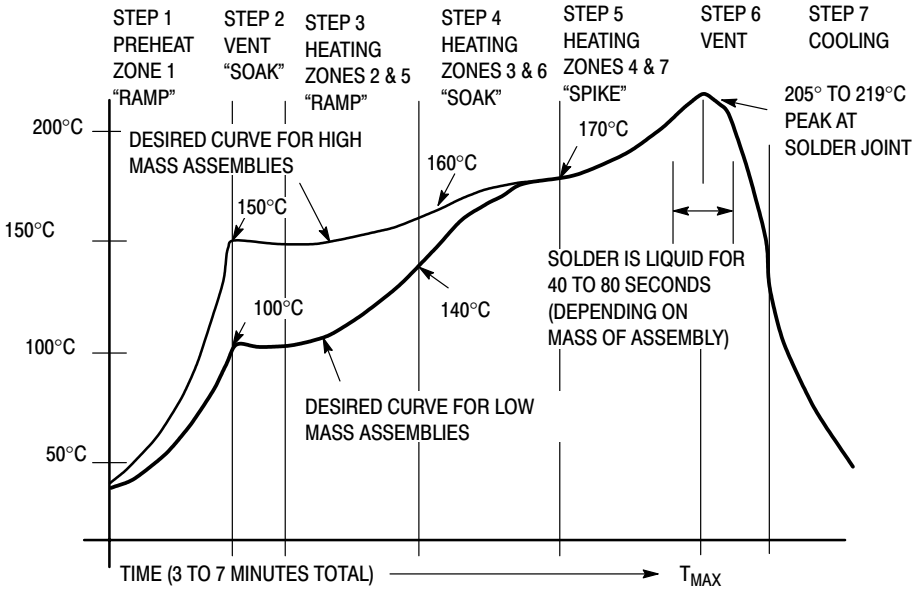
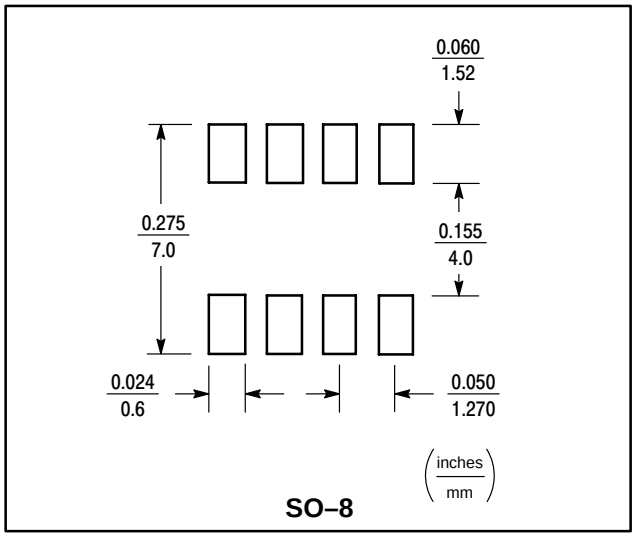
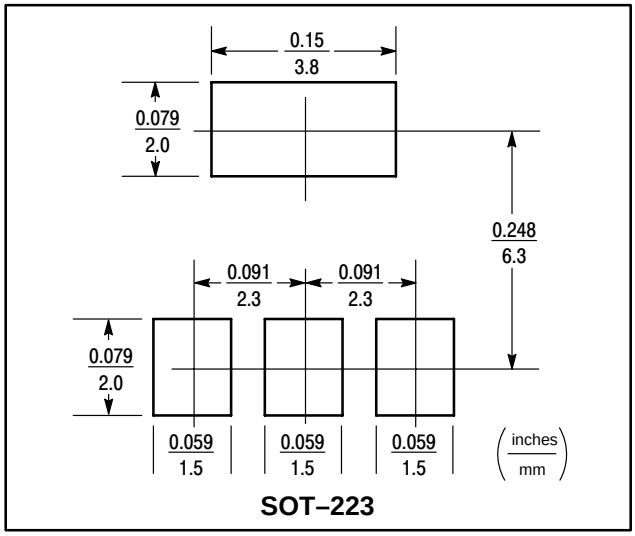


Figure 5. Typical Solder Heating Profile

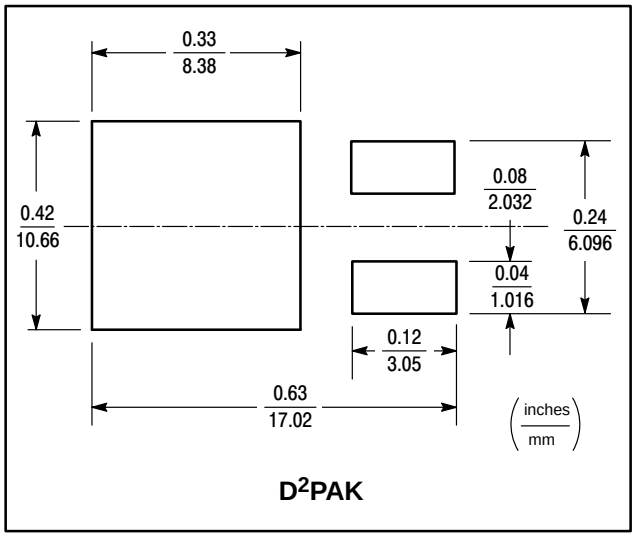
Typical Footprints for Soldering Surface Mount Packages



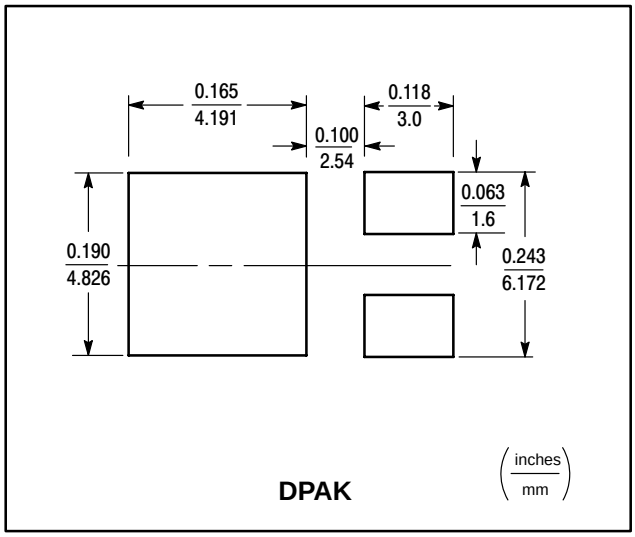
SO–8



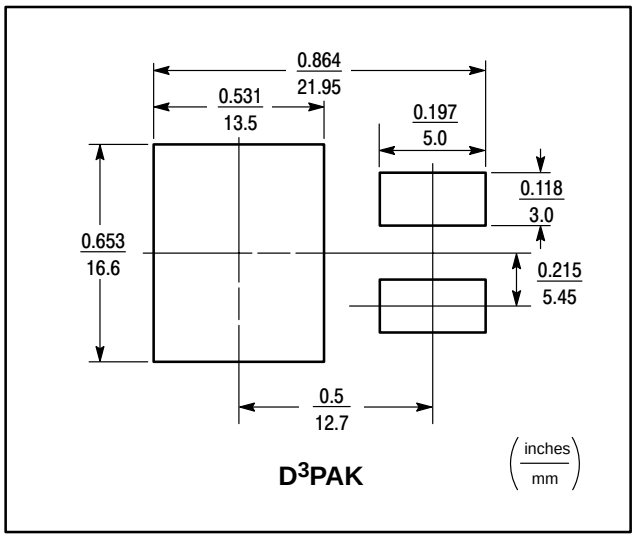
SOT–223



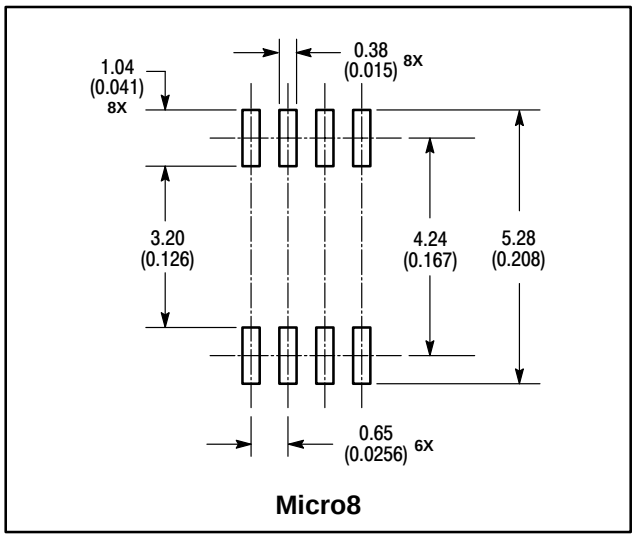
D^{2}PAK



DPAK



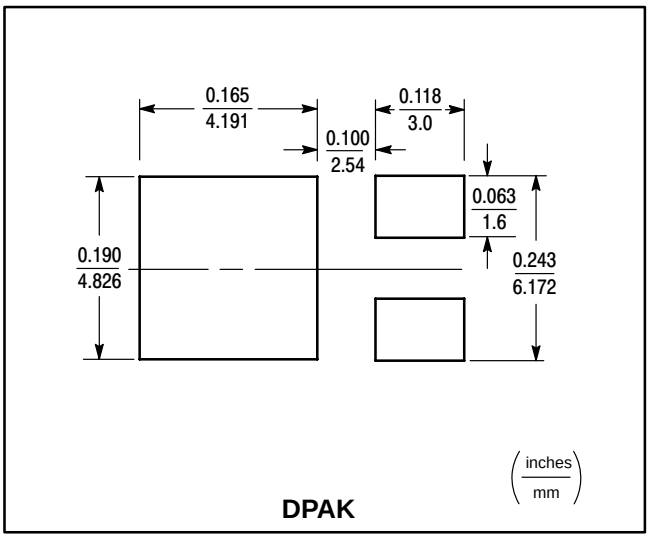
D^{3}PAK



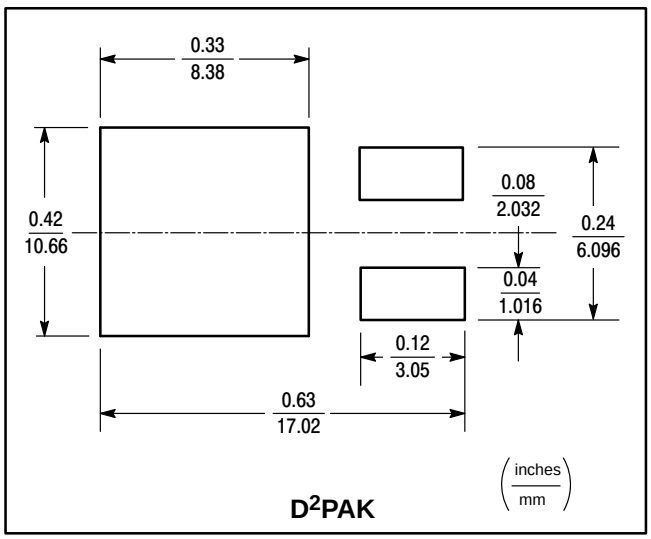
Micro8

Appendix B Footprints for Soldering

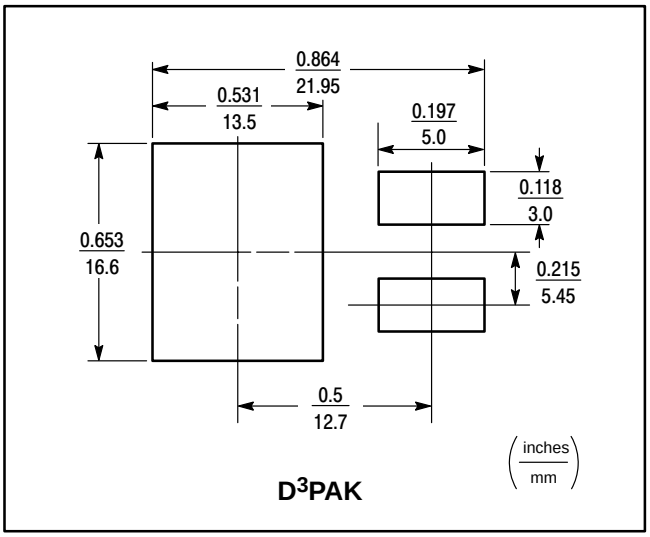
Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry the packages will self align when subjected to a solder reflow process.



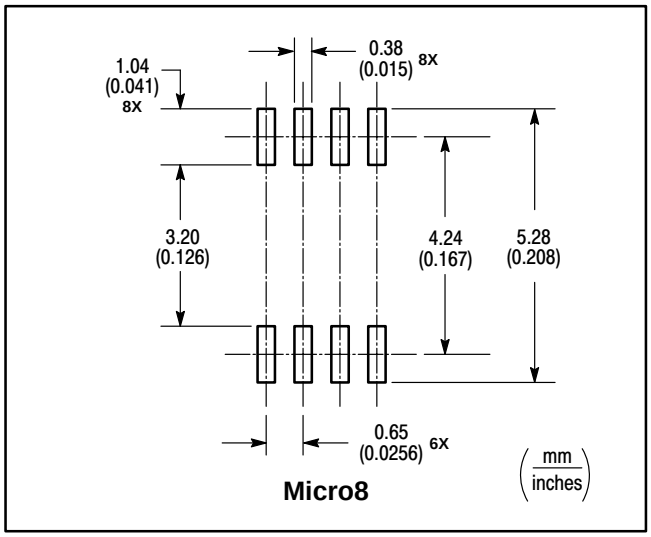
DPAK



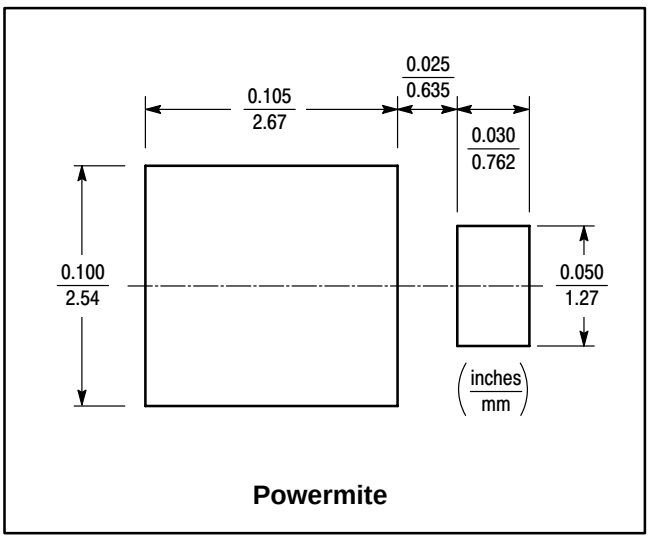
D²PAK



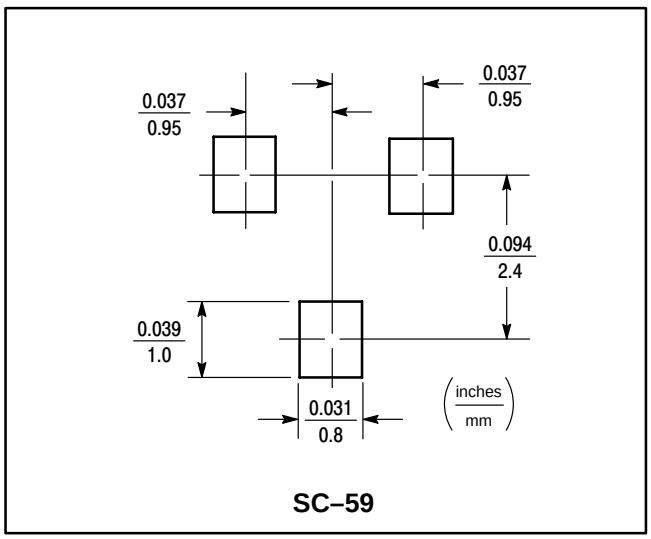
D³PAK



Micro8

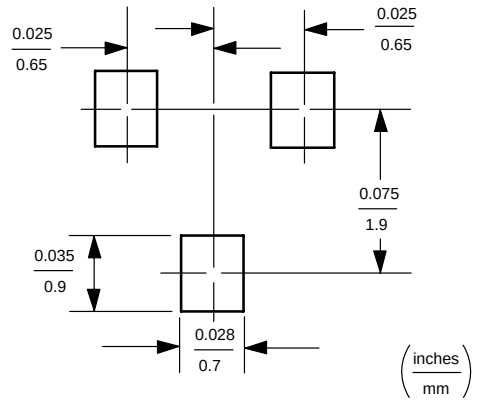


Powermite

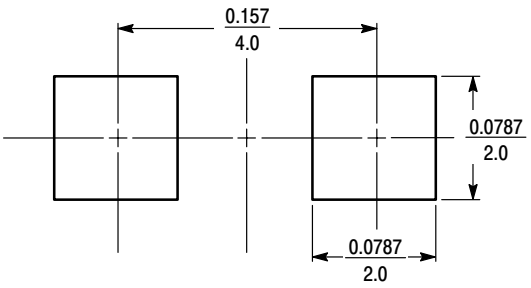


SC–59

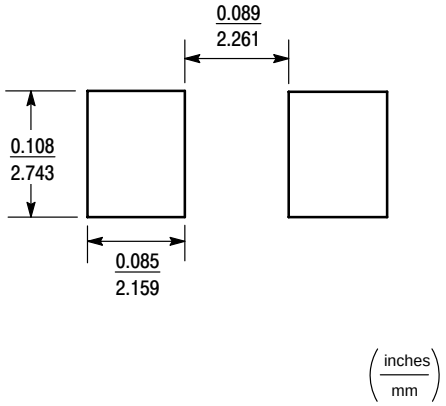
Appendix B Footprints for Soldering (continued)



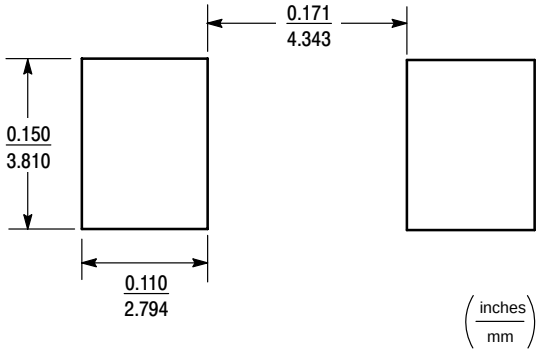
SC−70/SOT−323



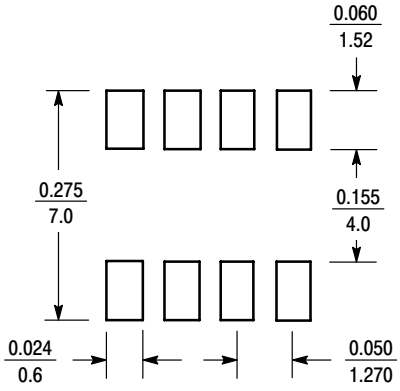
SMA



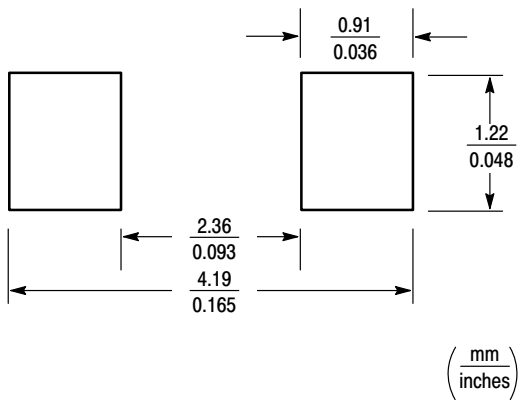
SMB



SMC

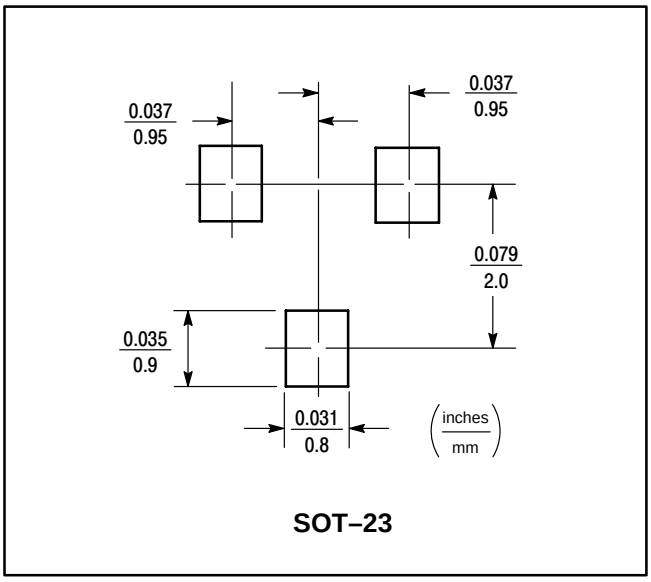


SO−8

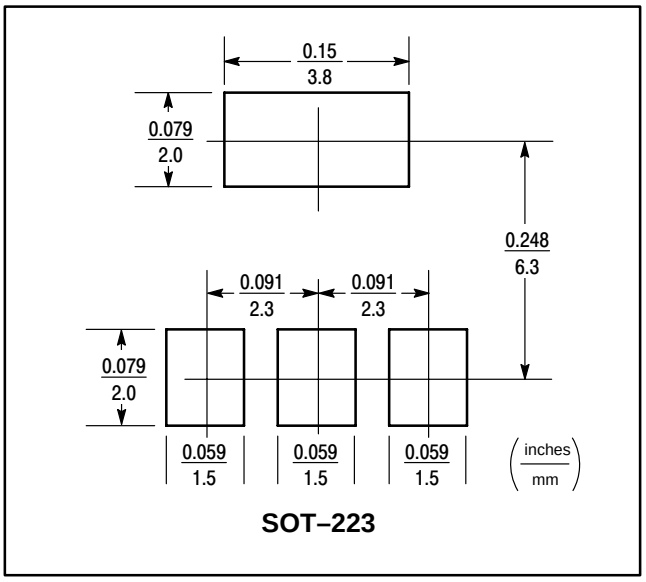


SOD−123

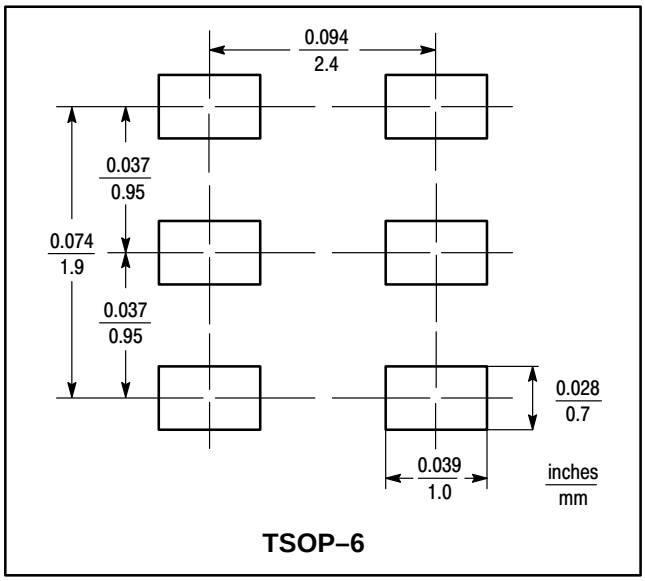
Appendix B Footprints for Soldering (continued)



SOT−23



SOT−223



TSOP−6

AN1040/D

Mounting Considerations for Power Semiconductors

Prepared by: Bill Roehr

ON Semiconductor

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead–mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one–half for a decrease in junction temperature from 160°C to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic–packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 1 shows an example of doing nearly everything wrong. A tab mount TO–220 package is shown being used as a replacement for a TO–213AA (TO–66) part which was socket mounted. To use the socket, the leads are bent – an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet–metal screw through a 1/4″ hole containing a fiber–insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

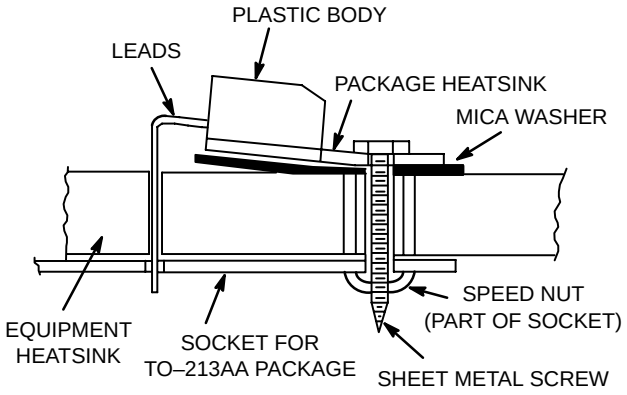


Figure 1. Extreme Case of Improperly Mounting a Semiconductor (Distortion Exaggerated)

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc–over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Stud Mount
Flange Mount
Pressfit
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high–power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e, Δh/TlR, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy, Inc., using a copper TO–204 (TO–3) package with a typical 32–microinch finish, showed that heatsink finishes between 16 and 64 μ–in caused less than ± 2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.(3) Most commercially available cast or extruded heatsinks will require spotfacing when used in high–power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO–3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This “crater” in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat–dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early–life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine–edge blanking or sheared–through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four–post die sets equipped with proper pressure pads and holding fixtures.

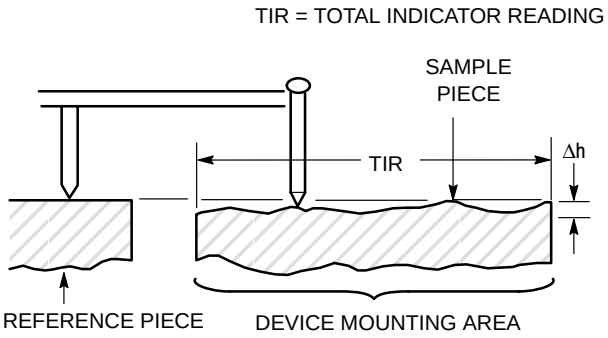


Figure 2. Surface Flatness Measurement

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black–anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromateacid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock–marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease–like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic–encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Figure 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil®, a dry graphite compound, is shown in the data of Figure 3 through Figure 6. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called Kon–Dux™. It is made with a unique, grain oriented, flake–like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

Table 1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed in ON Semiconductor Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
			Metal–to–Metal		With Insulator			
JEDEC Outlines	Description	Test Torque In–Lb	Dry	Lubed	Dry	Lubed	Type	See Note
DO–203AA, TO–210AA TO–208AB	10–32 Stud 7/16″ Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO–203AB, TO–210AC TO–208	1/4–28 Stud 11/16″ Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO–208AA	Pressfit, 1/2″	–	0.15	0.1	–	–	–	
TO–204AA (TO–3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO–213AA (TO–66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO–126	Thermopad 1/4″ x 3/8″	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO–220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figure 3 through Figure 7 for additional data on TO–3 and TO–220 packages.
2. Screw not insulated. See Figure 20.

INSULATION CONSIDERATIONS

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the ON Semiconductor FULLPAK™ and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal–to–metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO–204 (TO–3) and TO–220 packages, are shown in Figure 3 through Figure 6, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 3 through Figure 6, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraded, as the dust is highly toxic.) Thermafilm™ is a filled polymide material which is used for isolation (variation of Kapton®). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

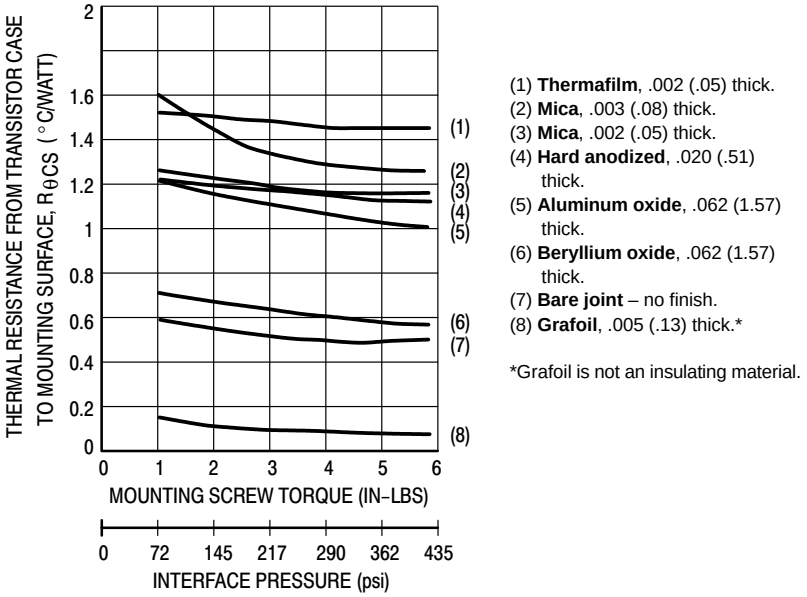


Figure 3. TO–204AA (TO–3) Without Thermal Grease

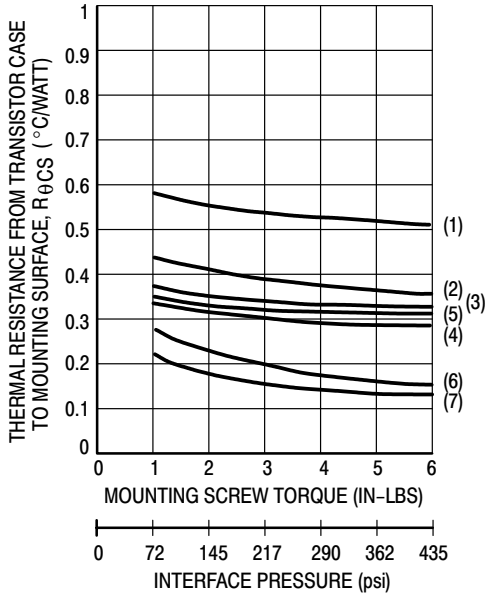


Figure 4. TO–204AA (TO–3) With Thermal Grease

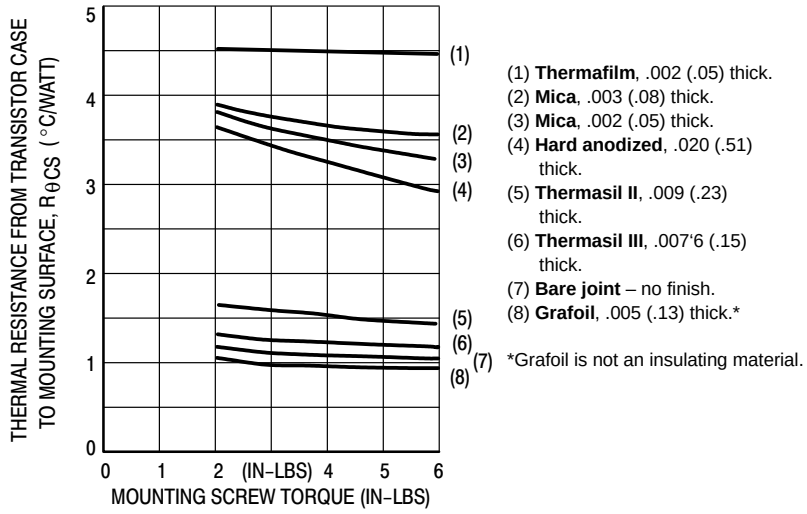


Figure 5. TO–220 Without Thermal Grease

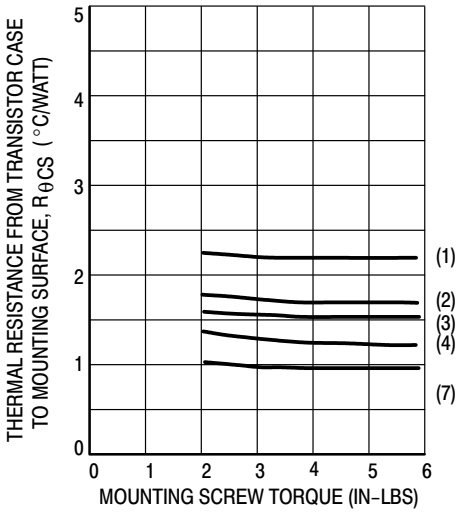


Figure 6. TO–220 With Thermal Grease

INTERFACE THERMAL RESISTANCE FOR TO–204, TO–3 AND TO–220 PACKAGES USING DIFFERENT INSULATING MATERIALS AS A FUNCTION OF MOUNTING SCREW TORQUE (DATA COURTESY THERMALLOY)

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut–through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figure 5 and Figure 6, it can be noted that Thermasil™, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO–220 package.

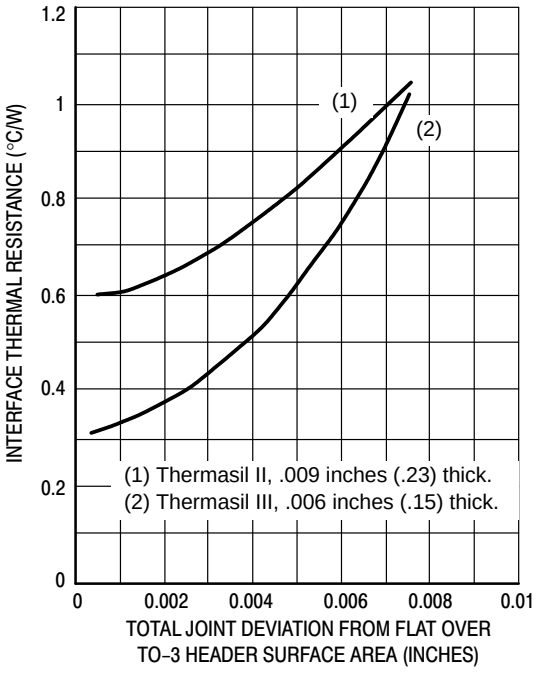
A number of manufacturers offer silicone rubber insulators. Figure 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out–of–flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K–10® pad, for example, is described as having about 2/3 the interface resistance of the Sil–Pad® 1000 which would place its performance close to the Chomerics 1671 pad. Aavid also offers an isolated pad called Rubber–Duc™, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from Aavid shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

Table 2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173–7	.790	1.175
Bergquist	Sil–Pad K–4®	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil–Pad 400–9®	.735	1.205
Thermalloy	Thermasil II	.680	1.045
Shin–Etsu	TC–30AG	.664	1.260
Bergquist	Sil–Pad 400–7®	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174–9	.574	.755
Bergquist	Sil–Pad 1000®	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermasil III	.440	1.035
Chomerics	1671	.367	.655

*Test Fixture Deviation from flat from Thermalloy EIR86–1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO–204AA (TO–3) package insulated with Thermasil is shown on Figure 7. Observe that the “worst case” encountered (7.5 mils) yields results having about twice the thermal resistance of the “typical case” (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.



Data courtesy of Thermalloy

Figure 7. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the CHO–THERM® 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in–lb from an initial 6 in–lb. With nonconformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Figure 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 3. Performance of Silicon Rubber Insulators Tested Per MIL–I–49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Bergquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	–
CHO–THERM, 1617	0.233	–
Q Pad (non–insulated)	–	0.009
Sil–Pad, K–10	0.263	0.200
Thermasil III	0.267	–
Mica, greased	0.329	0.400
Sil–Pad 1000	0.400	0.300
CHO–THERM 1674	0.433	–
Thermasil II	0.500	–
Sil–Pad 400	0.533	0.440
Sil–Pad K–4	0.583	0.440

(1) From Thermalloy EIR 87–1030
(2) From Bergquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi–pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost–effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The EMS (Energy Management Series) Modules, shown on Figure 16, Case 806 (ICePAK™) and Case 388A (TO–258AA) (see Figure 16) are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The isolated, Case 221C, illustrated in Figure 21, is an example of parts in the second category.

Parts in the first category – those with an exposed metal flange or tab – are mounted the same as their non–insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 8, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection – generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a "sync nut," the patented device can be soldered to a PC board and the semiconductor mounted with a 6–32 machine screw.(4)

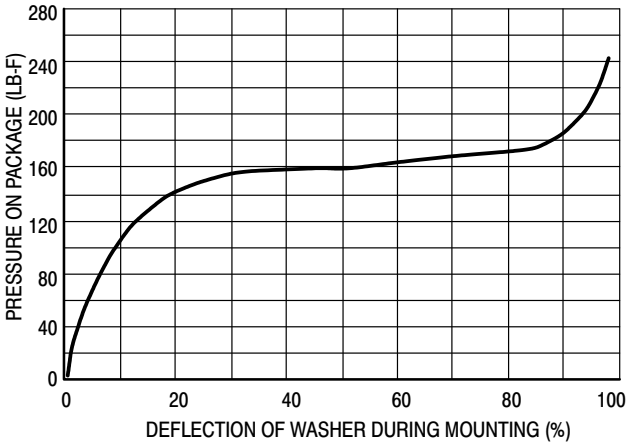


Figure 8. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board–mounted or free–standing heat dissipaters with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO–220 and TO–126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO–220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync nuts) can form a trouble–free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self–Tapping Screws

Under carefully controlled conditions, sheet–metal screws are acceptable. However, during the tapping process with a standard screw, a volcano–like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speednut. If a self tapping process is desired, the screw type must be used which roll–forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange–mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press–riveting is used. Crimping force must be applied slowly and evenly. Pop–riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt–furnace, irons, vapor–phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.[5] Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non–field serviceable systems or low strength types for field serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

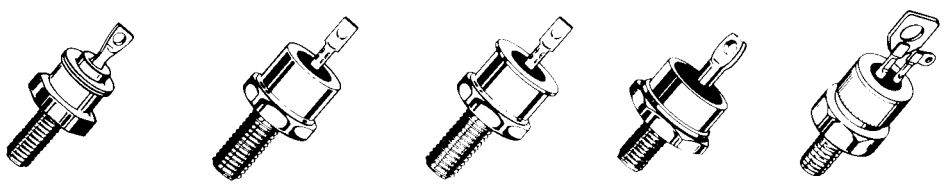
To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel– or gold–plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

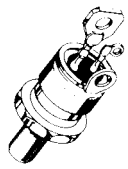
Stud Mount

Parts which fall into the stud–mount classification are shown in Figure 8 through Figure 11. Mounting errors with non–insulated stud–mounted parts are generally confined to application of excessive torque or tapping the stud into a threaded heatsink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer; the details are shown in Figure 12.



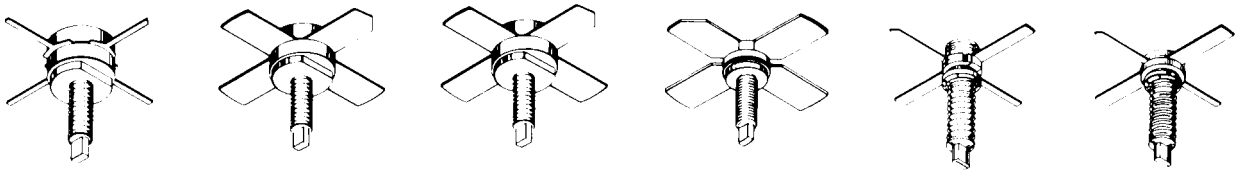
CASE 42A (DO–5) | **CASE 56–03 DO–203AA (DO–4)** | **CASE 245 (DO–4)** | **CASE 257 DO–203AB (DO–5)** | **CASE 263–04**

Figure 9. Standard Non–Isolated Types



CASE 311–02

Figure 10. Isolated Type



CASE 144B–05 (.380″ STUD) | **CASE 145A–09 (.380″ STUD)** | **CASE 145A–10 (.500″ STUD)** | **CASE 244–04 (.280″ STUD)** | **CASE 305–01 (.204″ STUD)** | **CASE 332–04 (.380″ STUD)**

Figure 11. RF Stripline Opposed Emitter (SOE) Series

A VARIETY OF STUD–MOUNT PARTS

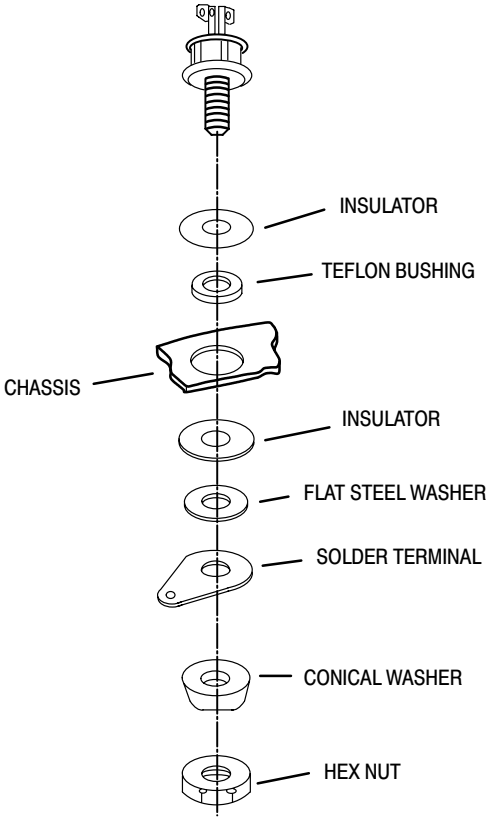


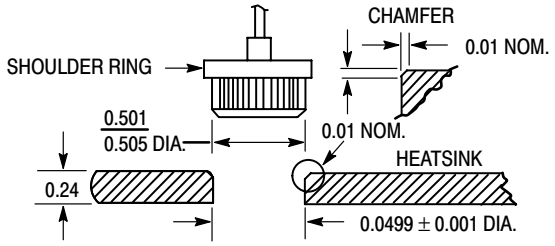
Figure 12. Isolating Hardware Used for a Non–Isolated Stud–Mount Package

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non–insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a beryllium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

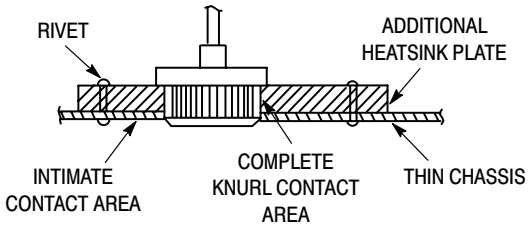
RF transistors in the stud–mount stripline opposed emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the stripline leads and to mount the part so no tension or shear forces are applied to any ceramic – metal interface are discussed in the section entitled “Connecting and Handling Terminals.”

Press Fit

For most applications, the press–fit case should be mounted according to the instructions shown in Figure 13. A special fixture meeting the necessary requirements must be used.



HEATSINK MOUNTING



THIN–CHASSIS MOUNTING

The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press–in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heatsink material. Recommended hardnesses are: copper–less than 50 on the Rockwell F scale; aluminum–less than 65 on the Brinell scale. A heatsink as thin as 1/8″ may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

Figure 13. Press–Fit Package

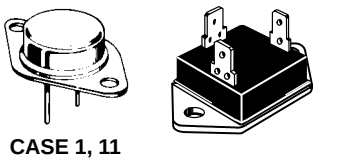
Flange Mount

A large variety of parts fit into the flange mount category as shown in Figure 14 through Figure 17. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO–204 (TO–3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger–tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 18. Machine screws (preferred) self–tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section, “Fastener and Hardware Characteristics.”

The copper flange of the Energy Management Series (EMS) Modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, Figure 15, final torque should be applied first to the center position.

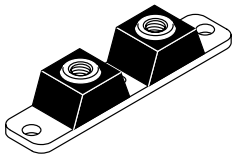
The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in Engineering Bulletin EB107/D "Mounting Considerations for ON Semiconductor RF Power Modules." Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.



CASE 1, 11 TO–204AA (TO–3)

CASE 383–01

Figure 14. TO–3 Variations



CASE 357C–03

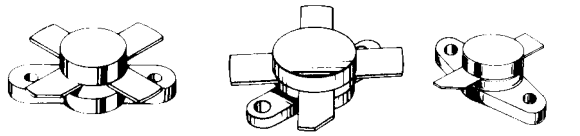
Figure 15. Plastic Power Tap

CASE 373–01 CASE 807–03 CASE 807A–03 CASE 808–01

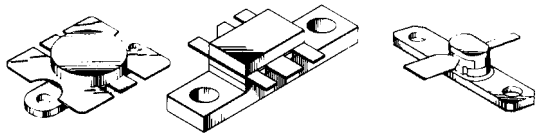
CASE 809–02 CASE 812–02 CASE 813–02

CASE 814–02 CASE 816–02 CASE 819–02

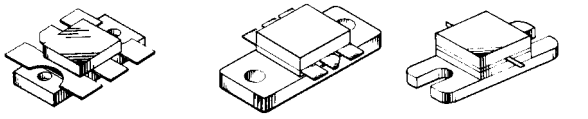
Figure 16. Energy Management Series (Isolated Base Plate)



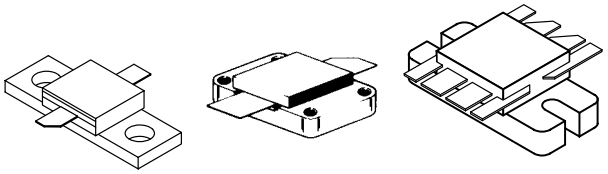
CASE 211–07 CASE 211–11 CASE 215–02



CASE 316–01 CASE 319–07 (CS–12) CASE 328A–03



CASE 333–04 CASE 333A–02 (MAAC PAC) CASE 336–03



CASE 337–02 CASE 368–03 (HOG PAC) CASE 744A–01

Figure 17. RF Stripline Isolated Output Opposed Emitter (SOE) Series

A LARGE ARRAY OF PARTS FIT INTO THE FLANGE–MOUNT CLASSIFICATION

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area Case 368–03 (HOG PAC) will be used to illustrate problem areas. It is more sensitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4–40 mounting screws is 5 in/lbs. Spring and flat washers are recommended. Over torquing is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length, instead it bends upwards in the mid–section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With

sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center of the flange, deforming it. Deformations of 2 – 3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

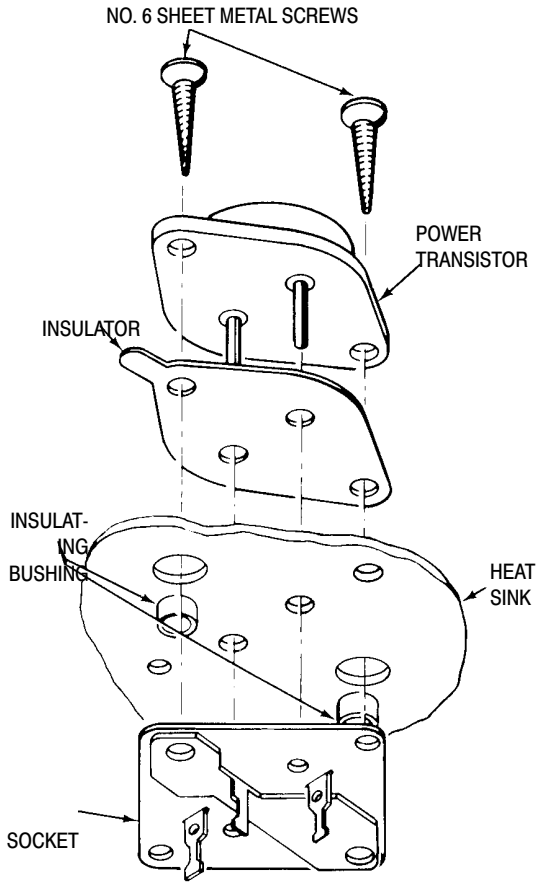


Figure 18. Hardware Used for a TO–204AA (TO–3) Flange Mount Part

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 19. Mounting considerations for all varieties are similar to that for the popular TO–220 package, whose suggested mounting arrangements and hardware are shown in Figure 20. The rectangular washer shown in Figure 20a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch–pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, ON Semiconductor TO–220 packages have a chamfer on one end. TO–220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

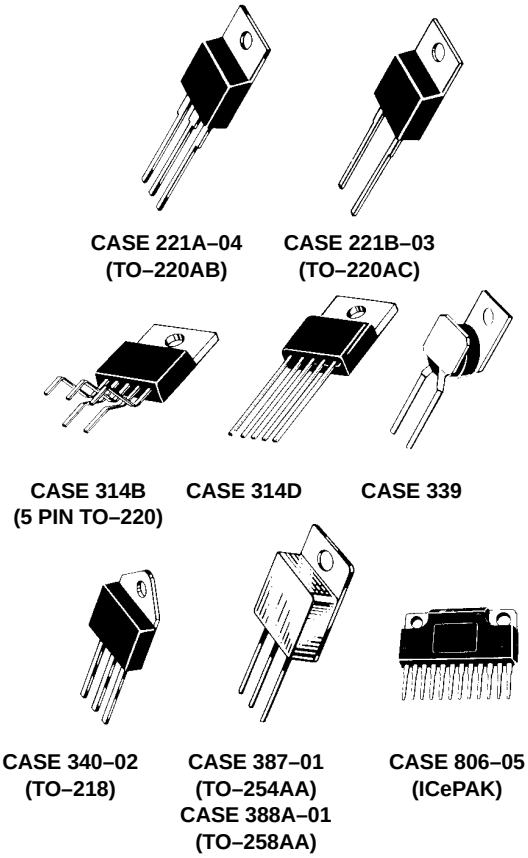


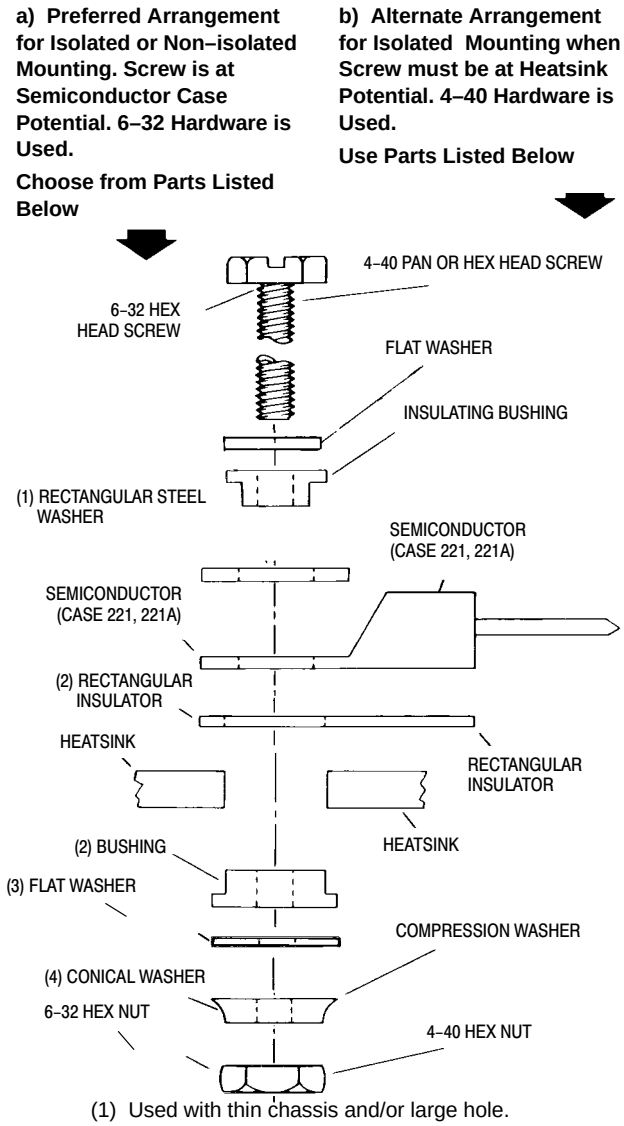
Figure 19. Several Types of Tab–Mount Parts

The popular TO–220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure 36.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 27.

To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806–05) is basically an elongated TO–220 package with isolated chips. The mounting precautions for the TO–220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

Figure 20. Mounting Arrangements for Tab Mount TO–220

Plastic Body Mount

The Thermopad™ and isolated plastic power packages shown in Figure 21 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts this is accomplished by die–bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The isolated (Case 221C–02) is similar to a TO–220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO–220 and is similar to that of the Thermopad.

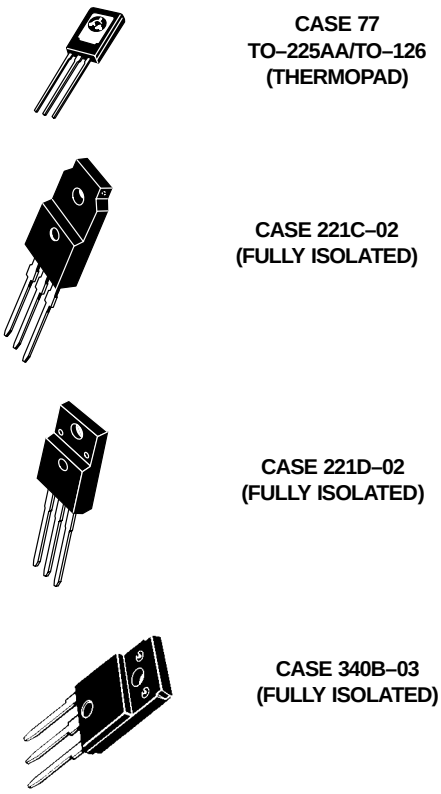


Figure 21. Plastic Body–Mount Packages

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air–driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 8.

Figure 22 through Figure 24 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The isolated, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO–220. As shown in Figure 27, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure 36 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 26 may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO–220 package which is shown in Figure 25.

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 28, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

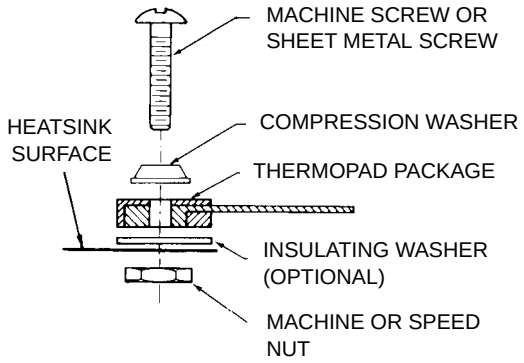
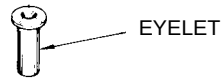


Figure 22. Machine Screw Mounting



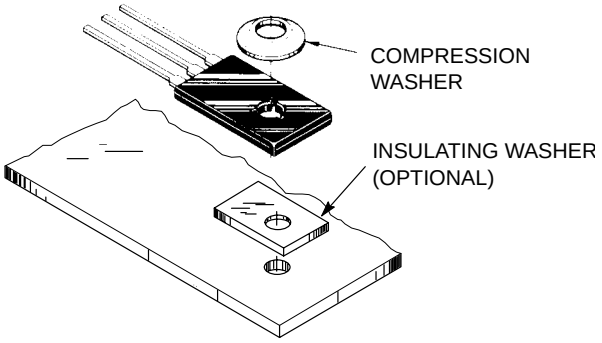


Figure 23. Eyelet Mounting

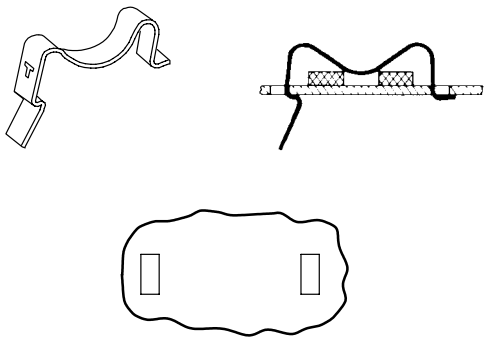


Figure 24. Clips

RECOMMENDED MOUNTING ARRANGEMENTS FOR TO–225AA (TO–126) THERMOPAD PACKAGES

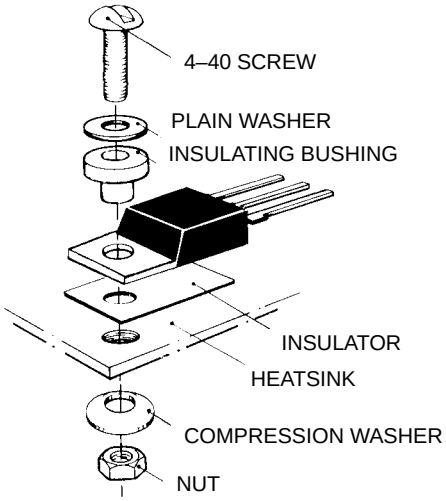


Figure 25. Screw–Mounted TO–220

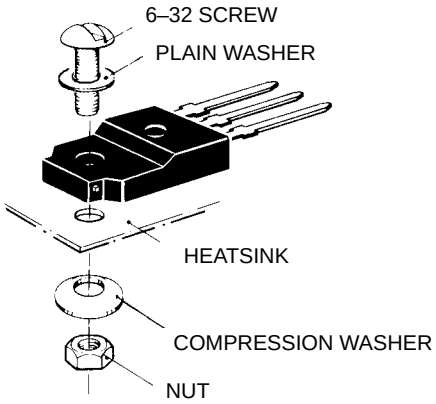


Figure 26. Screw–Mounted Isolated Package

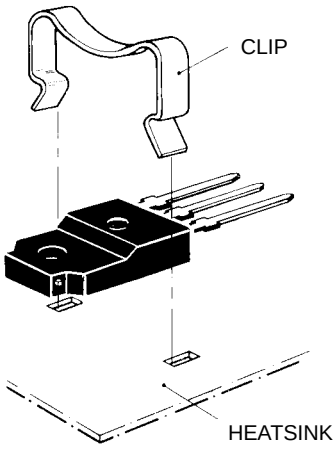


Figure 27. Clip–Mounted Isolated Package

MOUNTING ARRANGEMENTS FOR THE ISOLATED PACKAGE AS COMPARED TO A CONVENTIONAL

CASE 369–07 CASE 369A–13

Figure 28. Surface Mount D–PAK Parts

Standard Glass–Epoxy 2–ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 29 shows, thermal resistance asymptotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlaid with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.(7) The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

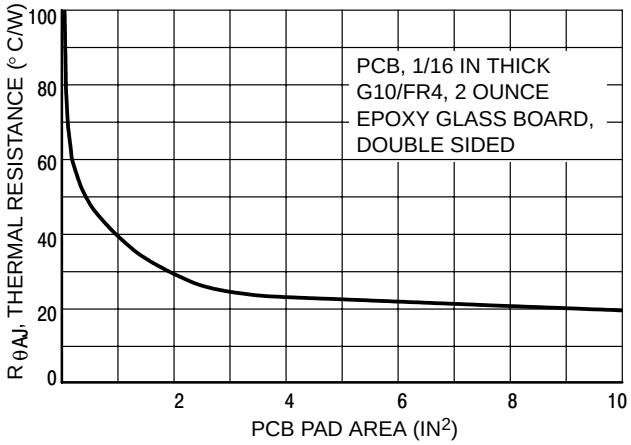


Figure 29. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass–Epoxy Board

FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO–220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the Case 77 (TO–225AA) (TO–127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 30 and Figure 31. The arrangement of Figure 30 could be used with any plastic package, but the scheme of Figure 31 is more practical with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

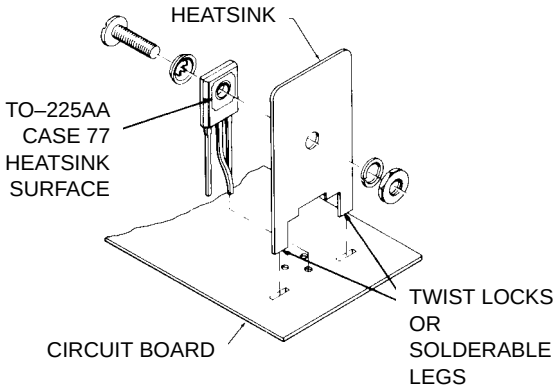


Figure 30. Simple Plate, Vertically Mounted

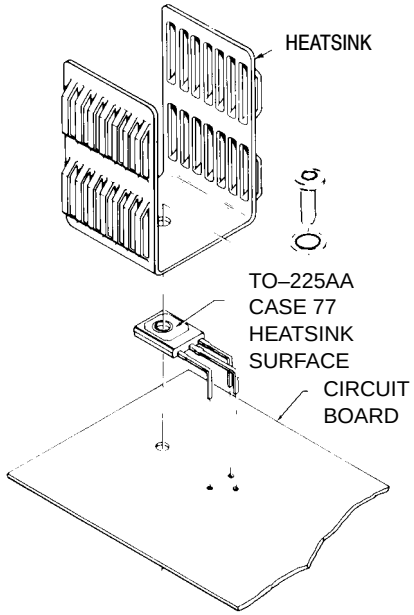


Figure 31. Commercial Sink, Horizontally Mounted

METHODS OF USING SMALL HEATSINKS WITH PLASTIC SEMICONDUCTOR PACKAGES

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from ON Semiconductor. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

EMS Modules

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead–bending unnecessary. Numerous lead and tab–forming options are available from ON Semiconductor on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead–bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO–225AA (Case 77) and 1/32 inch for TO–220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead–to–plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire–wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Stripline Packages

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 32 through Figure 34. The following rules should be observed:

1. The device should never be mounted in such a manner as to place ceramic–to–metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 33 shows a cross–section of a printed circuit board and heatsink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D–flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud – BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead–soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger, this may result in device failure as power is applied.

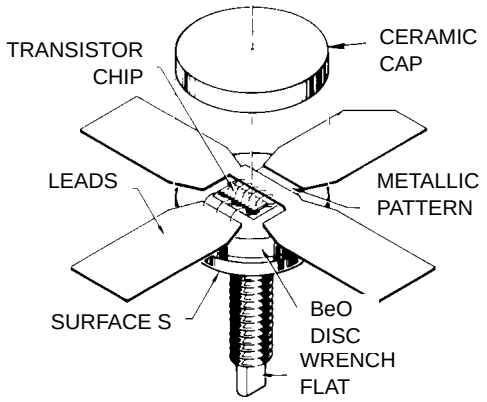


Figure 32. Component Parts of a Stud Mount Stripline Package. Flange Mounted Packages are Similarly Constructed

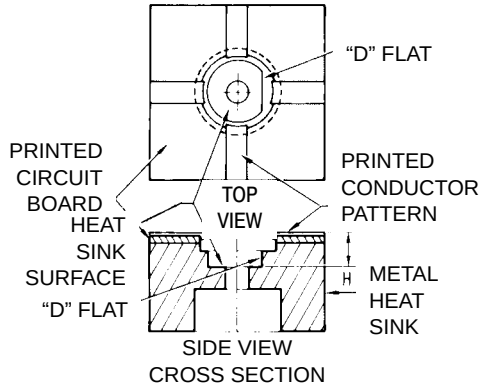


Figure 33. Typical Stud Type SOE Transistor Mounting Method

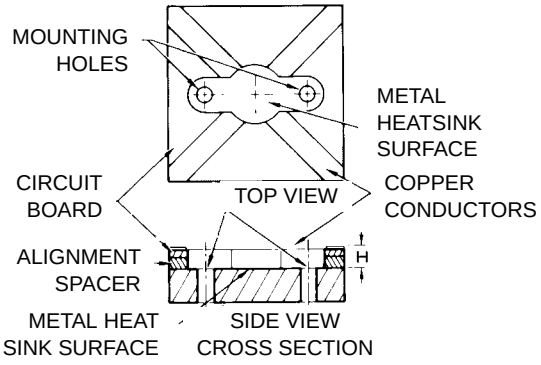


Figure 34. Flange Type SOE Transistor Mounting Method

MOUNTING DETAILS FOR SOE TRANSISTORS

Figure 34 shows a typical mounting technique for flange–type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free–standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see ON Semiconductor Application Note, AN569/D.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where T_J = junction temperature (°C)
T_C = case temperature (°C)
$R_{\theta JC}$ = thermal resistance junction–to case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the “test” position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A
THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady–state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D)
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure 35.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D (R_{\theta JC} + P_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
PD = power dissipation
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat–sink),
$R_{\theta SA}$ = heat sink thermal resistance (heatsink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short–pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

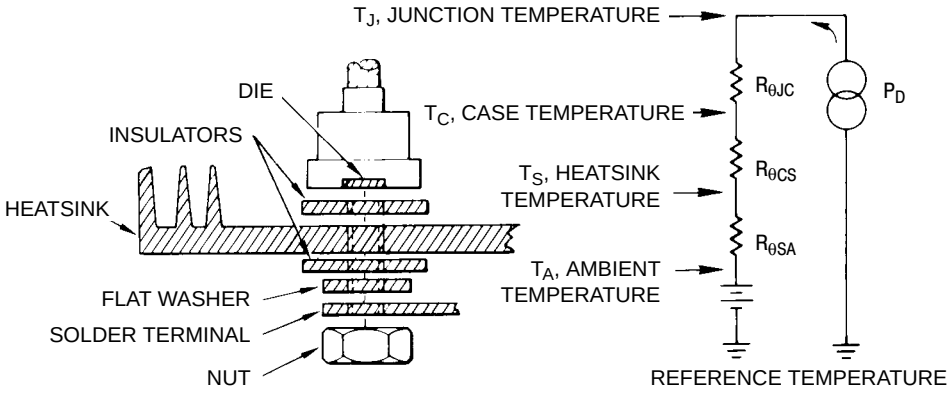


Figure 35. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B
MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO–3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL–I–49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The ON Semiconductor fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO–220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO–220 package shown in Figure 36. The mounting pressure at one end causes the other end – where the die is located – to lift off the mounting surface slightly. To improve contact, ON Semiconductor TO–220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

1. The ON Semiconductor location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.
2. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.
3. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

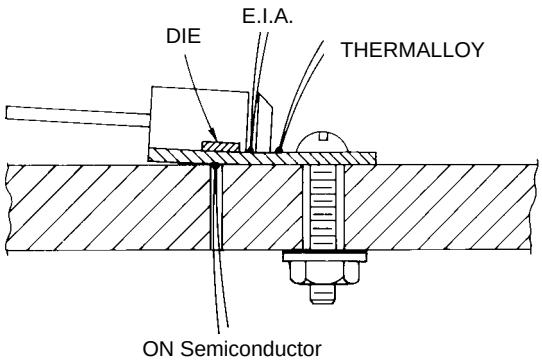


Figure 36. JEDEC TO–220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the ON Semiconductor location is even hotter. Since junction–to–sink thermal resistance must be constant for a given test setup, the calculated junction–to–case thermal resistance values decrease and case–to–sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The ON Semiconductor location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The ON Semiconductor location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO–220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction–to–case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ–inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application–oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction–to–case thermal resistance while testing for interface thermal resistance. If the junction–to–case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C
Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks	Clips
			BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber		
Aavid	–	–	–	–	–	–	X	X	X	X
AHAM–TOR	–	–	–	–	–	–	–	–	X	–
Asheville–Schoonmaker	–	–	–	–	–	X	–	–	–	–
Astrodynamis	X	–	–	–	–	–	–	–	X	–
Delbert Blinn	–	–	X	–	X	X	X	X	X	–
IERC	X	–	–	–	–	–	–	–	X	–
Staver	–	–	–	–	–	–	–	–	X	–
Thermalloy	X	X	X	X	X	X	X	X	X	X
Tran–tec	X	–	X	X	X	X	–	X	X	–
Wakefield	X	X	X	–	X	–	–	X	X	X

Other Sources for silicone rubber pads: Chomerics, Bergquist

Suppliers Addresses

Aavid Engineering, Inc., P.O. Box 400, Laconia, New Hampshire 03247 (603) 524–1478
AHAM–TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676–4151
Asheville–Schoonmaker, 900 Jefferson Ave., Newport News, VA 23607 (804) 244–7311
Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935–4944
Bergquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835–2322
Chomerics, Inc.,16 Flagstone Drive, Hudson, New Hampshire 03051 1–800–633–8800
Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 623–1257
International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849–2481
The Staver Company, Inc., 41–51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666–8000
Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243–4321
Tran–tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564–2748
Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245–5900

PACKAGE INDEX

PREFACE

When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non–related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a category are denoted by suffix letters. The older package designations were re–registered to the new system as time permitted.

For example the venerable TO–3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO–204 family. The TO–204AA conforms to the original outline for the TO–3 having 40 mil pins while the TO–204AE has 60 mil pins, for example.

The new numbers for the old parts really haven't caught on very well. It seems that the DO–4, DO–5 and TO–3 still convey sufficient meaning for general verbal communication.

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
001	TO-3	TO-204AA		Flange
003	TO-3		2	Flange
009	TO-61	TO-210AC		Stud
011	TO-3	TO-204AA	–	Flange
011A	TO-3	–	2	Flange
012	TO-3	–	2	Flange
036	TO-60	TO-210AB	–	Stud
042A	DO-5	DO-203AB	–	Stud
044	DO-4	DO-203AA	–	Stud
054	TO-3	–	2	Flange
056	DO-4	–	–	Stud
058	DO-5	–	2	Stud
61-04				Flange
63-02	TO-64	TO-208AB		Stud
63-03	TO-64	TO-2088AB		Stud
077	TO-126	TO-225AA	–	Plastic
080	TO-66	TO-213AA	–	Flange
086	–	TO-208	1	Stud
086L	–	TO-298	1	Stud
144B-05				Stud
145A-09				Stud
145A-10				Stud
145C	TO-232		1	Stud
157	–	DO-203	1	Stud
160-03	TO-59	TO-210AA	–	Stud
167	–	DO-203	1	Stud
174-04				Pressfit

Notes: 1. Would fit within this family outline if registered with JEDEC.
2. Not within all JEDEC dimensions.

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
175-03				Stud
197	–	TO-204AE	–	Flange
211-07				Flange
211-11				Flange
215-02				Flange
221	–	TO-220AB	–	Tab
221C-02				Plastic
221D-02	–	–	Isolated TO-220	Plastic
235	–	TO-208	1	Stud
235-03				Stud
238	–	TO-208	1	Stud
239	–	TO-208	–	Stud
244-04				Stud
245	DO-4	–	–	Stud
257-01	DO-5	–	–	Stud
263	–	TO-208	–	Stud
263-04				Stud
283	DO-4	–	–	Stud
289	–	TO-209	1	Stud
305-01				Stud
310-02				Pressfit
311-02			Isolated	Stud
311-02				Pressfit
311-02				Stud
314B-03				Tab

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
314D-03				Tab
316-01				Flange
319-06				Flange
328A-03				Flange
332-04				Stud
333-04				Flange
333A-02				Flange
336-03				Flange
337-02				Flange
340		TO-218AC		Tab
340A-02				Plastic
340B-03			Isolated TO-218	Plastic
342-01				Flange
357B-01				Flange
361-01				Flange
368-02				Flange
369-06		TO-251		Insertion
369A-12		TO-252		Surface
373-01			Isolated	Flange
383-01			Isolated	Flange
387-01		TO-254AA	Isolated 2	Tab
388A-01		TO-258AA	Isolated 2	Tab
744-02				Flange
744A-01				Flange
043-07	DO-21	DO-208AA		Pressfit

(1) MIL–HANDBOOK – 2178, SECTION 2.2.
(2) “Navy Power Supply Reliability – Design and Manufacturing Guidelines” NAVMAT P4855–1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.
(3) Catalog #87–HS–9, (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381–0839.
(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.
(5) Robert Batson, Elliot Fraunglass and James P Moran, “Heat Dissipation Through Thermalloy Conductive Adhesives,” EMTAS ’83. Conference, February 1 – 3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, Ml 48128.
(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.
(7) Herb Fick, “Thermal Management of Surface Mount Power Devices,” Powerconversion and Intelligent Motion, August 1987.

Section 5

Handling of Semiconductor Packages

AND8003/D

Storage and Handling of Drypacked Surface Mounted Devices (SMD)

Prepared by: R. Kampa, D. Hagen, W. Lindsay, and K.C. Brown

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

APPLICATION NOTE

INTRODUCTION

This information provides ON Semiconductor customers with the necessary storage and handling guidelines to preclude component package cracking during solder reflow procedures.

This document applies to plastic encapsulated SMDs that ON Semiconductor identifies as moisture sensitive and delivers in a drypack. Moisture sensitive SMDs include, but are not limited to small outline J pins (SOJs), plastic leaded chip carriers (PLCCs), quad flat packs (QFPs), plastic quad flat packs (PQFPs), thin quad flat packs (TQFPs), thin small outline packages (TSOPs), small outline integrated circuits (SOICs), and plastic ball grid arrays (PBGAs).

SMD PACKAGE LIMITATIONS

During reflow procedures, moisture absorbed from the atmosphere will vaporize inside an SMD and swell into a vapor dome. The internal stresses exerted by the vapor dome are directly proportional to the amount of moisture absorbed prior to reflow. The pressure from the vapor dome may cause of one or more of the internal package interfaces to delaminate. This pressure may also form cracks in the mold compound and possibly expose the die to the external environment.

Both, die surface delaminating and package cracks, pose potential reliability problems. By following the guidelines herein, ON Semiconductor customers will avoid the occurrence of these problems.

DRYPACK DESCRIPTION

Drypack consists of a moisture vapor barrier bag with a preprinted moisture sensitive warning label, a desiccant, and RH indicator, and a barcode label.

The bag construction consists of a three layer laminate; tyvek or nylon for puncture resistance, aluminum for a moisture barrier, and polyethylene for an airtight seal.

The preprinted warning label identifies the contents as moisture sensitive and outlines the recommended storage and handling requirements and shelf life.

The desiccant packed in each bag will keep the internal humidity level below 20% RH for at least one year, under worst case storage conditions of 40°C and 90% RH.

The RH indicator provides the customer with a simple and efficient means to verify that the internal humidity level remains below 20% RH during storage. NOTE: If the RH indicator reads greater than 20% RH at 23°C ± 5°C immediately upon opening the bag, then the SMDs contained therein must undergo a dry–out procedure (see Dry–Out Procedures) prior to any reflow process.

The barcode label identifies the bag seal date and the qualified moisture sensitivity level of the SMD. An ON Semiconductor Standard Operating Procedure (S.O.P.) specification titled “Moisture Characterization and Preconditioning of Plastic Surface Mounted Devices” defines the requirements for qualifying the moisture sensitivity level of a plastic SMD and meets the intent of JEDEC A112, Moisture Induced Stress Sensitivity for Plastic Surface Mounted Devices, and JEDEC A113, Preconditioning of Plastic Surface Mounted Devices Prior to Reliability Testing.

STORAGE REQUIREMENTS AND TIME LIMITS OUT OF DRYPACK

The qualified moisture sensitivity level for each SMD determines the appropriate storage requirements and time limits once out of drypack. Table 1 relates the moisture sensitivity (MS) level to the storage environment and time limits. If these limits are exceeded once the drypack is removed, then the effected SMDs must undergo a dry–out procedure prior to any reflow process.

Table 1.

MS Level	Drypack	Storage TH	Time Out of Drypack
1	No	30°C / 90% RH	Indefinite
2	Yes	30°C / 60% RH	One Year
3	Yes	30°C / 60% RH	168 Hours Max
4	Yes	30°C / 60% RH	72 Hours Max
5	Yes	30°C / 60% RH	24 Hours Max
6	Yes	30°C / 60% RH	6 Hours Max

OPTIONAL STORAGE METHODS OUT OF DRYPACK

If the customer cannot mount the SMDs within the specified time limit, or factory ambient conditions exceed the specified maximum temperature and/or humidity level, then the customer can abate moisture absorption by immediately storing the SMDs at less than 20% RH. Any of the following storage methods may be used.

Store the SMDs in a rigid metal container with a tight fitting lid. Place fresh desiccant (as a minimum, the equivalent of one ON Semiconductor desiccant bag per every 0.8 cubic feet) in the storage container. Desiccant is readily available at any chemical supply house. An RH indicator strip must be kept inside the container to verify that the humidity level remains below 20 percent.

Store the SMDs in a dry nitrogen purge cabinet or container that maintains the humidity level at less than 20 % RH.

For short term storage, SMDs can be resealed in the original drypack bag soon after opening. Bags opened carefully near the seal are easily resealed with either a heat seal or a tight fitting clip. Fresh desiccant may be required in equal proportion to the amount originally shipped with the bag. An RH indicator strip must be kept inside the bag to verify that the humidity level remains below 20% RH.

DRY–OUT PROCEDURES

SMDs that are not handled or stored within specification must undergo one of the following dry–out procedures prior to reflow.

125°C DRY–OUT BAKE

Bake TSOPs at 125°C (± 5°C) for four hours (+1/–0 hour). Bake all other SMDs at 125°C (± 5°C) for eight hours (+1/–0 hour). CAUTION:Do not bake SMDs in shipping trays with a temperature rating of less than 130°C. Do not bake SMDs in plastic tubes or tape and reel (T & R) packaging. Use care in handling SMDs out of their shipping container to maintain lead coplanarity.

40°C DRY–OUT BAKE

Bake TSOPs at 40°C (± 5°C) for 96 hours (± eight hours). Bake all other SMDs at 40°C (± 5°C) for 168 hours (± eight hours). NOTE: This bake is designed for SMDs in plastic tubes or T&R, and is best achieved in a dry nitrogen purge oven. Higher temperatures warp or melt plastic tubes and T&R cover tape separates from carrier tape at 60°C.

ROOM TEMPERATURE DRY–OUT

Store units per Optional Storage Methods for a minimum of 500 hours. This drying method is designed for SMDs in plastic tubes or T&R when a 40°C dry–out bake is not possible or desirable.

NOTE:
The customer must apply the same storage requirements and time limits specified in Storage Requirements to all dried SMDs

SOLDER REFLOW PROFILES

The following guidelines do not necessarily indicate the temperature extremes that can safely be applied to SMDs. In most cases and SMD can withstand higher temperatures than the standard PC board. These guidelines represent good soldering practices that will yield high quality assemblies and minimize rework.

VAPOR PHASE REFLOW

Preheat leads to a nominal temperature of 150°C at a maximum rate of 2°C per second.

Operate the reflow chamber between 215°C and 220°C maximum, with a nominal dwell time of 50 to 80 seconds above the eutectic tin/lead solder melting pint of 183°C. Dwell times should not exceed 120 seconds above the eutectic tin/lead solder melting point of 183°C.

NOTE:
Some vapor phase machines cannot provide preheat, and therefore subject boards and components to rather severe thermal shocks.

INFRARED REFLOW

Preheat leads to a temperature of 100°C minimum and a 140°C maximum rate of 2°C per second.

Generate peak lead temperatures between 205°C minimum and 235°C with a nominal dwell time of 50 to 80 seconds above the eutectic tin/lead solder melting point of 183°C. Dwell times should not exceed 120 seconds above the eutectic tin/lead solder melting point of 183°C.

NOTE:
Peak temperatures can vary greatly across the PC board during IR processes. The variables that contribute to this wide temperature range include the furnace type and the size, mass and relative location of the components on the board. Profiles must be carefully tested to determine the hottest and coolest points on the board. The hottest and coolest points should fall within the recommended temperatures. Thermocouples must be carefully attached directly to the solder joint interface between the package leads and the board with very small amounts of thermally conductive grease or epoxy.

WAVE SOLDER

Preheat leads to a temperature of 100°C minimum and 140°C maximum at a maximum rate of 2°C per second.

Generate a solder wave temperature of 245°C nominal, 265°C maximum, with a nominal dwell time of two to three seconds and a maximum dwell time of five seconds

NOTE:

The wave solder process is suitable for the SOIC, but it is not recommended for PLCC, SOJ, QFP, TSOP, PQFP, TQFP or CQFP because of the high rate of bridging and 0pen solder joints caused by shadowing effects. Thermal shock is much greater if the whole body is immersed in molten solder. Wave solder immersion tests have not been conducted on large PLCC, QFP, PQFP, TQFP and CQFP.

REFERENCE DOCUMENTS

JEDEC Test Method A112, “Moisture Induced Stress Sensitivity for Plastic Surface Mounted Devices.” JEDEC Test Method A113, “Preconditioning of Plastic Surface Mounted Devices Prior to Reliability Testing.” ON Semiconductor S.O.P. titled “Moisture Characterization and Preconditioning of Plastic Surface Mounted Devices.”

MOS Gated Device

HANDLING PRECAUTIONS

All MOS devices have insulated gates that are subject to voltage breakdown. The gate oxide for ON Semiconductor CMOS devices is about 900 Å thick and breaks down at a gate–source potential of about 100 volts. To guard against such a breakdown from static discharge or other voltage transients, the protection networks shown in Figures 1A and 1B are used on each input to the CMOS device.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged inputs are the easiest to detect because the input has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open–circuited. The effect is that the device no longer responds to signals present at the damaged input. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Another effect of static damage is that the inputs generally have increased leakage currents.

Although the input protection network does provide a great deal of protection, CMOS devices are not immune to large static voltage discharges that can be generated during handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4–15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed:

1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low–impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board are connected to an input of a CMOS device, a resistor should be used in series with the input. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. This is caused by the time constant formed by the series resistor and input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 2, two possible networks are shown using a series resistor to reduce ESD (Electrostatic Discharge) damage. For convenience, an equation for added propagation delay and rise time effects due to series resistance size is given.
5. All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic “snow”, styrofoam, or plastic trays, but should be left in their original container until ready for use.
6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 3 for an example of a typical work station.
7. Nylon or other static generating materials should not come in contact with CMOS devices.
8. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static build–up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
10. When lead–straightening or hand–soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations:
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

12. The following steps should be observed during board–cleaning operations:
    a. Vapor degreasers and baskets must be grounded to an earth ground.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when assembled printed circuit boards are grounded and a static eliminator is directed at the board.
13. The use of static detection meters for production line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of V_{DD} and V_{SS} before conducting parametric or functional testing.
17. Do not recycle shipping rails or trays. Repeated use causes deterioration of their antistatic coating.

RECOMMENDED FOR READING:

"Total Control of the Static in Your Business"

Available by writing to:
3M Company
Static Control Systems
P.O. Box 2963
Austin, Texas 78769–2963
Or by Calling:
1–800–328–1368

Section 6

Semiconductor Package Reliability and Quality

Semiconductor Package Quality and Reliability

In Brief . . .

The word quality has been used to describe many things, such as fitness for use, customer satisfaction, customer enthusiasm, what the customer says quality is, etc. These descriptions convey important truths, however, quality should be described in a way that precipitates immediate action. With that in mind, quality can be described as reduction of variability around a target, so that conformance to customer requirements and possibly expectations can be achieved in a cost effective way. This definition provides direction and potential for immediate action for a person desiring to improve quality.

The definition of quality as described above can be applied to a task, process or a whole company. If we are to reap the benefits of quality and obtain a competitive advantage, quality must be applied to the whole company.

Implementation of quality ideas company wide requires a quality plan showing: a philosophy (belief) of operation, measurable goals, training of individuals and methods of communicating this philosophy of operation to the whole organization.

ON Semiconductor, for example, believes that quality and reliability are the responsibility of every person. Participative Management is the process by which problem solving and quality improvement are facilitated at all levels of the organization through crossfunctional teams. Continuous improvement for the individual is facilitated by a broad educational program covering onsite, university and college courses. ON Semiconductor University provides leadership and administers this educational effort on a company wide basis.

Another key belief is that quality excellence is accomplished by people doing things right the first time and committed to never ending improvement. The Six Sigma (6σ) challenge is designed to convey and facilitate the idea of continuous improvement at all levels.

The following information provides an overview of the Reliability and Quality principals applicable to semiconductor packaging. For comprehensive information on ON Semiconductor's Reliability and Quality Programs, please refer to Reference Manual R&QARM.

Quality Concepts

Quality improvement for a task or a process can be quickly described in terms of the target, current status with respect to target (variability), reduction of variability (commitment to never ending improvement), customer requirements (who receives output, what are a person's requirements/ expectations) and economics (cost of nonconformance, loss function, etc.).

Application of quality to the whole company has come to be known by such names as **"Total Quality Control" (TQC); "Company Wide Quality Control" (CWQC); "Total Quality Excellence" or "Total Quality Engineering" (TQE); "Total Quality Involvement" (TQI).** These names attempt to convey the idea that quality is a process (a way of acting continuously) rather than a program (implying a beginning and an end). Nevertheless for this process to be successful it must be able to show measurable results.

''**Six Sigma** is the required capability level to approach the standard. The **standard** is **zero defects**. Our goal is to be Best-in-Class in product, sales and service." (For a more detailed explanation, contact your ON Semiconductor Representative for a pamphlet of the Six Sigma Challenge.)

Quick insight into six sigma is obtained if we realize that a six sigma process has variability which is one half of the variation allowed (tolerance, spread) by the customer requirements (i.e. natural variation is one half of the customer specification range for a given characteristic). When six sigma is achieved, virtually zero defects are observed in the output of a process/product even allowing for potential process shifts (Figure 1).

Policies, objectives and five year plans are the mechanisms for communicating the key beliefs and measurable goals to all personnel and continuously keeping them in focus. This is done at the corporate, sector, group, division, and department levels.

ON Semiconductor, for example, evaluates performance to the corporate goals of **10 fold improvement by 1989; 100 fold improvement by 1991** and achievement of **six sigma capability by 1992** by utilizing indices such as Outgoing Electrical and Visual Mechanical Quality **(AOQ)** in terms of PPM (parts per million or sometimes given in parts per billion); **% of devices with zero PPM ; product quality returns** (RMR); number of processes/products with specified **capability indices (cp, cpk); six sigma capability roadmaps; failure rates for various reliability tests** (operating life, temperature humidity bias, hast, temperature cycling, etc.); **on-time delivery; customer product evaluation and failure analysis turnaround; cost of nonconformance; productivity improvement and personnel development**.

Figure 2 shows the improvement in electrical outgoing quality for analog products over recent years in a normalized form. Figure 3 shows the number of parts with zero PPM over a period of time.

Documentation control is an important part of **statistical process control. Process mapping** (flow charting etc.) with documentation identified allows visualization and therefore optimization of the process. Figure 4 shows a portion of a flow chart for wafer fabrication. **Control plans** are an important part of Statistical Process Control, these plans identify in detail critical points where data for process control is taken, parameters measured, frequency of measurements, type of control device used, measuring equipment, responsibilities and reaction plans. Figure 5 shows a portion of a control plan for wafer fabrication. Six sigma progress is tracked by roadmaps based on the six sigma process, a portion of which is shown on Figure 6.

On-time delivery is of great importance, with the current emphasis on **just-in-time** systems. Tracking is done on an overall basis, and at the device levels.

Figure 1. A Six Sigma Process Has Virtually Zero Defects Allowing for 1.5σ Shift

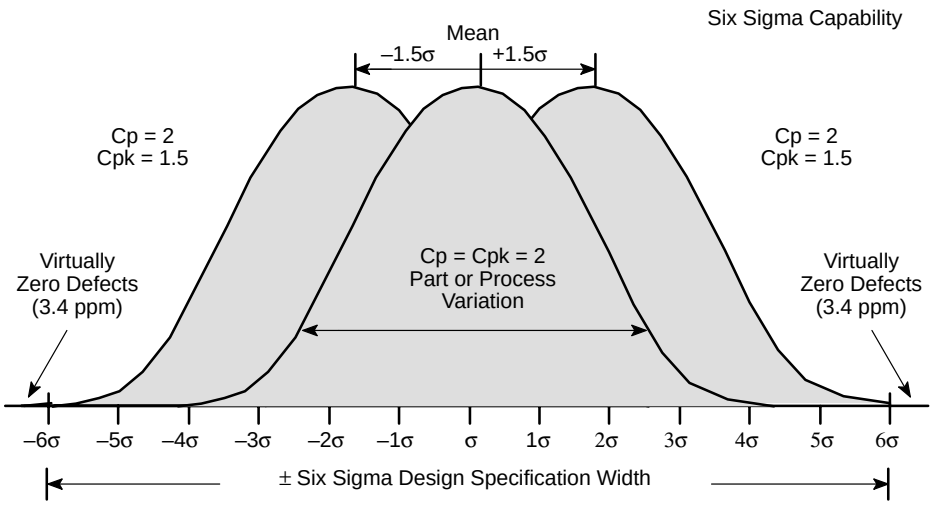
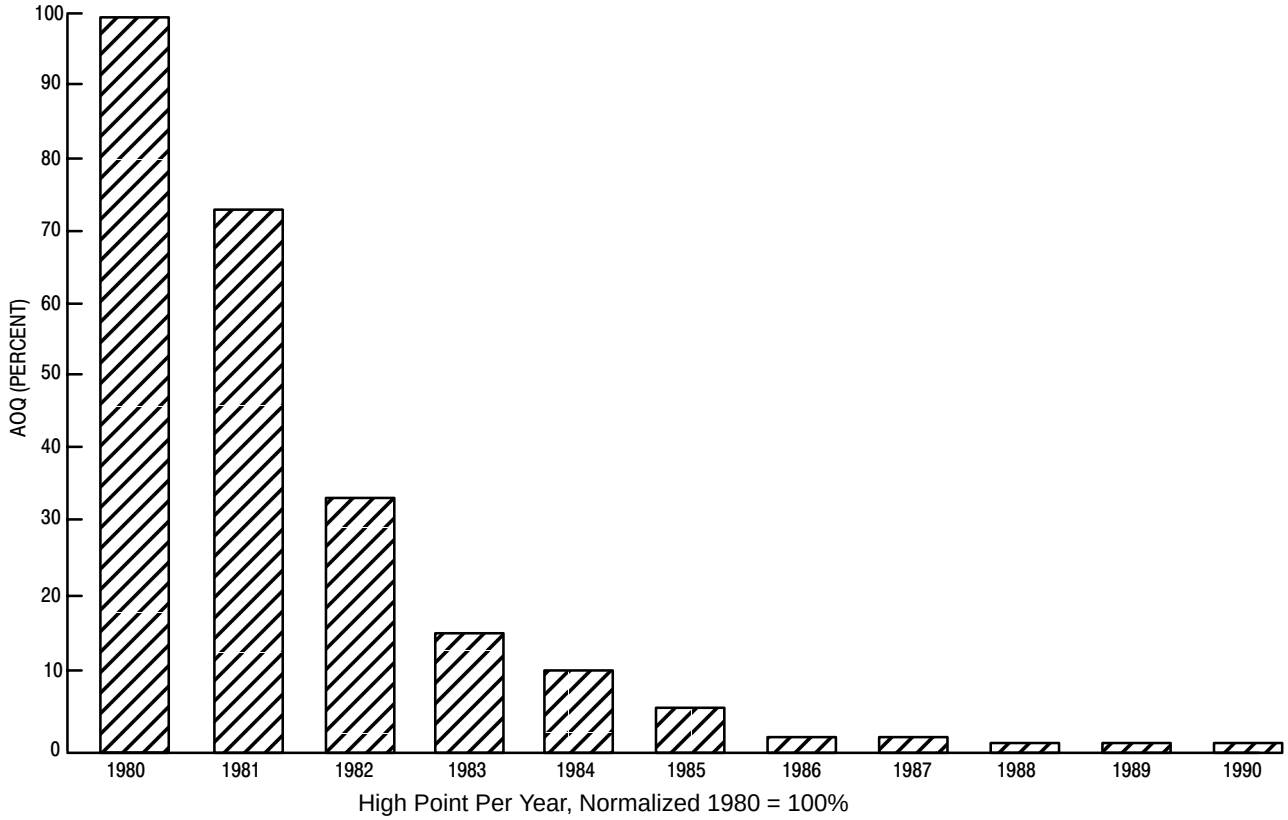
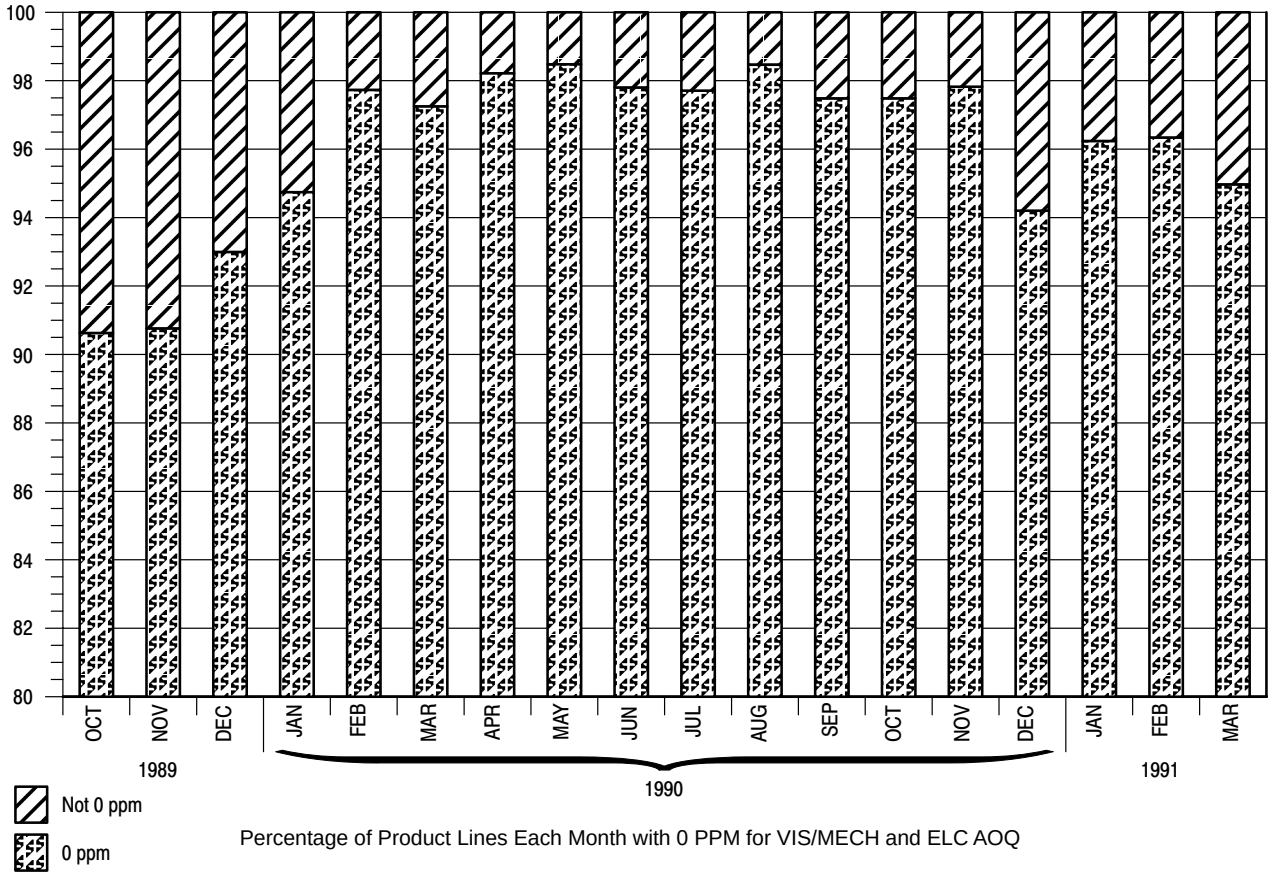


Figure 2. ON Semiconductor Logic & Analog Technologies Group Electrical AOQ



High Point Per Year, Normalized 1980 = 100%

Figure 3. Percentage of Parts with Zero PPM AOQ



Percentage of Product Lines Each Month with 0 PPM for VIS/MECH and ELC AOQ

Figure 4. Portion of a Process Flow Chart From Wafer Fab, Showing Documentation Control and SPC

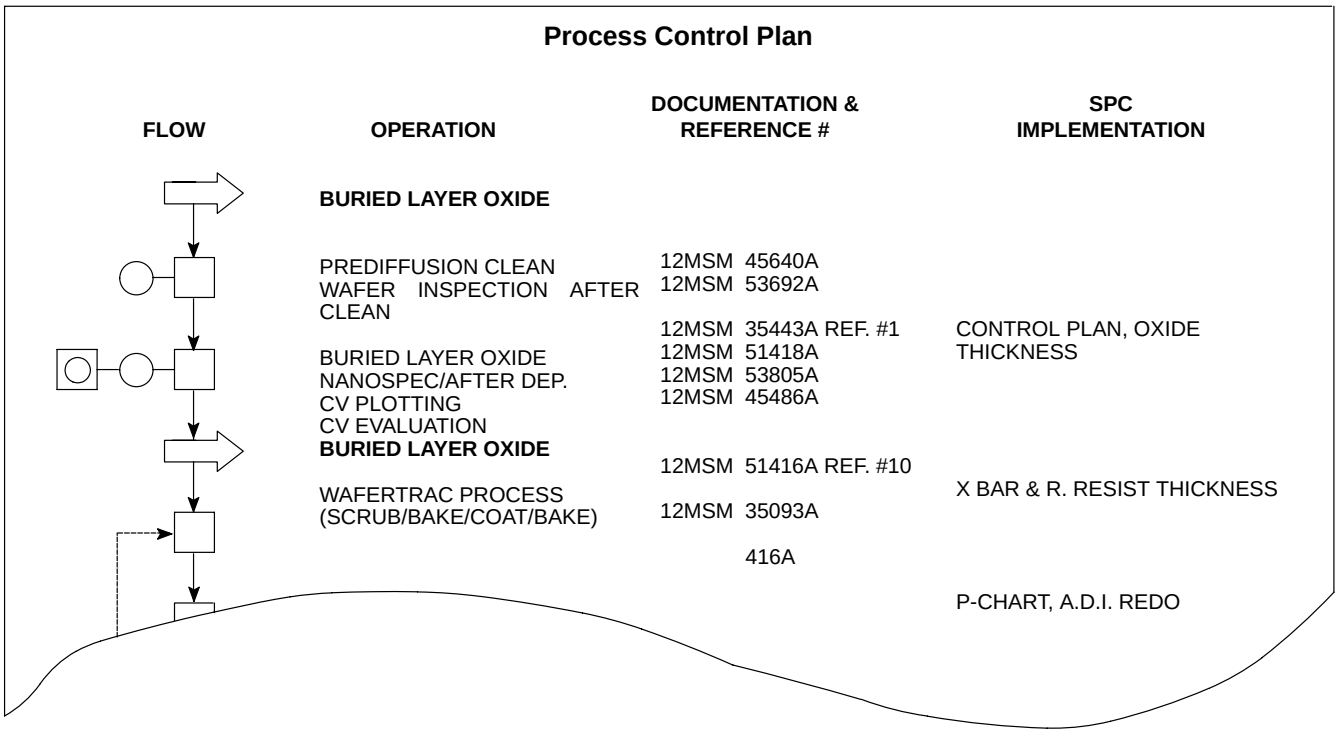


Figure 5. Part of a Wafer Fab Control Plan, Showing Statistical Process Control Details

Characteristics:	Code	Description	Code	Description
	A	VISUAL DEFECTS	E	FILM SHEET RESISTANCE
	B	VISUAL DEFECTS . . . MICROSCOPE	F	REFRACTIVE INDEX
	C	PARTICLE . . . MONITOR	G	CRITICAL DIMENSION
	D	FILM THICKNESS	H	CV PLOT

Process Location	Ref. No.	Characteristic Affected	Part/Process Detail	Measurements Method	Analysis Methods	Frequency Sample Size	Reaction Plan: Point out of Limit (3) (4)
B.L. OXIDE	1	D	OXIDE THICKNESS	NANOMETRIC	CONTROL GRAPH	EVERY RUN 3 WFR/RUN	IMPOUND LOT (1) ADJUST TIME TO CENTER PROCESS PER SPEC
EPI	2	D	THICKNESS	DIGILAB	$\overline{X}$ R CHART	EVERY RUN 5 SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		D	THICKNESS	DIGILAB	$\overline{X}$ R CHART	1WFR/SHIFT 5 SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
		E	FILM RESISTIVITY	4PT PROBE	$\overline{X}$ R CHART	EVERY RUN 5 SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		E	FILM RESISTIVITY	4PT PROBE	$\overline{X}$ R CHART	1WFR/SHIFT 5 SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
DEEP				4PT PROBE	MOVING R	EVERY LOT 1 CTRL WFR PER LOT	IMPOUND LOT NOTIFY ENGR.

Figure 6. Portion of Six Sigma (6σ) Roadmap Showing Steps to Six Sigma Capability

STEP	±6σ Summary
1. Identify critical characteristics	• Product Description • Marketing • Industrial Design • R&D/Developmental Engineering • Actual or Potential Customers
2. Determine specified product elements contributing to critical characteristics	• Critical Characteristics Matrix • Cause-and-Effect and Ishikawa Diagrams • Success Tree/Fault Tree Analysis • Component Search or Other Forms of Planned Experimentation • FMECA (Failure Mode Effects and Critical Analysis)
3. For each product element, determine the process step or process choice that affects or controls required performance	• Planned Experiments • Computer-Aided Simulation • TOP/Process Engineering Studies • Multi-Vari Analysis • Comparative Experiments
4. Determine maximum (real) allowable tolerance for each and process	• Graphing Techniques • Engineering Handbooks • Planned Experiments • Optimization, Especially Response Surface Methodology

Reliability Concepts

Reliability is the probability that an analog integrated circuit will successfully perform its specified function in a given environment for a specified period of time. This is the classical definition of reliability applied to analog integrated circuits.

Another way of thinking about reliability is in relationship to quality. While **quality** is a measure of variability (extending to potential nonconformances-rejects) in the population domain, **reliability** is a measure of variability (extending to potential nonconformances-failures) in the population, time and environmental conditions domain. In brief, **reliability** can be thought of as **quality over time** and **environmental conditions**.

Ultimately, **product reliability** is a function of proper **understanding** of **customer requirements** and **communicating** them throughout design, product/process development, manufacturing and final product use. **Quality Function Deployment (QFD)** is a technique which may be used to facilitate identification of customer quality and reliability requirements and communicating them throughout an organization.

The most frequently used reliability measure for integrated circuits is the **failure rate expressed** in percent per thousand device hours (%/1000 hrs.). If the time interval is small the failure rate is called **Instantaneous Failure Rate** [λ (t)] or "Hazard Rate." If the time interval is long (for example total operational time) the failure rate is called **Cumulative Failure Rate**.

The number of failures observed, taken over the number of device hours accumulated at the end of the observation period and expressed as a percent is called the point estimate failure rate. This however, is a number obtained from observations from a sample of all integrated circuits. If we are to use this number to estimate the failure rate of all integrated circuits (total population), we need to say something about the risk we are taking by using this estimate. A **risk** statement is provided by the **confidence level** expressed together with the failure rate. Mathematically, the failure rate at a given confidence level is obtained from the point estimate and the **CHI square** (X^2) distribution. (The X^2 is a statistical distribution used to relate the observed and expected frequencies of an event.) In

practice, a reliability calculator rule is used which gives the failure rate at the confidence level desired for the number of failures and device hours under question.

As the number of device hours increases, our confidence in the estimate increases. In integrated circuits, it is preferred to make estimates on the basis of failures per 1,000,000,000 (10^9) device hours **(FITS)** or more. If such large numbers of device hours are not available for a particular device, then the point estimate is obtained by pooling the data from devices that are similar in process, voltage, construction, design, etc., and for which we expect to see the same failure modes in the field.

The environment is specified in terms of the temperature, electric field, relative humidity, etc., by an **Eyring** type equation of the form:

$$\lambda = Ae^{-\frac{\phi}{KT}} \ldots e^{-\frac{B}{RH}} \ldots e^{-\frac{C}{E}}$$

where A, B, C, ϕ & K are constants, T is temperature, RH is relative humidity, E is the electric field, etc.

The most familiar form of this equation deals with the first exponential which shows an **Arrhenius type** relationship of the **failure rate** versus the **junction temperature** of integrated circuits, while the causes of failure generally remain the same. Thus we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then applying known acceleration factors, estimate the failure rates for lower junction temperatures. The Eyring or Arrhenius relationships should be used for failure rate projections in conjunction with proper understanding of failure modes, mechanisms and patterns such as infant mortality, constant failure rate (useful region) and wearout. For example if by design and proper process control infant mortality and useful period failures have been brought to zero and wearout failures do not start until, let us say, 30,000 hours at 125°C then failure rate projections at lower temperatures must account for these facts and whether the observed wearout failures occur at lower temperatures.

Figure 7 shows an example of a curve which gives estimates of failure rates versus temperature for an integrated circuit case study.

Arrhenius type of equation: $\lambda = Ae^{-\frac{\phi}{KT}}$

where:
- λ = Failure Rate
- A = Constant
- e = 2.72
- ϕ = Activation Energy
- K = Botzman's Constant
- T = Temperature in Degrees Kelvin

$T_J = T_A + \theta_{JA} P_D$ or $T_J = T_C + \theta_{JC} P_D$

where:
- T_J = Junction Temperature
- T_A = Ambient Temperature
- T_C = Case Temperature
- θ_{JA} = Junction to Ambient Thermal Resistance
- θ_{JC} = Junction to Case Thermal Resistance
- P_D = Power Dissipation

Life patterns (failure rate curves) for equipment and devices can be represented by an idealized graph called the **Bathtub Curve** (Figure 8).

There are three important regions identified on this curve. In Region A, the failure rate decreases with time and it is generally called **infant mortality** or early life failure region. In Region B, the failure rate has reached a relatively constant level and it is called **constant failure rate** or useful life region**.** In the third region, the failure rate increases again and it is called **wearout region**. Modern integrated circuits generally do not reach the wearout portion of the curve when operating under normal use conditions.

Figure 7. Example of a Failure Rate versus Junction Temperature Curve

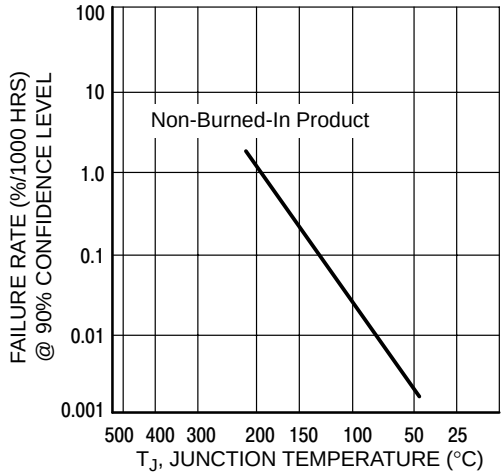
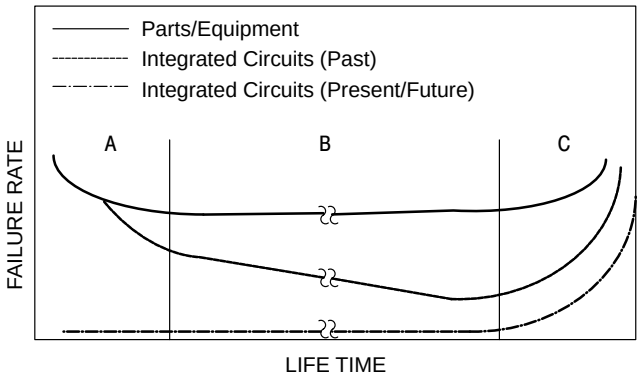


Figure 8. A Model for Failure Distribution in Time Domain Bathtub Curve Model



Decreasing Failure Rate	Constant Failure Rate	Increasing Failure Rate
Infant Mortality Burn-In Manufacturing Variations Workmanship Defects	Useful Life Random (Chance) Defects (No Pattern; Occur Regularly)	Wearout Material, Design, Process Limitations
Weibull Log Normal Gamma Distribution	Weibull Exponential for Equipment Log Normal for ICs	Weibull Normal (Gaussian)

The wearout portion of the curve can usually be identified by using highly accelerated test conditions. For modern integrated circuits, even the useful life portion of the curve may be characterized by few or no failures. As a result the bathtub

curve looks like continuously declining (few failures, Figure 8, Curve B) or zero infant and useful period failures (constant failure rate until wearout, Curve C).

The **infant mortality** portion of the curve is of most interest to equipment manufacturers because of its impact on customer perception and potential warranty costs. In recent years the infant mortality portion of the curve for integrated circuits, and even equipment, has been drastically reduced

(Figure 8, Curve C). The reduction was accomplished by improvements in technology, emphasis on statistical process control, reliability modeling in design and reliability in manufacturing (wafer level reliability, assembly level reliability, etc.). In this respect many integrated circuit families have zero or near zero failure patterns until wearout starts.

Does a user still need to consider burn-in? For this question to be answered properly the IC user must consider the **target failure rate** of the equipment, **apportioned** to the components used, application environment, maturity of equipment and components (new versus mature technology), the impact of a failure (i.e. safety versus casual loss of entertainment), maintenance costs, etc. Therefore, if the IC user is going through these considerations for the first time, the question of burn-in at the component level should be discussed during a user-vendor interface meeting.

A frequently asked question is about the reliability differences between **plastic** and **hermetic** packaged integrated circuits. In general, for all integrated circuits including analog, the field removal rates are the same for normal use environments, with many claims of plastic being better because of its ‘‘solid block” structure.

The tremendous decrease of failure rates of plastic packages has been accomplished by **continuous improvements** in piece parts, materials and processes. Nevertheless, differences can still be observed under highly accelerated environmental stress conditions. For example, if a bimetallic (gold wire and aluminum metallization) system is used in plastic packages and they are placed on a high temperature operating life test (125°C) then failures in the form of opens, at the gold to aluminum interface, may not be observed until 30,000 hours of continuous operating life. Packages, whether plastic or hermetic, with a monometallic system (aluminum wire to aluminum metallization) will have no opens because of the absence of the gold to aluminum interface. As a result, a difference in failure rates will

be observable.

Differences in failure rates between plastics and hermetics may also be observed if devices from both packaging systems are placed in a moist environment such as 85°C, 85% RH with bias applied. At some point in time plastic encapsulated ICs should fail since they are considered pervious by moisture, (the failure mechanism being corrosion of the aluminum metallization) while hermetic packages should not fail since they are considered impervious by moisture. The reason the word ‘‘should” was used is because advances in plastic compounds, package piece parts, encapsulation processes and final chip passivation have made plastic integrated circuits capable of operating more than 5000 hours without failures in an 85°C, 85% RH environment. Differences in failure rates due to internal corrosion between plastic and hermetic packages may not be observable until well after 5000 operating hours.

The aforementioned two examples had environments substantially more accelerated than normal life so the two issues discussed are not even a factor under normal use conditions. In addition, mechanisms inherent in hermetic packages but absent in plastics were not even considered

here. Improved reliability of plastic encapsulated ICs has decreased demand of hermetic packages to the point where many devices are offered only in plastic packages. The user then should feel comfortable in using the present plastic packaging systems.

A final question that is asked by the IC user is, how can one be assured that the reliability of standard product does not degrade over time? This is accomplished by our emphasis on **statistical process control, in-line reliability** assessment and **reliability auditing** by periodic and strategic sampling and accelerated testing of the various integrated circuit device packaging systems. A description of these audit programs follows.

ON Semiconductor Reliability Audit Program

The reliability of a product is a function of proper understanding of the application and environmental conditions that the product will encounter during its life as well as design, manufacturing process and final use conditions. **Inherent reliability** is the reliability which a product would have if there were no imperfections in the materials, piece parts and manufacturing processes of the product. The presence of imperfections gives rise to reliability risks. **Failure Mode and Effects Analysis (FMEA)** is a technique for identifying, controlling and eliminating potential failures from the design and manufacture of the product.

ON Semiconductor uses **on-line** and **off-line** reliability monitoring in an attempt to prevent situations which could degrade reliability. **On-line** reliability monitoring is at the **wafer and assembly levels** while **off-line** reliability monitoring involves reliability assessment of the **finished product** through the use of **accelerated** environmental tests.

Continuous monitoring of the reliability of analog integrated circuits is accomplished by the **Analog Reliability Audit Program**, which is designed to compare the actual reliability to that specified. This objective is accomplished by periodic and strategic sampling of the various integrated circuit device packaging systems. The samples are tested by subjecting them to accelerated environmental conditions and the results are reviewed for unfavorable trends that would indicate a degradation of the reliability or quality of a particular packaging system. This provides the trigger mechanism for initiating an investigation for **root cause** and **corrective action**. Concurrently, in order to provide a minimum of interruption of product flow and assure that the product is fit for use, a lot by lot sampling or a non-destructive type 100% screen may be used to assure that a particular packaging system released for shipment does have the expected reliability. This rigorous surveillance is continued until there is sufficient proof (many consecutive lots) that the problem has been corrected.

The **Logic and Analog Technologies Group** has used reliability audits since the late sixties. Such programs have been identified by acronyms such as CRP (Consumer Reliability Program), EPIIC (Environmental Package Indicators for Integrated Circuits), LAPP (Linear Accelerated Punishment Program), and RAP (Reliability Audit Program).

Currently, the Analog Reliability Audit Program consists of a **Weekly Reliability Audit** and a **Quarterly Reliability Audit**. The Weekly Reliability Audit consists of rapid (short time) types of tests used to monitor the production lines on a real time basis. This type of testing is performed at the assembly/test sites worldwide. It provides data for use as an **early warning system** for identifying negative trends and triggering investigations for root cause and corrective actions.

The Quarterly Reliability Audit consists of long term types of tests and is performed at th U.S. Bipolar Analog Division Center. The data obtained from the Quarterly Reliability Audit is used to assure that the correlation between the short term weekly tests and long term quarterly tests has not changed and a new failure mechanism has not appeared.

A large data base is established by combining the results from the Weekly Reliability Audit with the results from the Quarterly Reliability Audit. Such a data base is necessary for estimating long term failure rates and evaluating potential process improvement changes. Also, after a process improvement change has been implemented, the Analog Reliability Audit Program provides a system for monitoring the change and the past history data base for evaluating the affect of the change.

Weekly Reliability Audit

The Weekly Reliability Audit is performed by each assembly/test site worldwide. The site must have capability for final electrical and quality assurance testing, reliability testing and first level of failure analysis. The results are reviewed on a continuous basis and corrective action is taken when appropriate. The results are accumulated on a monthly basis and published.

The Reliability Audit test plan is as follows:

Electrical Measurements: Performed initially and after each reliability test, consist of critical parameters and functional testing at 25°C on a go-no-go basis.

High Temperature Operating Life: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015 with an ambient temperature of 145°C for 40 hours or equivalent based on a 1.0 eV activation energy and the Arrhenius equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction of dissimilar materials, etc. Procedures and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of –65° to +150°C or –40° to +125°C (JEDEC-STD-22-A104), for a minimum of 100 cycles.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes.

Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15 psig. The duration of the test is 96 hours (minimum).

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.

Quarterly Reliability Audit

The Quarterly Analog Reliability Audit Program is performed at the U.S. Bipolar Analog Division Center. This testing is designed to assure that the correlation between the short term weekly tests and the longer quarterly tests has not changed and that no new failure mechanisms have appeared. It also provides additional long term information for a data base for estimating failure rates and evaluation of potential process improvement changes.

Electrical Measurements: Performed initially and at interim readouts, consist of all standard DC and functional parameters at 25°C, measured on a go-no-go basis.

High Temperature Operating Life Test: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015, with an ambient temperature of 145°C for 40 and 250 hours or equivalent, based on 1.0 eV activation energy and the Arrhenius equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction, mismatch effects, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of –65° to +150°C or –40° to +125°C (JEDEC-STD-22-A104) for 100, 500 and 1000 or more cycles, depending on the temperature range used. Temperature Cycling is used more frequently than Thermal Shock.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15 psig. The duration of the test is for 96 hours (minimum), with a 48 hour interim readout.

Pressure Temperature Humidity Bias (PTHB; Biased Autoclaved): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by the moisture and the applied electrical fields. Conditions are per JEDEC-STD-22, Method 102, with bias applied, a temperature of 121°C, steam environment and 15 psig. This test detects the same type of failures as the Temperature Humidity Bias (85°C, 85% RH, with bias) test, only faster. The acceleration factor between PTHB and THB is between 20 and 40 times, depending on the type of corrosion mechanism, electrical field and packaging system.

Highly Accelerated Stress Test (HAST) is increasingly replacing the aforementioned **PTHB** test. The reason is that the **HAST** test allows control of pressure, temperature and humidity independently of each other, thus we are able to set different combinations of temperature and relative humidity. The most frequently used combination is **130°C with 85% RH**. This has been related to THB (85°C, 85% RH) by an **acceleration factor of 20** (minimum). The ability to keep the relative humidity variable constant for different temperatures is the most appealing factor of the HAST test because it reduces the determination of the acceleration factor to a single Arrhenius type of relationship. ON Semiconductor has been phasing over to HAST testing since 1985.

Temperature, Humidity and Bias (THB): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by moisture and the applied electrical fields. Conditions are per JEDEC-STD-22, Method 102 (85°C, 85% RH), with bias applied. The duration is for 1008 hours, with a 504 hour interim readout. The acceleration factor between THB (85°C, 85% RH with bias) and the 30°C, 90% RH is typically 40 to 50 times, depending on the type of corrosion mechanism, electrical field and packaging system.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test(s) are verified and characterized electrically, then they are submitted for root cause failure analysis and corrective action for continuous improvement.

OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Todays plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$\text{Eq. (1)}\quad T = (6.376 \times 10^{9})e\left[\frac{11554.267}{273.15 + T_J}\right]$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).

T_J = Device junction temperature, °C.

And:

$$\text{Eq. (2)}\quad T_J = T_A + P_D\theta_{JA} = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.

T_A = Ambient temperature, °C.

P_D = Device power dissipation in watts.

θ_{JA} = Device thermal resistance, junction to air, °C/Watt.

ΔT_J = Increase in junction temperature due to on–chip power dissipation.

Table 1 shows the relationship between junction temperature, and continuous operating time to 0.1%. bond failure, (1 failure per 1,000 bonds).

Table 1. Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 1 is graphically illustrated in Figure 7 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid–life failure rates of plastic devices are not effected by this intermetallic mechanism.

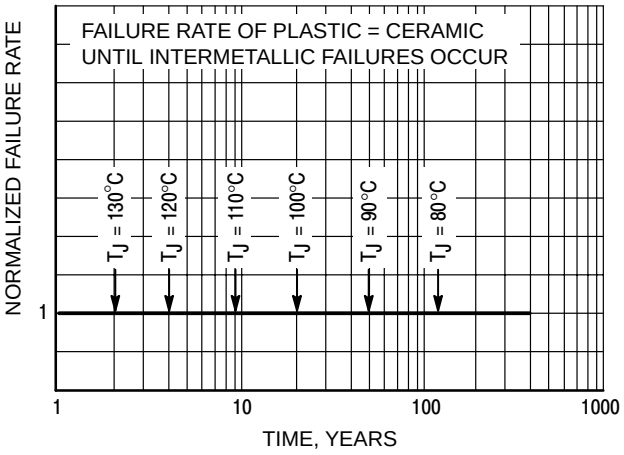


Figure 4. Failure Rate versus Time Junction Temperature

Procedure

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each device in the system should be evaluated for maximum junction temperature. Knowing the maximum junction temperature, refer to Table 1 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 7.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing. Since $\overline{\theta}_{CA}$ is entirely dependent on the application, it is the responsibility of the designer to determine its value. This can be achieved by various techniques including simulation, modeling, actual measurement, etc.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

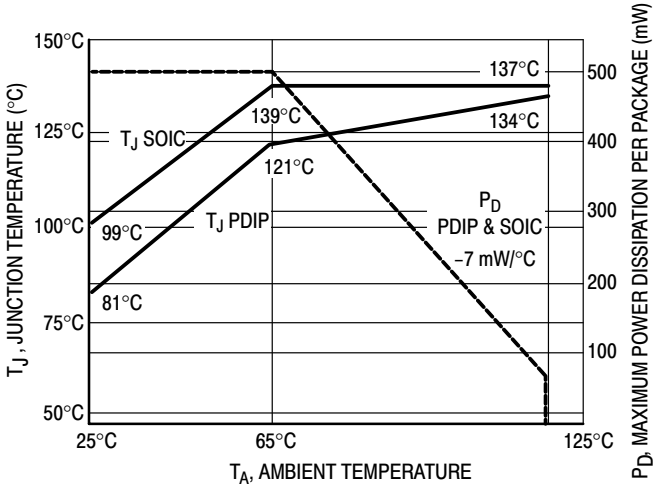


Figure 5. Junction Temperature for Worst Case CMOS Logic Device

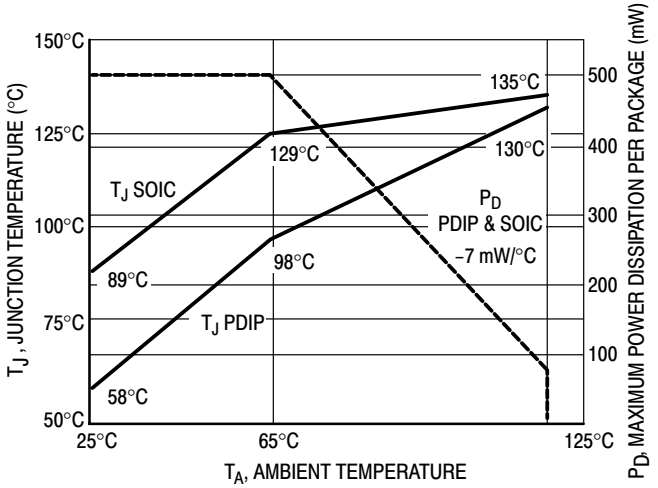


Figure 6. Junction Temperature for Typical CMOS Logic Device

This graph illustrates junction temperature for the worst case CMOS Logic device (MC14007UB) — smallest die area operating at maximum power dissipation limit in still air. The solid line indicates the junction temperature, T_J, in a Dual–In–Line (PDIP) package and in a Small Outline IC (SOIC) package versus ambient temperature, T_A. The dotted line indicates maximum allowable power dissipation derated over the ambient temperature range, 25°C to 125°C.

This graph illustrates junction temperature for a CMOS Logic device (MC14053B) — average die area operating at maximum power dissipation limit in still air. The solid line indicates the junction temperature, T_J, in a Dual–In–Line (PDIP) package and in a Small Outline IC (SOIC) package versus ambient temperature, T_A. The dotted line indicates maximum allowable power dissipation derated over the ambient temperature range, 25°C to 125°C.

STATISTICAL PROCESS CONTROL

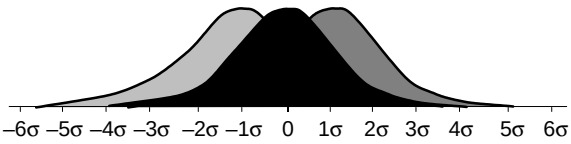
ON Semiconductor is continually pursuing new ways to improve product quality. Initial design improvement is one method that can be used to produce a superior product. Equally important to outgoing product quality is the ability to produce product that consistently conforms to specification. Process variability is the basic enemy of semiconductor manufacturing since it leads to product variability. Used in all phases of ON Semiconductor's product manufacturing, STATISTICAL PROCESS CONTROL (SPC) replaces variability with predictability. The traditional philosophy in the semiconductor industry has been adherence to the data sheet specification. Using SPC methods ensures that the product will meet specific process requirements throughout the manufacturing cycle. The emphasis is on defect prevention, not detection. Predictability through SPC methods requires the manufacturing culture to focus on constant and permanent improvements. Usually, these improvements cannot be bought with state–of–the–art equipment or automated factories. With quality in design, process, and material selection, coupled with manufacturing predictability, ON Semiconductor can produce world class products.

The immediate effect of SPC manufacturing is predictability through process controls. Product centered and distributed well within the product specification benefits ON Semiconductor with fewer rejects, improved yields, and lower cost. The direct benefit to ON Semiconductor's customers includes better incoming quality levels, less inspection time, and ship–to–stock capability. Circuit performance is often dependent on the cumulative effect of component variability. Tightly controlled component distributions give the customer greater circuit predictability. Many customers are also converting to just–in–time (JIT) delivery programs. These programs require improvements in cycle time and yield predictability achievable only through SPC techniques. The benefit derived from SPC helps the manufacturer meet the customer's expectations of higher quality and lower cost product.

Ultimately, ON Semiconductor will have Six Sigma capability on all products. This means parametric distributions will be centered within the specification limits, with a product distribution of plus or minus Six Sigma about mean. Six Sigma capability, shown graphically in Figure 1, details the benefit in terms of yield and outgoing quality levels. This compares a centered distribution versus a 1.5 sigma worst case distribution shift.

New product development at ON Semiconductor requires more robust design features that make them less sensitive to minor variations in processing. These features make the implementation of SPC much easier.

A complete commitment to SPC is present throughout ON Semiconductor. All managers, engineers, production operators, supervisors, and maintenance personnel have received multiple training courses on SPC techniques. Manufacturing has identified 22 wafer processing and 8 assembly steps considered critical to the processing of semiconductor products. Processes controlled by SPC methods that have shown significant improvement are in the diffusion, photolithography, and metallization areas.



Distribution Centered	Distribution Shifted ± 1.5
At ± 3σ 2700 ppm defective 99.73% yield	66810 ppm defective 93.32% yield
At ± 4σ 63 ppm defective 99.9937% yield	6210 ppm defective 99.379% yield
At ± 5σ 0.57 ppm defective 99.999943% yield	233 ppm defective 99.9767% yield
At ± 6σ 0.002 ppm defective 99.9999998% yield	3.4 ppm defective 99.99966% yield

Figure 1. AOQL and Yield from a Normal Distribution of Product With 6σ Capability

To better understand SPC principles, brief explanations have been provided. These cover process capability, implementation, and use.

PROCESS CAPABILITY

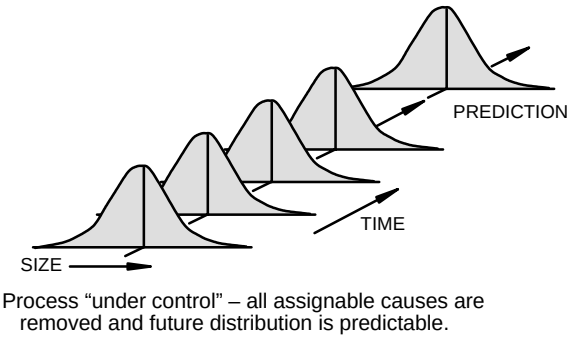
One goal of SPC is to ensure a process is **CAPABLE**. Process capability is the measurement of a process to produce products consistently to specification requirements. The purpose of a process capability study is to separate the inherent **RANDOM VARIABILITY** from **ASSIGNABLE CAUSES**. Once completed, steps are taken to identify and eliminate the most significant assignable causes. Random variability is generally present in the system and does not fluctuate. Sometimes, the random variability is due to basic limitations associated with the machinery, materials, personnel skills, or manufacturing methods. Assignable cause inconsistencies relate to time variations in yield, performance, or reliability.

Traditionally, assignable causes appear to be random due to the lack of close examination or analysis. Figure 2 shows the impact on predictability that assignable cause can have. Figure 3 shows the difference between process control and process capability.

A process capability study involves taking periodic samples from the process under controlled conditions. The performance characteristics of these samples are charted against time. In time, assignable causes can be identified and engineered out. Careful documentation of the process is the key to accurate diagnosis and successful removal of the

assignable causes. Sometimes, the assignable causes will remain unclear, requiring prolonged experimentation.

Elements which measure process variation control and capability are Cp and Cpk, respectively. Cp is the specification width divided by the process width or Cp = (specification width) / 6σ. Cpk is the absolute value of the closest specification value to the mean, minus the mean, divided by half the process width or Cpk = | closest specification – $\overline{X}$/3σ.



Process “under control” – all assignable causes are removed and future distribution is predictable.

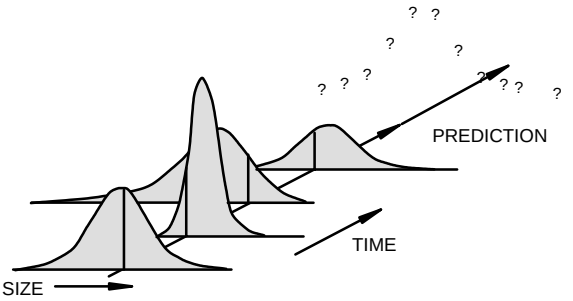
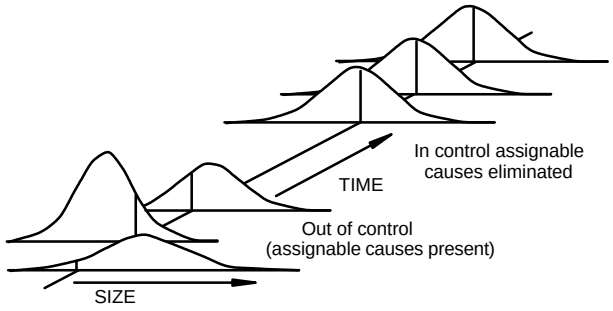


Figure 2. Impact of Assignable Causes on Process Predictable



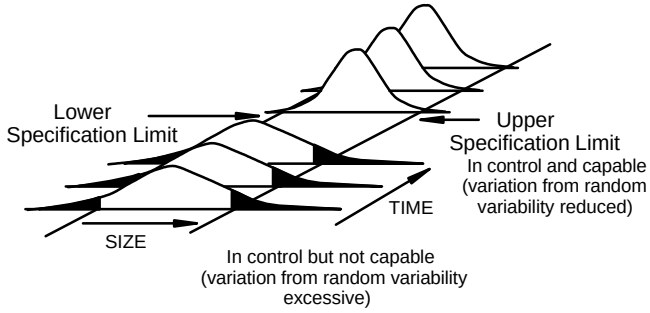


Figure 3. Difference Between Process Control and Process Capability

At ON Semiconductor, for critical parameters, the process capability is acceptable with a Cpk = 1.50 with continual improvement our goal. The desired process capability is a Cpk = 2 and the ideal is a Cpk = 5. Cpk, by definition, shows where the current production process fits with relationship to the specification limits. Off center distributions or excessive process variability will result in less than optimum conditions.

SPC IMPLEMENTATION AND USE

CPSTG uses many parameters that show conformance to specification. Some parameters are sensitive to process variations while others remain constant for a given product line. Often, specific parameters are influenced when changes to other parameters occur. It is both impractical and unnecessary to monitor all parameters using SPC methods. Only critical parameters that are sensitive to process variability are chosen for SPC monitoring. The process steps affecting these critical parameters must be identified as well. It is equally important to find a measurement in these process steps that correlates with product performance. This measurement is called a critical process parameter.

Once the critical process parameters are selected, a sample plan must be determined. The samples used for measurement are organized into **RATIONAL SUBGROUPS** of approximately two to five pieces. The subgroup size should be such that variation among the samples within the subgroup remain small. All samples must come from the same source e.g., the same mold press operator, etc. Subgroup data should be collected at appropriate time intervals to detect variations in the process. As the process begins to show improved stability, the interval may be increased. The data collected must be carefully documented and maintained for later correlation. Examples of common documentation entries are operator, machine, time, settings, product type, etc.

Once the plan is established, data collection may begin. The data collected with generate $\overline{X}$ and R values that are plotted with respect to time. $\overline{X}$ refers to the mean of the values within a given subgroup, while R is the range or greatest value minus least value. When approximately 20 or more $\overline{X}$ and R values have been generated, the average of these values is computed as follows:

$$\overline{\overline{X}} = (\overline{X} + \overline{X}2 + \overline{X}3 + \ldots)/K$$
$$\overline{R} = (R1 + R2 + R2 + \ldots)/K$$

where K = the number of subgroups measured.

The values of X and $\overline{R}$ are used to create the process control chart. Control charts are the primary SPC tool used to signal a problem. Shown in Figure 4, process control charts show $\overline{X}$ and R values with respect to time and concerning reference to upper and lower control limit values. Control limits are computed as follows:

R upper control limit = $UCL_R = D4\ \overline{R}$
R lower control limit = $LCL_R = D3\ \overline{R}$
$\overline{X}$ upper control limit = $UCL_{\overline{X}} = X + A2\ \overline{R}$
$\overline{X}$ lower control limit = $LCL_{\overline{X}} = X - A2\ \overline{R}$

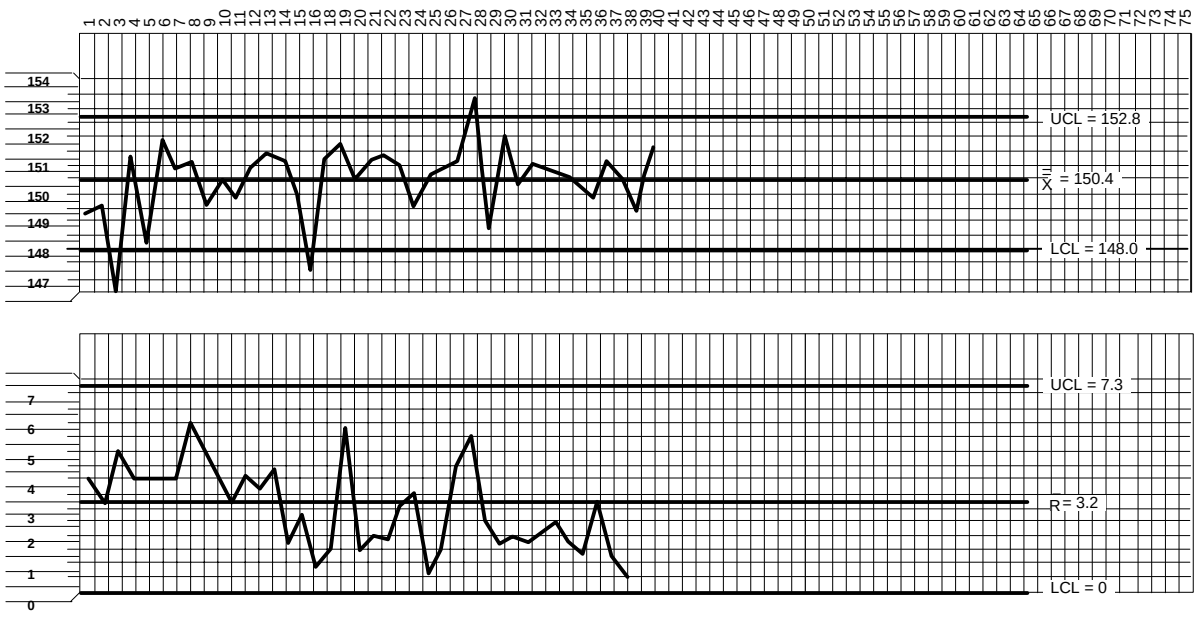


Figure 4. Example of Process Control Chart Showing Oven Temperature Data

Where D4, D3, and A2 are constants varying by sample size, with values for sample sizes from 2 to 10 shown in the following partial table:

n	2	3	4	5	6	7	8	9	10
D_4	3.27	2.57	2.28	2.11	2.00	1.92	1.86	1.82	1.78
D_3	*	*	*	*	*	0.8	0.14	0.18	0.22
A_2	1.88	1.02	0.73	0.58	0.48	0.42	0.37	0.34	0.31

*For sample sizes below 7, the LCL_R would technically be a negative number; in those cases there is no lower control limit; this means that for a subgroup size 6, six "identical" measurements would not be unreasonable.

Control charts are used to monitor the variability of critical process parameters. The R chart shows basic problems with piece to piece variability related to the process. The X chart can often identify changes in people, machines, methods, etc. The source of the variability can be difficult to find and may require experimental design techniques to identify assignable causes.

Some general rules have been established to help determine when a process is **OUT–OF–CONTROL**. Figure 5 shows a control chart subdivided into zones A, B, and C corresponding to 3 sigma, 2 sigma, and 1 sigma limits respectively. In Figures 6 through 9 four of the tests that can be used to identify excessive variability and the presence of assignable causes are shown. As familiarity with a given process increases, more subtle tests may be employed successfully.

Once the variability is identified, the cause of the variability must be determined. Normally, only a few factors have a significant impact on the total variability of the process. The importance of correctly identifying these factors is stressed in the following example. Suppose a process variability depends on the variance of five factors A, B, C, D, and E. Each has a variance of 5, 3, 2, 1, and 0.4, respectively.
Since:

$$\sigma \text{ tot} = \sqrt{\sigma A^2 + \sigma B^2 + \sigma C^2 + \sigma D^2 + \sigma E^2}$$

$$\sigma \text{ tot} = \sqrt{5^2 + 3^2 + 2^2 + 1^2 + (0.4)^2} = 6.3$$

If only D is identified and eliminated, then:

$$\sigma \text{ tot} = \sqrt{5^2 + 3^2 + 2^2 + (0.4)^2} = 6.2$$

This results in less than 2% total variability improvement. If B, C, and D were eliminated, then:

$$\sigma \text{ tot} = \sqrt{5^2 + (0.4)^2} = 5.02$$

This gives a considerably better improvement of 23%. If only A is identified and reduced from 5 to 2, then:

$$\sigma \text{ tot} = \sqrt{2^2 + 3^2 + 2^2 + 1^2 + (0.4)^2} = 4.3$$

Identifying and improving the variability from 5 to 2 yields a total variability improvement of nearly 40%.

Most techniques may be employed to identify the primary assignable cause(s). Out–of–control conditions may be correlated to documented process changes. The product may be analyzed in detail using best versus worst part comparisons or Product Analysis Lab equipment. Multi–variance analysis

can be used to determine the family of variation (positional, critical, or temporal). Lastly, experiments may be run to test theoretical or factorial analysis. Whatever method is used, assignable causes must be identified and eliminated in the most expeditious manner possible.

After assignable causes have been eliminated, new control limits are calculated to provide a more challenging variability criteria for the process. As yields and variability improve, it may become more difficult to detect improvements because they become much smaller. When all assignable causes have been eliminated and the points remain within control limits for 25 groups, the process is said to in a state of control.

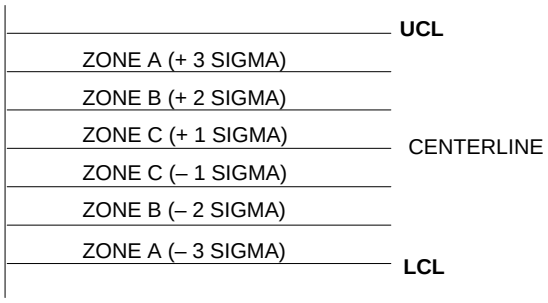


Figure 5. Control Chart Zones

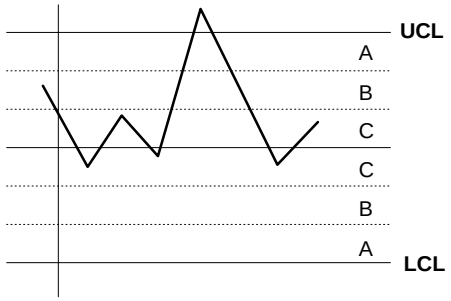


Figure 6. One Point Outside Control Limit Indicating Excessive Variability

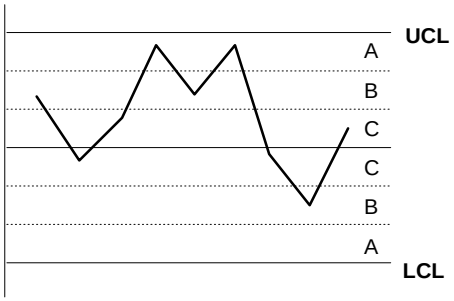


Figure 7. Two Out of Three Points in Zone A or Beyond Indicating Excessive Variability

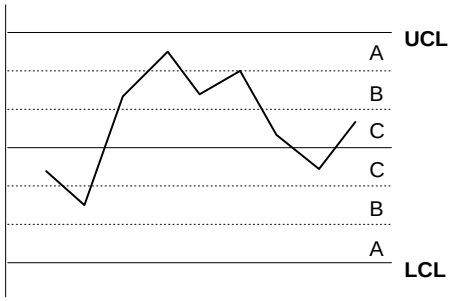


Figure 8. Four Out of Five Points in Zone B or Beyond Indicating Excessive Variability

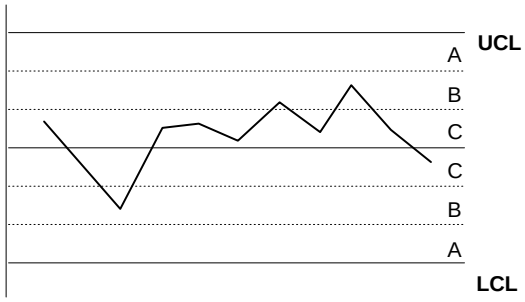


Figure 9. Seven Out of Eight Points in Zone C or Beyond Indicating Excessive Variability

SUMMARY

ON Semiconductor is committed to the use of STATISTICAL PROCESS CONTROLS. These principles, used throughout manufacturing have already resulted in many significant improvements to the processes. Continued dedication to the SPC culture will allow ON Semiconductor to reach the Six Sigma and zero defect capability goals. SPC will further enhance the commitment to **TOTAL CUSTOMER SATISFACTION**.

Appendix A

Applicable Standards

APPENDIX A: APPLICABLE STANDARDS

The following list contains applicable Electronic Industries Association (EIA) JEDEC Standards. These may be obtained by accessing the JEDEC website at www.JEDEC.org

JESD30–B Descriptive Designation System for Semiconductor–Device Packages

JESD1 JEDEC Standard 1, Leadless Chip Carrier Pinouts Standardized for Linear's

JESD2 JEDEC Standard 2, Digital Bipolar Pinouts for Chip Carriers

JESD4 JEDEC Standard 4, Definition of External Clearance and Creepage Distances of Discrete Semiconductor Packages for Thyristors and Rectifiers

JESD9–A JEDEC Standard 9–A, Metal Package Specification for Microelectronic Packages

JESD11 JEDEC Standard 11, Chip Carrier Pinouts Standardized for CMOS 4000, HC and HCT Series of Logic Circuits

JESD27 JEDEC Standard 27, Ceramic Package Specification for Microelectronic Packages

JESD51 JEDEC Standard 51, Methodology for the Thermal Measurement of Component Packages

JESD51–1 JEDEC Standard 51, Addendum No. 1, Integrated Circuit Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device)

JESD51–2 JEDEC Standard 51, Addendum No. 2, Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)

JESD51–3 JEDEC Standard 51, Addendum No. 3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

JESD51–4 JEDEC Standard 51, Addendum No. 4, Thermal Test Chip Guideline (Wire Bond Type Chip)

JESD51–5 JEDEC Standard 51, Addendum No. 5, Extension of Thermal Test board Standards for Packages with direct Thermal Attachment Mechanisms

JESD51–6 JEDEC Standard 51, Addendum No. 6, Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)

JESD51–7 JEDEC Standard 51, Addendum No. 7, High Effective Thermal Conductivity Test Board for Leaded Surface mount Packages

JESD51–8 JEDEC Standard 51, Addendum No. 8, Integrated Circuit Thermal Test Method Environmental Conditions – Junction–to–Board

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A Data Sheet is the fundamental publication for each individual product/device, or series of products/devices, containing detailed parametric information and any other key information needed in using, designing–in or purchasing of the product(s)/device(s) it describes. Below are the three classifications of Data Sheet: Product Preview; Advance Information; and Fully Released Technical Data

PRODUCT PREVIEW

A Product Preview is a summary document for a product/device under consideration or in the early stages of development. The Product Preview exists only until an "Advance Information" document is published that replaces it. The Product Preview is often used as the first section or chapter in a corresponding reference manual. The Product Preview displays the following disclaimer at the bottom of the first page: "This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice."

ADVANCE INFORMATION

The Advance Information document is for a device that is NOT fully qualified, but is in the final stages of the release process, and for which production is eminent. While the commitment has been made to produce the device, final characterization and qualification may not be complete. The Advance Information document is replaced with the "Fully Released Technical Data" document once the device/part becomes fully qualified. The Advance Information document displays the following disclaimer at the bottom of the first page: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

FULLY RELEASED TECHNICAL DATA

The Fully Released Technical Data document is for a product/device that is in full production (i.e., fully released). It replaces the Advance Information document and represents a part that is fully qualified. The Fully Released Technical Data document is virtually the same document as the Product Preview and the Advance Information document with the exception that it provides information that is unavailable for a product in the early phases of development, such as complete parametric characterization data. The Fully Released Technical Data document is also a more comprehensive document than either of its earlier incarnations. This document displays no disclaimer, and while it may be informally referred to as a "data sheet," it is not labeled as such.

DATA BOOK

A Data Book is a publication that contains primarily a collection of Data Sheets, general family and/or parametric information, Application Notes and any other information needed as reference or support material for the Data Sheets. It may also contain cross reference or selector guide information, detailed quality and reliability information, packaging and case outline information, etc.

APPLICATION NOTE

An Application Note is a document that contains real–world application information about how a specific ON Semiconductor device/product is used, or information that is pertinent to its use. It is designed to address a particular technical issue. Parts and/or software must already exist and be available.

SELECTOR GUIDE

A Selector Guide is a document published, generally at set intervals, that contains key line–item, device–specific information for particular products or families. The Selector Guide is designed to be a quick reference tool that will assist a customer in determining the availability of a particular device, along with its key parameters and available packaging options. In essence, it allows a customer to quickly "select" a device. For detailed design and parametric information, the customer would then refer to the device's Data Sheet. The *Master Components Selector Guide* (SG388/D) is a listing of **ALL** currently available ON Semiconductor devices.

REFERENCE MANUAL

A Reference Manual is a publication that contains a comprehensive system or device–specific descriptions of the structure and function (operation) of a particular part/system; used overwhelmingly to describe the functionality or application of a device, series of devices or device category. Procedural information in a Reference Manual is limited to less than 40 percent (usually much less).

HANDBOOK

A Handbook is a publication that contains a collection of information on almost any give subject which does not fall into the Reference Manual definition. The subject matter can consist of information ranging from a device specific design information, to system design, to quality and reliability information.

ADDENDUM

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