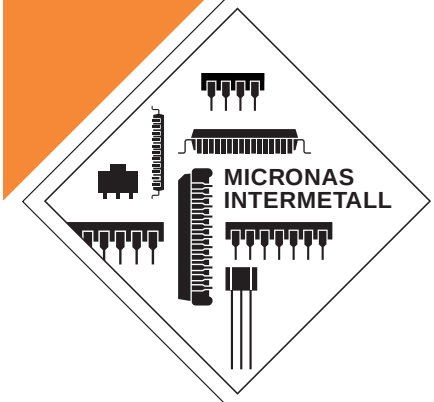


PRELIMINARY DATA SHEET

BSP 3501C
Baseband
Sound Processor

Edition March 16, 1998
6251-469-1PD

MICRONAS
INTERMETALL

Contents

Baseband Sound Processor

Release Notes: The hardware description in this document is valid for the BSP 3501C–A1 and newer codes.

1. Introduction

The **BSP 3501C** is designed as single-chip Baseband Sound Processor for applications in analog and digital TV sets, satellite receivers, and video recorders.

The BSP 3501C CMOS version is fully pin and software compatible to the MSP 34xx family. The main difference between the BSP 3501C and the MSP 34xx is that the BSP 3501C cannot demodulate any SIF-input signal.

The BSP 3501C is available in PLCC68, PSDIP64, PSDIP52, and PQFP80 packages.

BSP 3501C Integrated Functions:
– volume, balance, bass, treble, loudness for loudspeaker and headphone output
– automatic volume correction (A.V.C.)
– 5 band graphic equalizer
– subwoofer output alternatively with headphone output
– spatial effect (pseudostereo/basewidth enlargement)
– 3 pairs of D/A converters
– 1 pair of A/D converters
– SCART switches

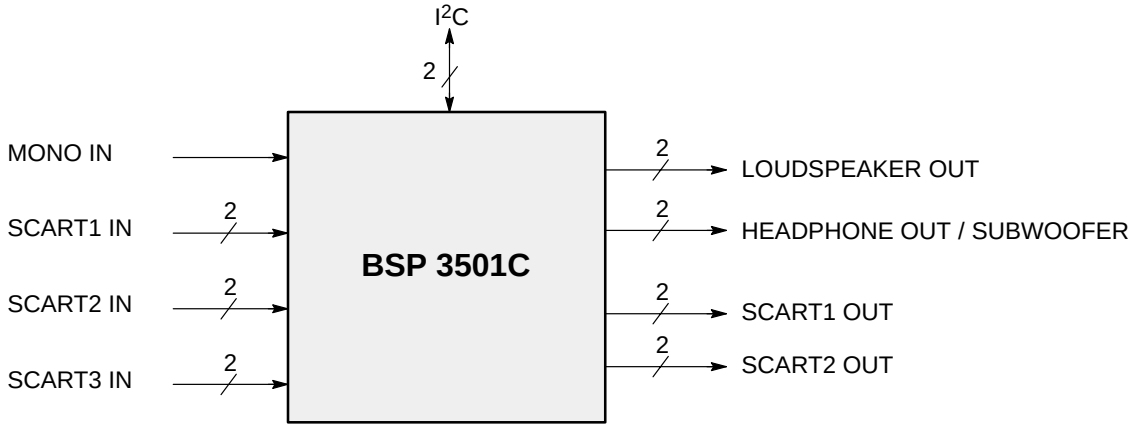


Fig. 1–1: Main I/O Signals BSP 3501C

1.1. Features of the DSP-Section

– flexible selection of audio sources to be processed

– digital baseband processing: volume, bass, treble, 5-band equalizer, loudness, pseudostereo, and base-width enlargement

– simple controlling of volume, bass, treble, equalizer etc.

1.2. Features of the Analog Section

– three selectable analog pairs of audio baseband inputs (= three SCART inputs)
input level: ≤2 V RMS,
input impedance: ≥25 kΩ

– one selectable analog mono input (i.e. AM sound),
input level: ≤2 V RMS,
input impedance: ≥10 kΩ

– two high quality A/D converters, S/N-Ratio: ≥85 dB

– 20 Hz to 20 kHz Bandwidth for SCART-to-SCART-Copy facilities

– MAIN (loudspeaker) and AUX (headphones): two pairs of 4-fold oversampled D/A-converters
output level per channel: max. 1.4 V RMS
output resistance: max. 5 kΩ
S/N-Ratio: ≥85 dB at maximum volume
max. noise voltage in mute mode: ≤10 µV (BW: 20 Hz ...16 kHz)

– one pair of four-fold oversampled D/A-converters supplying two selectable pairs of SCART-Outputs. Output level per channel: max. 2 V RMS, output resistance: max. 0.5 kΩ, S/N-Ratio: ≥85 dB
(20 Hz...16 kHz)

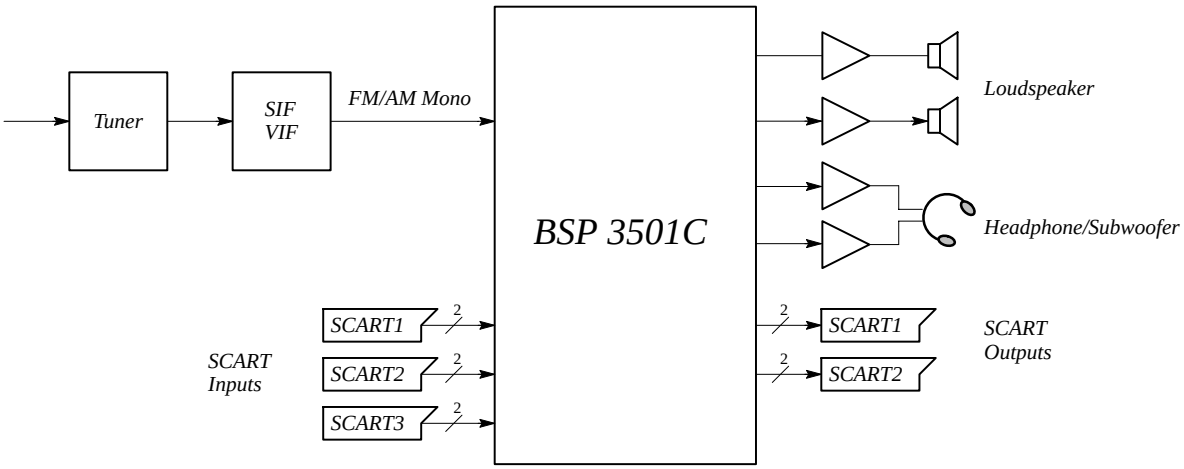


Fig. 1–2: Typical **BSP 3501C** application

2. Architecture of the BSP 3501C

Fig. 2–1 shows a simplified block diagram of the IC. Its architecture is split into two functional blocks:

1. digital signal processing (DSP) section performing audio baseband processing

2. analog section containing two A/D-converters, 6 D/A-converters, and SCART switching facilities

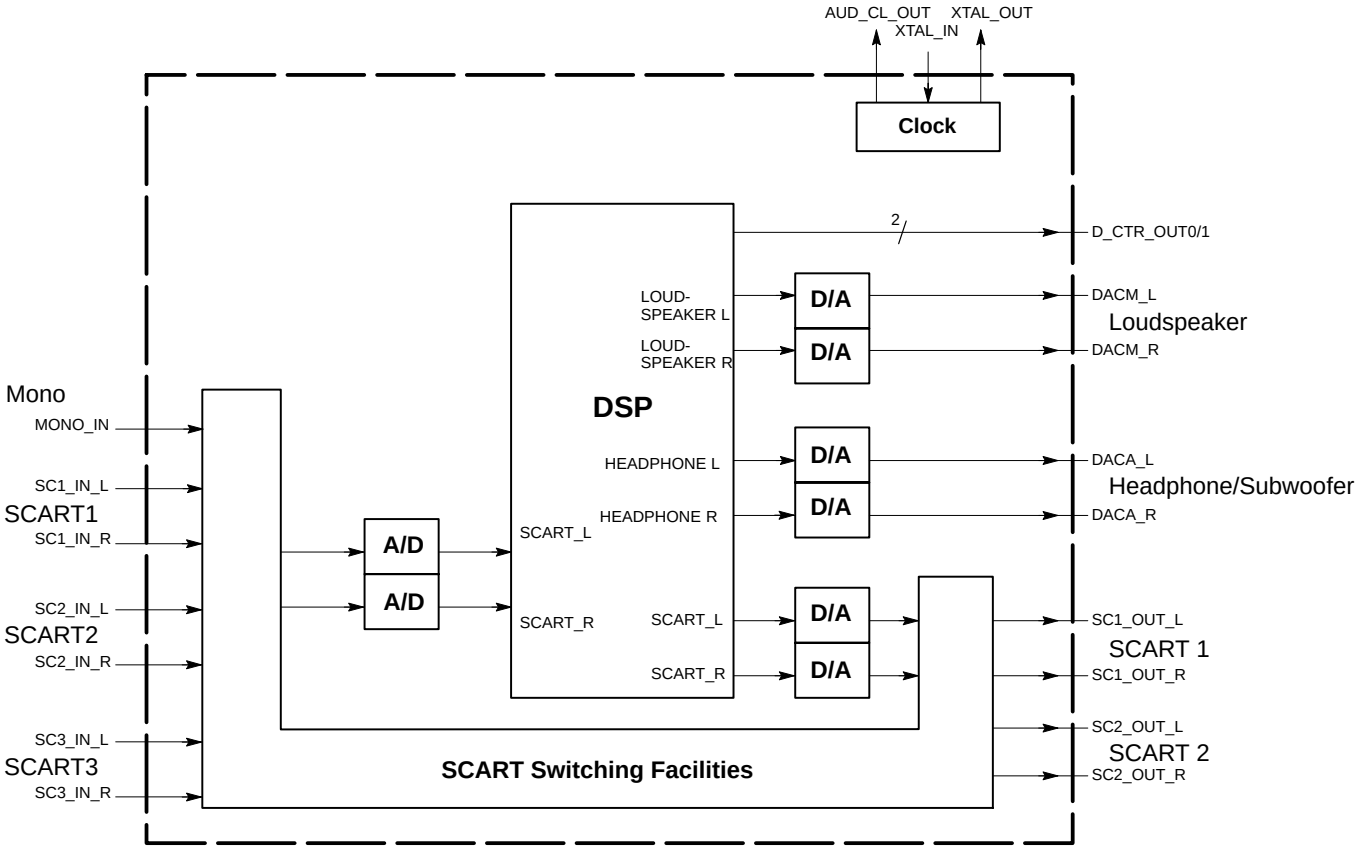


Fig. 2–1: Architecture of the BSP 3501C

2.1. Analog Section and SCART Switching Facilities

The analog input and output sections offer a wide range of switching facilities, which are shown in Fig. 2–2. To design a TV-set with 3 pairs of SCART-inputs and two pairs of SCART-outputs, no external switching hardware is required.

The switches are controlled by the ACB bits defined in the audio processing interface (see section 4.2. Summary of the DSP Control Registers for Audio Baseband Processing).

If the BSP 3501C is switched off by first pulling STANDBYQ low, and then disconnecting the 5 V, but keeping the 8 V power supply (**'Standby'-mode**), the switches S1, S2, and S3 maintain their position and function. This facilitates the copying from selected SCART-inputs to SCART-outputs in the TV-sets standby mode.

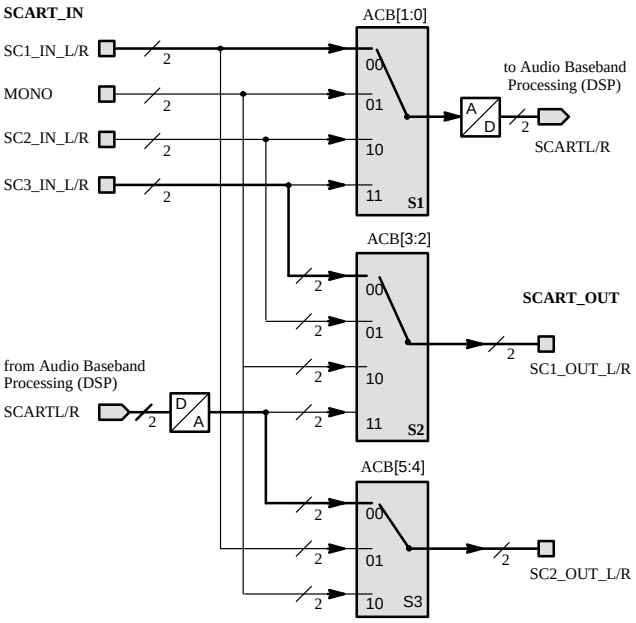


Fig. 2–2: SCART-Switching Facilities
Bold lines determine the default configuration

In case of power-on start or starting from standby, the IC switches automatically to the default configuration, shown in Fig. 2–2. This takes place after the first I^2C transmission into the DSP part. By transmitting the ACB register first, the default setting mode can be changed.

2.2. BSP 3501C Audio Baseband Processing

All audio baseband functions are performed by digital signal processing (DSP). The DSP functions are grouped into three processing parts: input preprocessing, channel source select, and channel postprocessing.

All input and output signals can be processed simultaneously.

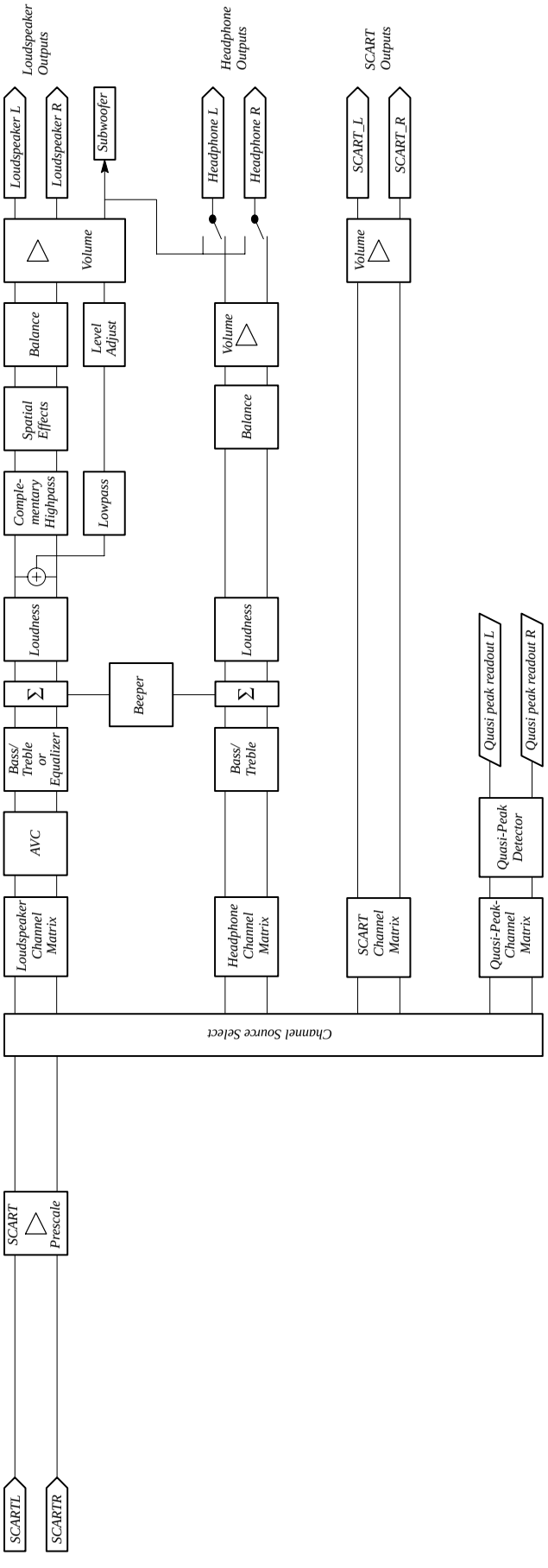


Fig. 2–3: Audio baseband processing (DSP-Firmware)

3. I²C Bus Interface: Device and Subaddresses

As a slave receiver, the BSP 3501C can be controlled via I²C bus. Access to internal memory locations is achieved by subaddressing. The Mode Register and the audio baseband processor (DSP) have two separate subaddressing register banks.

In order to allow for more BSP 3501C ICs to be connected to the control bus, an ADR_SEL pin has been implemented. With ADR_SEL pulled to high, the BSP 3501C responds to changed device addresses, thus two identical devices can be selected.

By means of the RESET bit in the CONTROL register, all devices with the same device address are reset.

The IC is selected by asserting a special device address in the address part of an I²C transmission. A device address pair is defined as a write address (80 hex or 84 hex) and a read address (81 hex or 85 hex). Writing is done by sending the device write address first, followed by the subaddress byte, two address bytes, and two data bytes. For reading, the read address has to be transmitted first by sending the device write address (80 hex or 84 hex), followed by the subaddress byte, and two address bytes. Without sending a stop condition, reading of the addressed data is done by sending the device read address (81 hex or 85 hex) and reading two bytes of data. Refer to Fig. 3–1 I²C Bus Protocol and section 3.2. Proposal for BSP 3501C I²C Telegrams.

Due to the internal architecture of the BSP 3501C, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms. If the addressed processor is not ready for further transmissions on the I²C bus, the clock line I2C_CL is pulled low. This puts the current transmission into a wait state. After a certain period of time, the BSP 3501C releases the clock, and the interrupted transmission is carried on.

The I²C Bus lines can be set tristate by switching the IC into “Standby”-mode.

I²C-Bus error conditions:
In case of any internal error, the BSP’s wait-period is extended to 1.77 ms. Afterwards, the BSP does not acknowledge (NAK) the device address. The data line will be left HIGH by the BSP, and the clock line will be released. The master can then generate a STOP condition to abort the transfer.

By means of NAK, the master is able to recognize the error state and to reset the IC via I²C-Bus. While transmitting the reset protocol (section. 3.2.4.) to ‘CONTROL’, the master must ignore the not acknowledge bits (NAK) of the BSP.

A detailed timing diagram is shown in Fig. 3–1 and Fig. 3–2.

Table 3–1: I²C Bus Device Addresses

ADR_SEL	Low		High		Left Open	
Mode	**Write**	**Read**	**Write**	**Read**	**Write**	**Read**
BSP device address	80 hex	81 hex	84 hex	85 hex	88 hex	89 hex

Table 3–2: I²C Bus Device and Subaddresses

Name	Binary Value	Hex Value	Function
CONTROL	0000 0000	00	software reset
TEST1	0000 0001	01	only for internal use
TEST2	0000 0010	02	only for internal use
MODE_REG	0001 0000	10	write address Mode Register
WR_DSP	0001 0010	12	write address DSP
RD_DSP	0001 0011	13	read address DSP
PLL_CAP	0001 1111	1F	read / write PLL_Cap

Table 3–3: Control Register

Name	15	14..0
CONTROL	RESET	0

3.1. Protocol Description

Write to MODE_REG or DSP (long protocol)

S	daw	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from DSP (long protocol)

S	daw	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	dar	Wait	ACK	data-byte high	ACK	data-byte low	NAK	P

Write to Control / Test / PLL_Cap Registers (short protocol)

S	daw	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from Control / Test / PLL_Cap Registers (short protocol)

S	daw	Wait	ACK	sub-addr	ACK	S	dar	Wait	ACK	data-byte high	ACK	data-byte low	NAK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
daw = Device Address Write
dar = Device Address Read
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= BSPC, grey) or master (= CCU, hatched)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (= CCU, hatched) to indicate 'End of Read' or from BSPC indicating internal error state (not illustrated)
Wait = I^2C-Clock line held low by the slave (= BSPC) while interrupt is serviced (<1.77 ms)

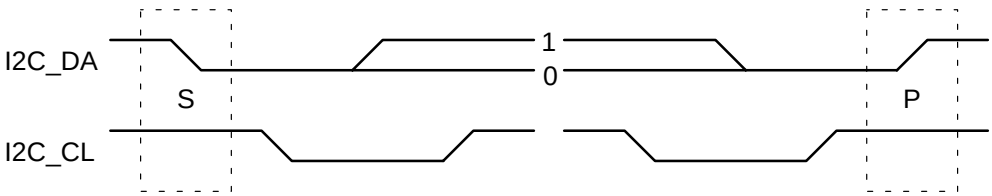


Fig. 3–1: I^2C bus protocol (MSB first; data must be stable while clock is high)

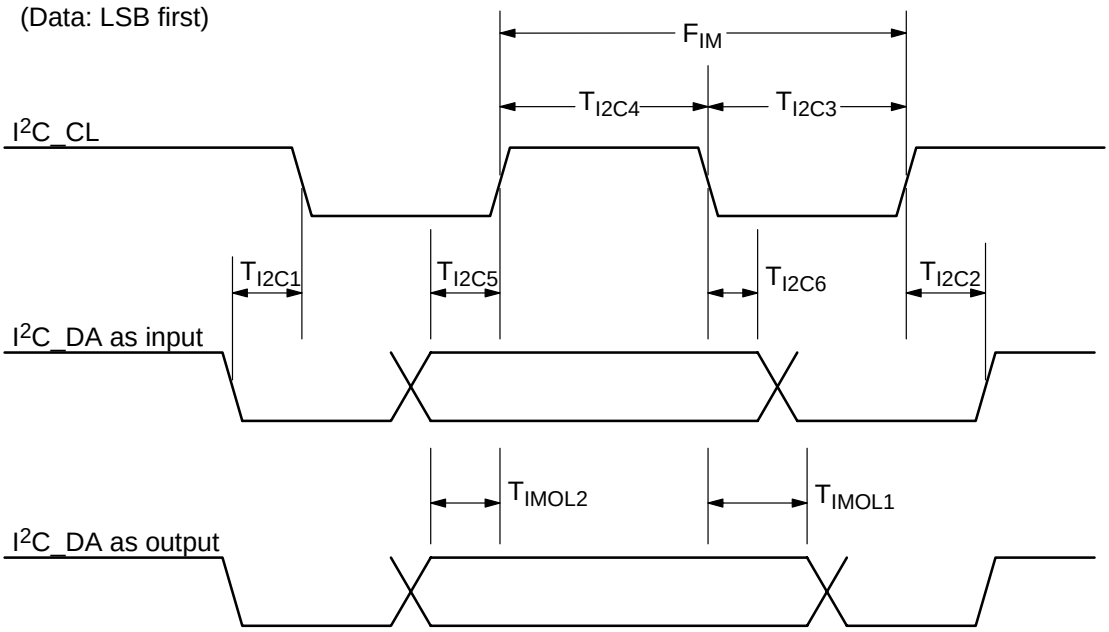


Fig. 3–2: I^2C bus timing diagram

3.2. Proposal for BSP 3501C I^2C Telegrams

3.2.1. Symbols

daw	device address write
dar	device address read
<	Start Condition
>	Stop Condition
aa	Address Byte
dd	Data Byte

3.2.2. Write Telegrams

`<daw 00 dd dd>`	software RESET
`<daw 12 aa aa dd dd>`	write data into DSP register

3.2.3. Read Telegrams

`<daw 13 aa aa <dar dd dd>`	read data from DSP

3.2.4. Examples

`<daw 00 80 00>`	RESET BSPC statically
`<daw 00 00 00>`	clear RESET
`<daw 12 00 08 02 20>`	set loudspeaker channel source to SCART

3.3. Start Up Sequence

After power on or RESET, the IC is in an inactive state. The CCU has to transmit the required coefficient set for a given operation via the I^2C bus. Initialization must start with the Mode Register.

The reset pin should not be >0.45 DVSUP (see recommended operation conditions) before the 5 Volt digital power supply (DVSUP) and the analog power supply (AVSUP) are >4.75 Volt **and** the BSP-Clock is running (Delay: 2 ms max, 0.5 ms typ.).

This means, if the reset low-high edge starts with a delay of 2 ms after DVSUP>4.75 Volt and AVSUP>4.75 Volt, even under worst case conditions, the reset is ok.

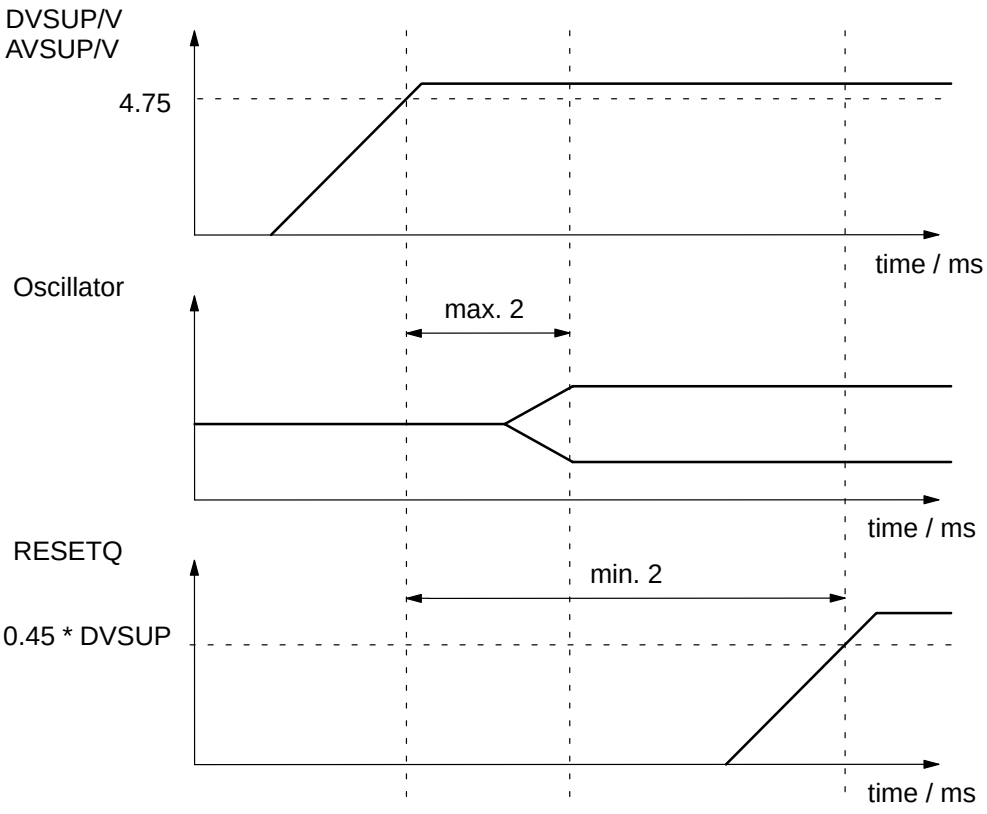


Fig. 3–3: Power-up sequence

Note: The reset should not reach high level before the oscillator has started. This requires a reset delay of >2 ms

4. Programming the BSP 3501C

4.1. Control Register ‘MODE_REG’

The register ‘MODE_REG’ contains the control bits determining the operation mode of the BSP 3501C; Table 4–1 explains all bit positions.

The transmission on the control bus is 16 bits wide, with 12 significant bits to be inserted LSB bound and filled with zero bits into the 16 bit transmission word.

Table 4–1: Control word ‘MODE_REG’: All bits are “0” after power-on-reset

Register	**Protocol**	**Write Address (hex)**	**Function**
MODE_REG	long	0083	mode register
Bit	**Function**	**Comment**	**Definition**
[0]	not used		must be 0
[1]	DCTR_TRI	Digital_Control_Output tristate	0 : active 1 : tristate
[2]	not used		must be 1
[3–4]	not used		must be 0
[5]	Audio_CL_OUT	Audio_Clock_Output tristate	0 : on 1 : tristate
[6–9]	not used		must be 0
[10]	not used		must be 1
[11–15]	not used		must be 0

4.2. Summary of the DSP Control Registers for Audio Baseband Processing

Control registers are 16 bit wide. Transmissions via I^2C bus have to take place in 16 bit words. Single data entries are 8 bit. Some of the defined 16 bit words are divided into low and high byte, thus holding two different control entities. All control registers are readable.
Note: Unused parts of the 16 bit registers must be zero.

Table 4–2: DSP Control Registers

Name	I^2C Bus Address	High/ Low	Adjustable Range, Operational Modes	Reset Mode
Volume loudspeaker channel	0000_{hex}	H	[+12 dB ... –114 dB, MUTE]	MUTE
Volume / Mode loudspeaker channel		L	1/8 dB Steps, Reduce Volume / Tone Control	00_{hex}
Balance loudspeaker channel [L/R]	0001_{hex}	H	[0..100 / 100 % and vv][–127..0 / 0 dB and vv]	100%/100%
Balance Mode loudspeaker		L	[Linear mode / logarithmic mode]	linear mode
Bass loudspeaker channel	0002_{hex}	H	[+20 dB ... –12 dB]	0 dB
Treble loudspeaker channel	0003_{hex}	H	[+15 dB ... –12 dB]	0 dB
Loudness loudspeaker channel	0004_{hex}	H	[0 dB ... +17 dB]	0 dB
Loudness Filter Characteristic		L	[NORMAL, SUPER_BASS]	NORMAL
Spatial effect strength loudspeaker ch.	0005_{hex}	H	[–100%...OFF...+100%]	OFF
Spatial effect mode/customize		L	[SBE, SBE+PSE]	SBE+PSE
Volume headphone channel	0006_{hex}	H	[+12 dB ... –114 dB, MUTE]	MUTE
Volume / Mode headphone channel		L	1/8 dB Steps, Reduce Volume / Tone Control	00_{hex}
Volume SCART channel	0007_{hex}	H	$[00_{hex}$ ... $7F_{hex}]$,[+12 dB ... –114 dB, MUTE]	00_{hex}
Volume / Mode SCART channel		L	[Linear mode / logarithmic mode]	linear mode
Loudspeaker channel source	0008_{hex}	H	[SCART]	undefined
Loudspeaker channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA
Headphone channel source	0009_{hex}	H	[SCART]	undefined
Headphone channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA
SCART1 channel source	$000a_{hex}$	H	[SCART]	undefined
SCART1 channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA
Quasi-peak detector source	$000c_{hex}$	H	[SCART]	undefined
Quasi-peak detector matrix		L	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA
Prescale SCART	$000d_{hex}$	H	$[00_{hex}$ ... $7F_{hex}]$	00_{hex}
ACB Register (SCART Switches and DIG_OUT Pins)	0013_{hex}	H/L	Bits [15..0]	00_{hex}
Beeper	0014_{hex}	H/L	$[00_{hex}$ ... $7F_{hex}]/[00_{hex}$ ... $7F_{hex}]$	0/0
Mode Tone Control	0020_{hex}	H	[BASS/TREBLE, EQUALIZER]	BASS/TREB

Name	I²C Bus Address	High/ Low	Adjustable Range, Operational Modes	Reset Mode
Equalizer loudspeaker ch. band 1	0021_{hex}	H	[+12 dB ... –12 dB]	0 dB
Equalizer loudspeaker ch. band 2	0022_{hex}	H	[+12 dB ... –12 dB]	0 dB
Equalizer loudspeaker ch. band 3	0023_{hex}	H	[+12 dB ... –12 dB]	0 dB
Equalizer loudspeaker ch. band 4	0024_{hex}	H	[+12 dB ... –12 dB]	0 dB
Equalizer loudspeaker ch. band 5	0025_{hex}	H	[+12 dB ... –12 dB]	0 dB
Automatic Volume Correction	0029_{hex}	H	[off, on, decay time]	off
Volume Subwoofer channel	002Chex	H	[0dB ... –30 dB, mute]	0 dB
Subwoofer Channel Corner Frequency	002Dhex	H	[50 Hz ... 400 Hz]	
Subwoofer: Complementary Highpass		L	[off, on]	off
Balance headphone channel [L/R]	0030_{hex}	H	[0...100 / 100% and vv][–127...0 / 0 dB and vv]	100%/100%
Balance Mode headphone		L	[Linear mode / logarithmic mode]	linear mode
Bass headphone channel	0031_{hex}	H	[+20 dB ... –12 dB]	0 dB
Treble headphone channel	0032_{hex}	H	[+15 dB ... –12 dB]	0 dB
Loudness headphone channel	0033_{hex}	H	[0 dB ... +17 dB]	0 dB
Loudness filter characteristic		L	[NORMAL, SUPER_BASS]	NORMAL

4.2.1. Volume Loudspeaker Channel and Headphone Channel

Volume loudspeaker	**0000_{hex}**	**11 MSBs**
Volume headphone	**0006_{hex}**	**11 MSBs**
+12 dB	0111 1111 000x	$7F0_{hex}$
+11.875 dB	0111 1110 111x	$7EE_{hex}$
+0.125 dB	0111 0011 001x	732_{hex}
0 dB	0111 0011 000x	730_{hex}
–0.125 dB	0111 0010 111x	$72E_{hex}$
–113.875dB	0000 0001 001x	012_{hex}
–114 dB	0000 0001 000x	010_{hex}
Mute	0000 0000 xxxx RESET	$00x_{hex}$
Fast Mute	1111 1111 111x	FFE_{hex}

The highest given positive 11-bit number ($7F0_{hex}$) yields in a maximum possible gain of 12 dB. Decreasing the volume register by 1 LSB decreases the volume by 0.125 dB. Volume settings lower than the given minimum mute the output. With large scale input signals, positive volume settings may lead to signal clipping.

With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. Going back from Fast Mute should be done to the volume step before Fast Mute was activated.

Clipping Mode loudspeaker	**0000_{hex}**	**3 LSBs**
Clipping Mode headphone	**0006_{hex}**	**3 LSBs**
Reduce Volume	x000 RESET	0_{hex}
Reduce Tone Control	x001	1_{hex}
Compromise Mode	x010	2_{hex}

If the clipping mode is set to “Reduce Volume”, the following clipping procedure is used: To prevent severe clipping effects with bass, treble, or equalizer boosts, the internal volume is automatically limited to a level where, in combination with either bass, treble, or equalizer setting, the amplification does not exceed 12 dB.

If the clipping mode is “Reduce Tone Control”, the bass or treble value is reduced if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced, where amplification together with volume exceeds 12 dB.

If the clipping mode is “Compromise Mode”, the bass or treble value and volume are reduced half and half if amplification exceeds 12 dB (see example below). If the equalizer is switched on, the gain of those bands is reduced half and half, where amplification together with volume exceeds 12 dB.

Example:	**Vol.: +6 dB**	**Bass: +9 dB**	**Treble: +5 dB**
Red. Volume	3	9	5
Red. Tone Con.	6	6	5
Compromise	4.5	7.5	5

4.2.2. Balance Loudspeaker and Headphone Channel

Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected. In linear mode, a step by 1 LSB decreases or increases the balance by about 0.8% (exact figure: 100/127). In logarithmic mode, a step by 1 LSB decreases or increases the balance by 1 dB.

Balance Mode loudspeaker	**0001_{hex}**	**LSB**
Balance Mode headphone	**0030_{hex}**	**LSB**
linear	xxx0 RESET	0_{hex}
logarithmic	xxx1	1_{hex}

Linear Mode		
Balance loudspeaker channel [L/R]	**0001_{hex}**	**H**
Balance headphone channel [L/R]	**0030_{hex}**	**H**
Left muted, Right 100%	0111 1111	$7F_{hex}$
Left 0.8%, Right 100%	0111 1110	$7E_{hex}$
Left 99.2%, Right 100%	0000 0001	01_{hex}
Left 100%, Right 100%	0000 0000 RESET	00_{hex}
Left 100%, Right 99.2%	1111 1111	FF_{hex}
Left 100%, Right 0.8%	1000 0010	82_{hex}
Left 100%, Right muted	1000 0001	81_{hex}

Logarithmic Mode		
Balance loudspeaker channel [L/R]	**0001_{hex}**	**H**
Balance headphone channel [L/R]	**0030_{hex}**	**H**
Left –127 dB, Right 0 dB	0111 1111	$7F_{hex}$
Left –126 dB, Right 0 dB	0111 1110	$7E_{hex}$
Left –1 dB, Right 0 dB	0000 0001	01_{hex}
Left 0 dB, Right 0 dB	0000 0000 RESET	00_{hex}
Left 0 dB, Right –1 dB	1111 1111	FF_{hex}
Left 0 dB, Right –127 dB	1000 0001	81_{hex}
Left 0 dB, Right –128 dB	1000 0000	80_{hex}

4.2.3. Bass Loudspeaker and Headphone Channel

Bass loudspeaker	**0002_{hex}**	**H**
Bass headphone	**0031_{hex}**	**H**
+20 dB	0111 1111	$7F_{hex}$
+18 dB	0111 1000	78_{hex}
+16 dB	0111 0000	70_{hex}
+14 dB	0110 1000	68_{hex}
+12 dB	0110 0000	60_{hex}
+11 dB	0101 1000	58_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive bass settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain.

Loudspeaker channel: Bass and Equalizer cannot work simultaneously (see Table: Mode Tone Control). If Equalizer is used, Bass and Treble coefficients must be set to zero and vice versa.

4.2.4. Treble Loudspeaker and Headphone Channel

Treble loudspeaker	**0003_{hex}**	**H**
Treble headphone	**0032_{hex}**	**H**
+15 dB	0111 1000	78_{hex}
+14 dB	0111 0000	70_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive treble settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain.

Loudspeaker channel: Treble and Equalizer cannot work simultaneously (see Table: Mode Tone Control). If Equalizer is used, Bass and Treble coefficients must be set to zero and vice versa.

4.2.5. Loudness Loudspeaker and Headphone Channel

Loudness loudspeaker	**0004_{hex}**	**H**
Loudness headphone	**0033_{hex}**	**H**
+17 dB	0100 0100	44_{hex}
+16 dB	0100 0000	40_{hex}
+1 dB	0000 0100	04_{hex}
0 dB	0000 0000 RESET	00_{hex}

Mode Loudness loudspeaker	**0004_{hex}**	**L**
Mode Loudness headphone	**0033_{hex}**	**L**
Normal (constant volume at 1 kHz)	0000 0000 RESET	00_{hex}
Super Bass (constant volume at 2 kHz)	0000 0100	04_{hex}

Loudness increases the volume of low and high frequency signals, while keeping the amplitude of the 1 kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that ,in conjunction with volume, would result in an overall positive gain.

By means of ‘Mode Loudness’, the corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.

4.2.6. Spatial Effects Loudspeaker Channel

Spatial effect strength loudspeaker channel	**0005_{hex}**	**H**
Enlargement 100%	0111 1111	$7F_{hex}$
Enlargement 50%	0011 1111	$3F_{hex}$
Enlargement 1.5%	0000 0001	01_{hex}
Effect off	0000 0000 RESET	00_{hex}
Reduction 1.5%	1111 1111	FF_{hex}
Reduction 50%	1100 0000	$C0_{hex}$
Reduction 100%	1000 0000	80_{hex}
Spatial Effect Mode	**0005_{hex}**	**[7:4]**
Stereo Basewidth Enlargement (SBE) and Pseudo Stereo Effect (PSE). (Mode A)	0000 RESET 0000	0_{hex} 0_{hex}
Stereo Basewidth Enlargement (SBE) only. (Mode B)	0010	2_{hex}
Spatial Effect Customize Coefficient	**0005_{hex}**	**[3:0]**
max high pass gain	0000 RESET	0_{hex}
2/3 high pass gain	0010	2_{hex}
1/3 high pass gain	0100	4_{hex}
min high pass gain	0110	6_{hex}
automatic	1000	8_{hex}

There are several spatial effect modes available:

Mode A (low byte = 00_{hex}) is compatible to the formerly used spatial effect. Here, the kind of spatial effect depends on the source mode. If the incoming signal is in mono mode, Pseudo Stereo Effect is active; for stereo signals, Pseudo Stereo Effect and Stereo Basewidth Enlargement is effective. The strength of the effect is controllable by the upper byte. A negative value reduces the stereo image. A rather strong spatial effect is recommended for small TV sets where loudspeaker spacing is rather close. For large screen TV sets, a more moderate spatial effect is recommended. In mode A, even in case of stereo input signals, Pseudo Stereo Effect is active, which reduces the center image.

In Mode B, only Stereo Basewidth Enlargement is effective. For mono input signals, the Pseudo Stereo Effect has to be switched on.

It is worth mentioning, that all spatial effects affect amplitude and phase response. With the lower 4 bits, the frequency response can be customized. A value of 0000_{bin} yields a flat response for center signals (L = R) but a high pass function of L or R only signals. A value of 0110_{bin} has a flat response for L or R only signals but a lowpass function for center signals. By using 1000_{bin}, the frequency response is automatically adapted to the sound material by choosing an optimal high pass gain.

4.2.7. Volume SCART

Volume Mode SCART	**0007_{hex}**	**LSB**
linear	xxx0 RESET	0_{hex}
logarithmic	xxx1	1_{hex}

Linear Mode		
Volume SCART	**0007_{hex}**	**H**
OFF	0000 0000 RESET	00_{hex}
0 dB gain (digital full scale (FS) to 2 V_{RMS} output)	0100 0000	40_{hex}
+6 dB gain (–6 dBFS to 2 V_{RMS} output)	0111 1111	$7F_{hex}$

Logarithmic Mode		
Volume SCART	**0007_{hex}**	**11 MSBs**
+12 dB	0111 1111 000x	$7F0_{hex}$
+11.875 dB	0111 1110 111x	$7EE_{hex}$
+0.125 dB	0111 0011 001x	732_{hex}
0 dB	0111 0011 000x	730_{hex}
–0.125 dB	0111 0010 111x	$72E_{hex}$
–113.875 dB	0000 0001 001x	012_{hex}
–114 dB	0000 0001 000x	010_{hex}
Mute	0000 0000 0000 RESET	000_{hex}

4.2.8. Channel Source Modes

Loudspeaker channel source	**0008_{hex}**	**H**
Headphone channel source	**0009_{hex}**	**H**
SCART channel source	**$000a_{hex}$**	**H**
Quasi-peak detector source	**$000c_{hex}$**	**H**
NONE (MSP 3410: FM)	0000 0000 RESET	00_{hex}
NONE (MSP3410: NICAM)	0000 0001	01_{hex}
SCART	0000 0010	02_{hex}

Note: For Headphone output it is also possible to select a subwoofer signal derived from the Loudspeaker channel. For more details see section 4.2.16.

4.2.9. Channel Matrix Modes

Loudspeaker channel matrix	**0008_{hex}**	**L**
Headphone channel matrix	**0009_{hex}**	**L**
SCART channel matrix	**$000a_{hex}$**	**L**
Quasi-peak detector-matrix	**$000c_{hex}$**	**L**
SOUNDA / LEFT	0000 0000 RESET	00_{hex}
SOUNDB / RIGHT	0001 0000	10_{hex}
STEREO	0010 0000	20_{hex}
MONO	0011 0000	30_{hex}
SUM/DIFF	0100 0000	40_{hex}
AB_XCHANGE	0101 0000	50_{hex}
INVERT_B	0110 0000	60_{hex}

The sum/difference mode can be used together with the quasi-peak detector to determine the sound material mode. If the difference signal on channel B (right) is near to zero, and the sum signal on channel A (left) is high, the incoming audio signal is mono. If there is a significant level on the difference signal, the incoming audio is stereo.

4.2.10. SCART Prescale

Volume Prescale SCART	**$000d_{hex}$**	**H**
OFF	0000 0000 RESET	00_{hex}
0 dB gain (2 V_{RMS} input to digital full scale)	0001 1001	19_{hex}
+14 dB gain (400 mV_{RMS} input to digital full scale)	0111 1111	$7F_{hex}$

4.2.11. ACB Register, Definition of the SCART-Switches and DIG_CTR_OUT Pins

ACB Register	**0013_{hex}**	**H**
DSP In Selection of Source: SC_1_IN MONO_IN SC_2_IN SC_3_IN	 xxxx xx00 xxxx xx01 xxxx xx10 xxxx xx11	 RESET
SC_1_OUT_L/R Selection of Source: SC_3_IN SC_2_IN MONO_IN DA_SCART	 xxxx 00xx xxxx 01xx xxxx 10xx xxxx 11xx	 RESET
SC_2_OUT_L/R Selection of Source: DA_SCART SC_1_IN MONO_IN	 xx00 xxxx xx01 xxxx xx10 xxxx	 RESET
DIG_CTR_OUT1 low high	 x0xx xxxx x1xx xxxx	 RESET
DIG_CTR_OUT2 low high	 0xxx xxxx 1xxx xxxx	 RESET
RESET: The RESET state is taken at the time of the first write transmission on the control bus to the audio processing part (DSP). By writing to the ACB register first, the RESET state can be redefined.		

4.2.12. Beeper

Beeper Volume	**0014_{hex}**	**H**
OFF	0000 0000 RESET	00_{hex}
Maximum Volume (full digital scale FDS)	0111 1111	$7F_{hex}$
Beeper Frequency	**0014_{hex}**	**L**
16 Hz (lowest)	0000 0001	01_{hex}
1 kHz	0100 0000	40_{hex}
4 kHz (highest)	1111 1111	FF_{hex}

A squarewave beeper can be added to the loudspeaker channel and the headphone channel. The addition point is just before loudness and volume adjustment.

4.2.13. Mode Tone Control

Mode Tone Control	**00020_{hex}**	**H**
Bass and Treble	0000 0000 RESET	00_{hex}
Equalizer	1111 1111	FF_{hex}

By means of ‘Mode Tone Control’, Bass/Treble or Equalizer may be activated.

4.2.14. Equalizer Loudspeaker Channel

Band 1 (below 120 Hz)	**0021_{hex}**	**H**
Band 2 (Center: 500 Hz)	**0022_{hex}**	**H**
Band 3 (Center: 1.5 kHz)	**0023_{hex}**	**H**
Band 4 (Center: 5 kHz)	**0024_{hex}**	**H**
Band 5 (above 10kHz)	**0025_{hex}**	**H**
+12 dB	0110 0000	60_{hex}
+11 dB	0101 1000	58_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive equalizer settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set equalizer bands to a value that, in conjunction with volume, would result in an overall positive gain.

Equalizer must not be used simultaneously with Bass and Treble (Mode Tone Control must be set to FF to use the Equalizer).

4.2.15. Automatic Volume Correction (AVC)

AVC	**on/off**	**0029hex**	**[15:12]**
AVC	off and Reset of int. variables	0000 RESET	0hex
AVC	on	1000	8hex
AVC	**Decay Time**	**0029hex**	**[11:8]**
8 sec	(long)	1000	8hex
4 sec	(middle)	0100	4hex
2 sec	(short)	0010	2hex
20 ms	(very short)	0001	1hex

Different sound sources (e.g. Terrestrial channels, SAT channels or SCART) fairly often don't have the same volume level. Advertisement during movies as well has mostly a different (higher) volume level, than the movie itself. The Automatic Volume Correction (AVC) solves this problem and equalizes the volume levels.

The absolute value of the incoming signal is fed into a filter with 16ms attack time and selectable decay time. The decay time must be adjusted as shown in the table above. This attack/decay filter block works similar to a peak hold function. The volume correction value with it's quasi continuous step width is calculated using the attack/decay filter output.

The Automatic Volume Correction works with an internal reference level of –18 dBFS. This means, input signals with a volume level of –18 dBFS will not be affected by the AVC. If the input signals vary in a range of –24 dB to 0 dB the AVC compensates this.

Example: A static input signal of 1 kHz on Scart has an output level as shown in the table below.

Scart Input 0dbr = 2 Vrms	**Volume Correction**	**Main Output 0dBr = 1.4 Vrms**
0 dBr	–18 dB	–18 dBr
–6 dBr	–12 dB	–18 dBr
–12 dBr	–6 dB	–18 dBr
–18 dBr	–0 dB	–18 dBr
–24 dBr	+ 6 dB	–18 dBr
–30 dBr	+ 6 dB	–24 dBr
Loudspeaker Volume = 73h = 0 dBFS Scart Prescale = 20h i.e. 2.0 Vrms = 0dBFS		

To reset the internal variables, the AVC should be switched off and on during any channel or source change. For standard applications, the recommended decay time is 4sec.

Note: AVC should not be used in any Dolby Prologic modes, except PANORAMA, where no other than the loudspeaker output is active.

4.2.16. Subwoofer on Headphone Output

The subwoofer channel is created by combining the left and right loudspeaker channels ((L+R)/2) directly behind the tone control filter block. A third order lowpass filter with programmable corner frequency and volume adjustment respectively to the loudspeaker channel output is performed to the bass-signal. Additionally, at the loudspeaker channels, a complementary high pass filter can be switched on. The subwoofer channel output can be switched to the headphone D/A converter alternatively with the headphone output.

Subwoofer Channel Volume Adjust	**002Chex**	**H**
0 dB	0000 0000 RESET	00hex
–1 dB	1111 1111	FFhex
–29 dB	1110 0011	E3hex
–30 dB	1110 0010	E2hex
Mute	1000 0000	80hex

Subwoofer Channel Corner Frequency	**002Dhex**	**H**
50 Hz .... 400 Hz e.g. 50 Hz = 5 int 400 Hz = 40int	 0000 0101 0010 1000	 05hex 28hex
Headphone Output	**002Dhex**	**[7:4]**
Headphone	0000	0hex
Subwoofer	1000	8hex
Subwoofer: Complementary Highpass	**002Dhex**	**[3:0]**
HP off	0000	0hex
HP on	0001	1hex

Note: If subwoofer is chosen for headphone output, the corner frequency must be set to the desired value, before the loudspeaker volume is set. This is to avoid plop noise.

4.3. Summary of Readable Registers

All readable registers are 16 bit wide. Transmissions via I^2C bus have to take place in 16 bit words. Single data entries are 8 bit. Some of the defined 16 bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writeable.

4.3.1. Quasi Peak Detector

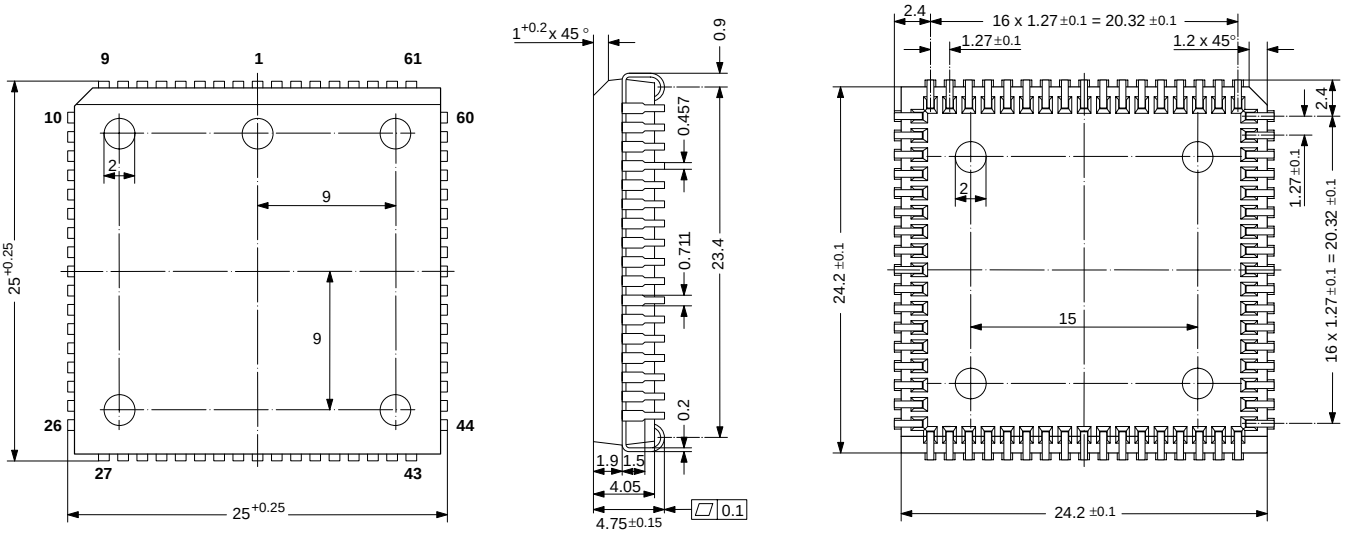
Quasi peak readout left	**0019_{hex}**	**H+L**
Quasi peak readout right	**$001a_{hex}$**	**H+L**
Quasi peak readout	$[0_{hex}$ ... $7FFF_{hex}]$ values are 16 bit binary	

The quasi peak readout register can be used to read out the quasi peak level of any input source, in order to adjust all inputs to the same normalized listening level. The refresh rate is 32 kHz. The feature is based on a filter time constant:

attack-time: 1.3 ms
decay-time: 37 ms

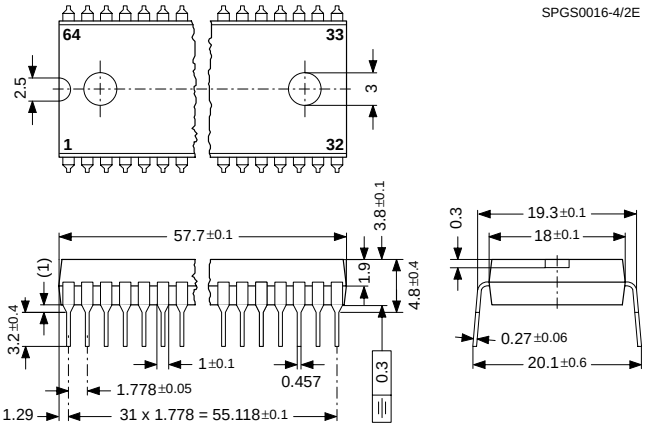
5. Specifications

5.1. Outline Dimensions



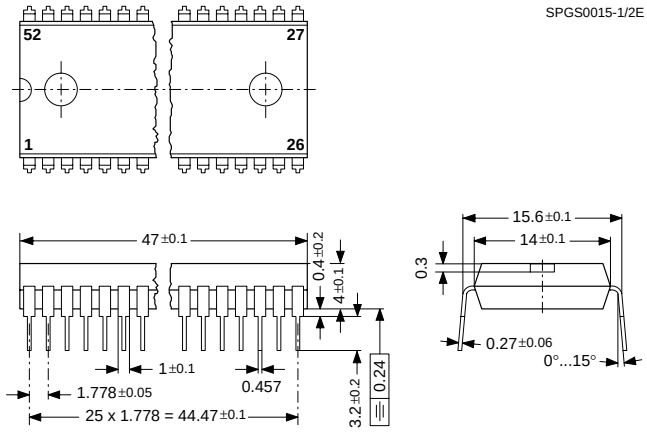
SPGS7004-3/4E

Fig. 5–1:
68-Pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approximately 4.8 g
Dimensions in mm



SPGS0016-4/2E

Fig. 5–2:
64-Pin Plastic Shrink Dual Inline Package
(PSDIP64)
Weight approximately 9.0 g
Dimensions in mm



SPGS0015-1/2E

Fig. 5–3:
52-Pin Plastic Shrink Dual In Line Package
(PSDIP52)
Weight approximately 5.5 g
Dimensions in mm

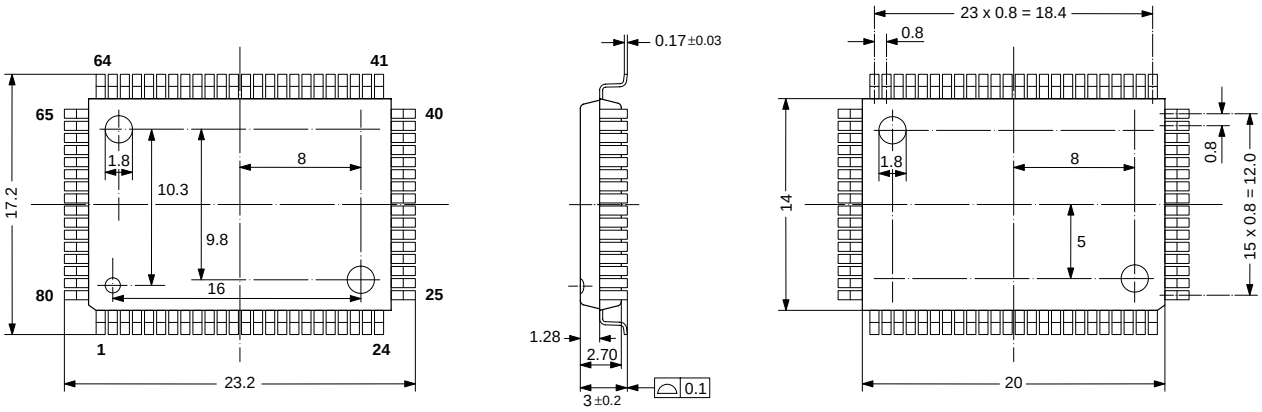


Fig. 5–4:
80-Pin Plastic Quad Flat Pack Package
(PQFP80)
Weight approximately 1.61 g
Dimensions in mm

5.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram

AHVSS = connect to AHVSS
DVSS = if not used, connect to DVSS
– = pin does not exist in this package

Pin No.				Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin				
1	16	14	9	TP	OUT	LV	Test pin
2	–	–	–	NC		LV	Not connected
3	15	13	8	NC		LV	Not connected
4	14	12	7	NC		LV	Not connected
5	13	11	6	TP	OUT	LV	Test pin
6	12	10	5	TP	IN/OUT	LV	Test pin
7	11	9	4	TP	IN/OUT	LV	Test pin
8	10	8	3	I^2C_DA	IN/OUT	X	I^2C data
9	9	7	2	I^2C_CL	IN/OUT	X	I^2C clock
10	8	–	1	NC		LV	Not connected
11	7	6	80	STANDBYQ	IN	X	Standby (low-active)
12	6	5	79	ADR_SEL	IN	X	I^2C Bus address select
13	5	4	78	D_CTR_OUT0	OUT	LV	Digital control output 0
14	4	3	77	D_CTR_OUT1	OUT	LV	Digital control output 1

[1] Due to compatibility with MSP 3410, it is possible to connect with DVSS as well.

Pin No.				Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin				
15	3	–	76	NC		LV	Not connected
16	2	–	–	NC		LV	Not connected
17	–	–	75	NC		LV	Not connected
18	1	2	74	AUD_CL_OUT	OUT	LV	Audio clock output
19	64	1	73	NC		LV	Not connected
20	63	52	72	XTAL_OUT	OUT	X	Crystal oscillator
21	62	51	71	XTAL_IN	IN	X	Crystal oscillator
22	61	50	70	TESTEN	IN	X	Test pin
23	60	49	69	NC		LV	Not connected
24	59	48	68	NC		LV	Not connected
25	58	47	67	NC		LV	Not connected
26	57	46	66	AVSUP		X	Analog power supply +5 V
–	–	–	65	AVSUP		X	Analog power supply +5 V
–	–	–	64	NC		LV	Not connected
–	–	–	63	NC		LV	Not connected
27	56	45	62	AVSS		X	Analog ground
–	–	–	61	AVSS		X	Analog ground
28	55	44	60	MONO_IN	IN	LV	Mono input
–	–	–	59	NC		LV	Not connected
29	54	43	58	VREFTOP		X	Reference voltage
30	53	42	57	SC1_IN_R	IN	LV	Scart input 1 in, right
31	52	41	56	SC1_IN_L	IN	LV	Scart input 1 in, left
32	51	–	55	ASG1		AHVSS	Analog Shield Ground 1
33	50	40	54	SC2_IN_R	IN	LV	Scart input 2 in, right
34	49	39	53	SC2_IN_L	IN	LV	Scart input 2 in, left
35	48	–	52	ASG2		AHVSS	Analog Shield Ground 2
36	47	38	51	SC3_IN_R	IN	LV	Scart input 3 in, right
37	46	37	50	SC3_IN_L	IN	LV	Scart input 3 in, left
38	45	–	49	NC		LV	Not connected
39	44	–	48	NC		LV	Not connected

[1] Due to compatibility with MSP 3410, it is possible to connect with DVSS as well.

Pin No.				Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin				
40	43	–	47	NC		LV	Not connected
41	–	–	46	NC		LV or AHVSS	Not connected
42	42	36	45	AGNDC		X	Analog reference voltage high voltage part
43	41	35	44	AHVSS		X	Analog ground
–	–	–	43	AHVSS		X	Analog ground
–	–	–	42	NC		LV	Not connected
–	–	–	41	NC		LV	Not connected
44	40	34	40	CAPL_M		X	Volume capacitor MAIN
45	39	33	39	AHVSUP		X	Analog power supply 8.0 V
46	38	32	38	CAPL_A		X	Volume capacitor AUX
47	37	31	37	SC1_OUT_L	OUT	LV	Scart output 1, left
48	36	30	36	SC1_OUT_R	OUT	LV	Scart output 1, right
49	35	29	35	VREF1		X	Reference ground 1 high voltage part
50	34	28	34	SC2_OUT_L	OUT	LV	Scart output 2, left
51	33	27	33	SC2_OUT_R	OUT	LV	Scart output 2, right
52	–	–	32	ASG3		AHVSS[1)]	Analog Shield Ground 3
53	32	–	31	NC		LV	Not connected
54	31	26	30	NC		LV	Not connected
55	30	–	29	NC		LV	Not connected
56	29	25	28	DACM_L	OUT	LV	Analog output MAIN, left
57	28	24	27	DACM_R	OUT	LV	Analog output MAIN, right
58	27	23	26	VREF2		X	Reference ground 2 high voltage part
59	26	22	25	DACA_L	OUT	LV	Analog output AUX, left
60	25	21	24	DACA_R	OUT	LV	Analog output AUX, right
–	–	–	23	NC		LV	Not connected
–	–	–	22	NC		LV	Not connected
61	24	20	21	RESETQ	IN	X	Power-on-reset

1) Due to compatibility with MSP 3410, it is possible to connect with DVSS as well.

Pin No.				Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin				
62	23	–	20	NC		LV	Not connected
63	22	–	19	NC		LV	Not connected
64	21	19	18	NC		LV	Not connected
65	20	18	17	NC		LV	Not connected
66	19	17	16	DVSS		X	Digital ground
–	–	–	15	DVSS		X	Digital ground
–	–	–	14	DVSS		X	Digital ground
67	18	16	13	DVSUP		X	Digital power supply +5 V
–	–	–	12	DVSUP		X	Digital power supply +5 V
–	–	–	11	DVSUP		X	Digital power supply +5 V
68	17	15	10	TP	OUT	LV	Test pin

[1] Due to compatibility with MSP 3410, it is possible to connect with DVSS as well.

5.3. Pin Configurations

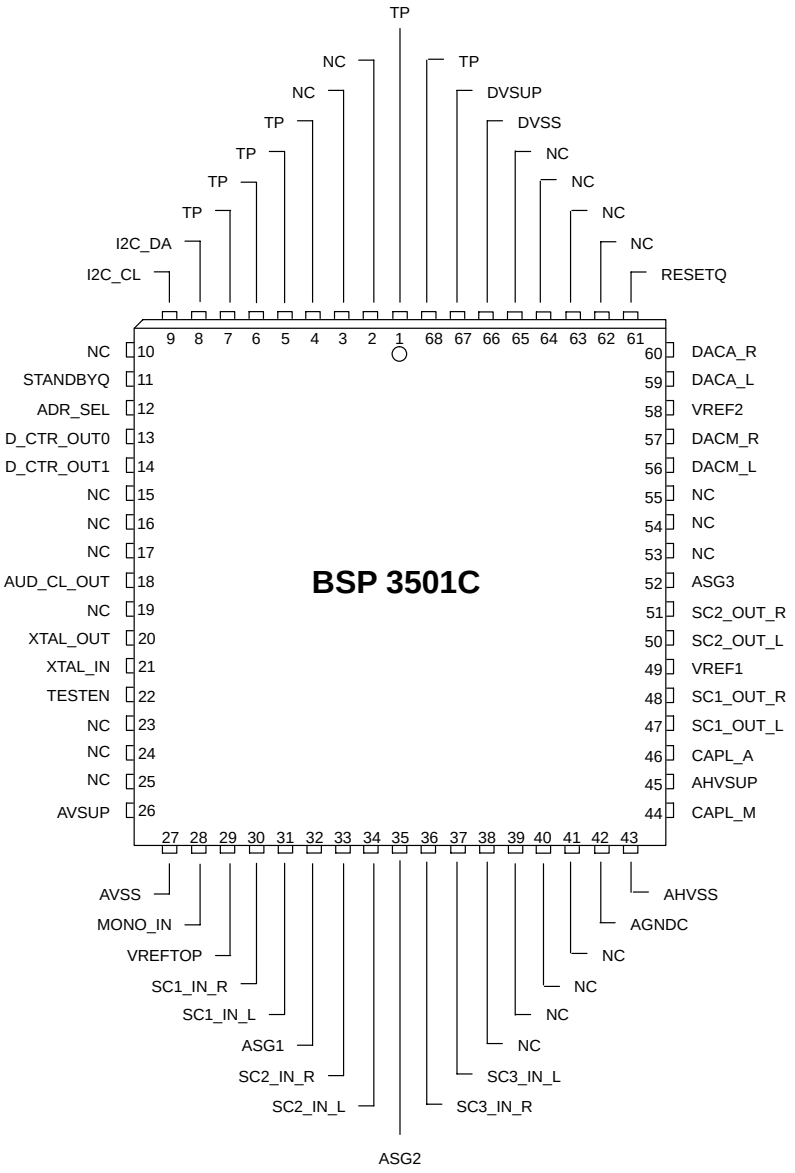


Fig. 5–5: 68-pin PLCC package

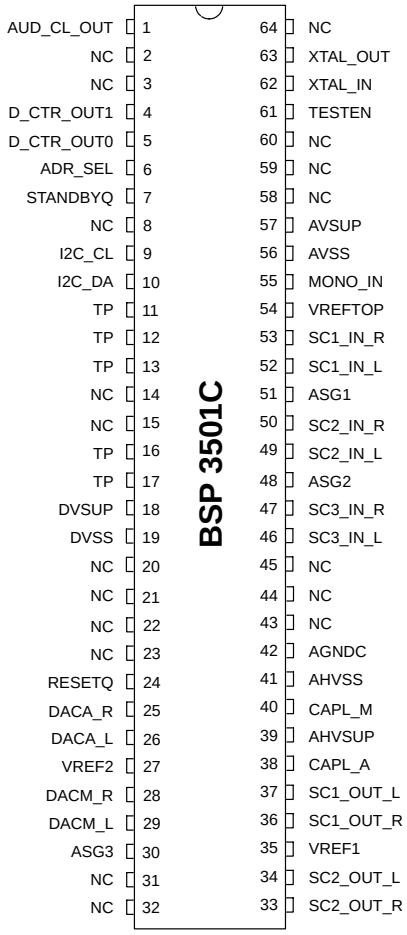


Fig. 5–6: 64-pin shrink PSDIP package

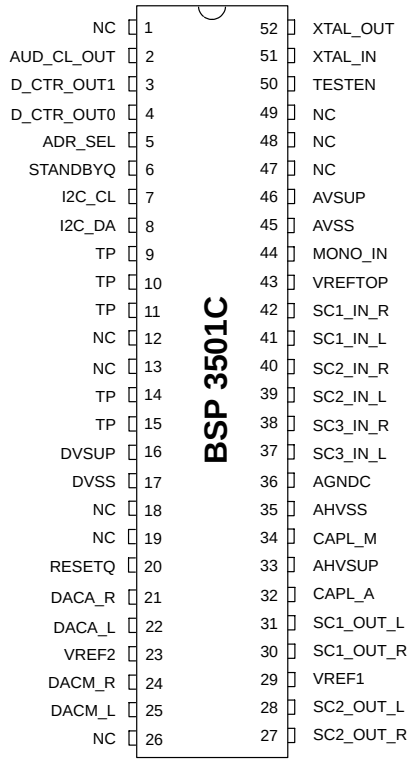


Fig. 5–7: 52-pin shrink PSDIP package

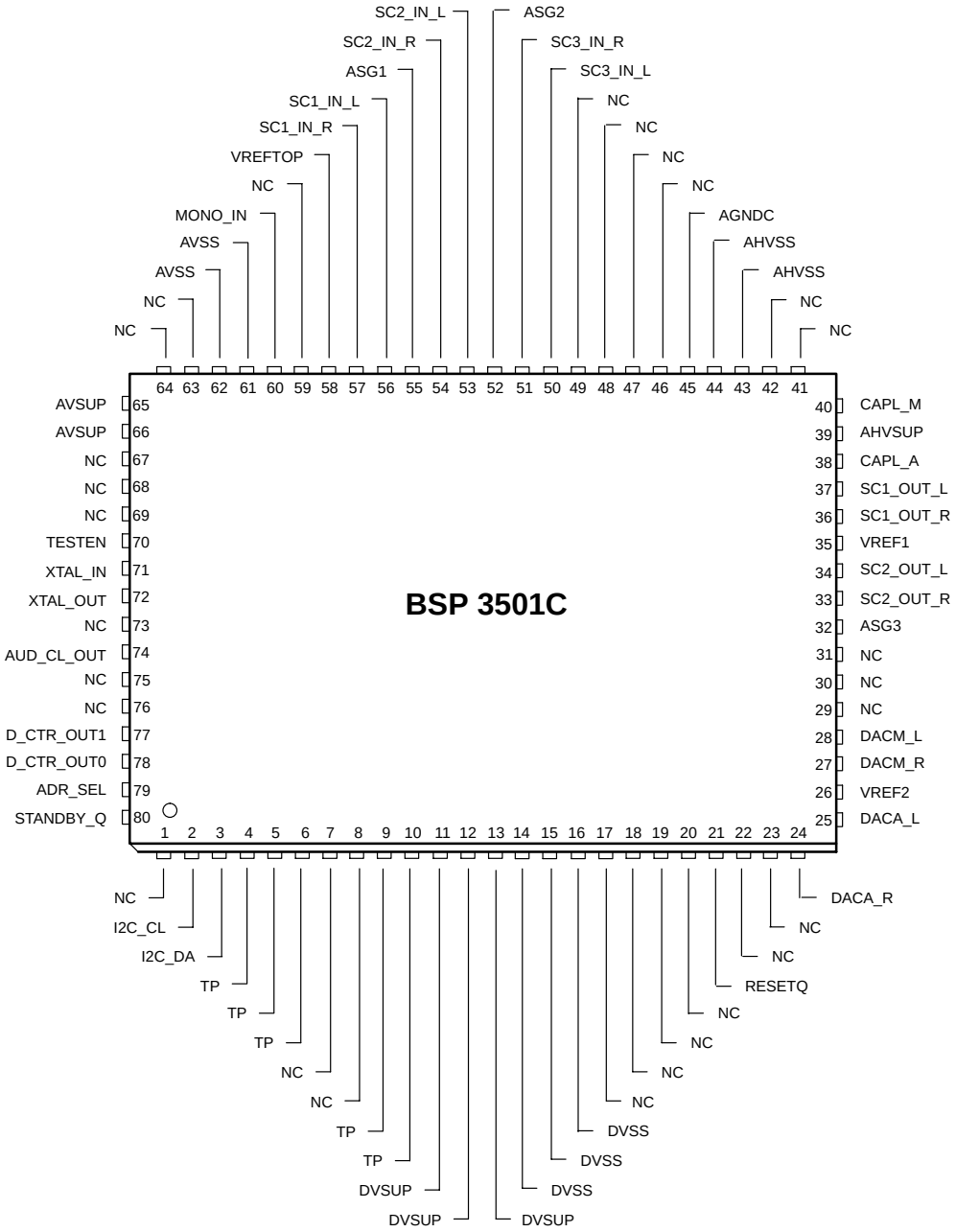


Fig. 5–8: 80-pin PQFP package

5.4. Pin Circuits

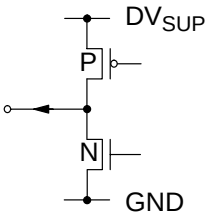


Fig. 5–9: Output Pins 13, 14 (D_CTR_OUT0/1)

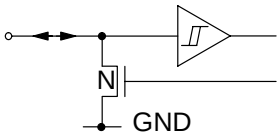


Fig. 5–10: Input/Output Pins 8 and 9 (I^2C_DA, I^2C_CL)

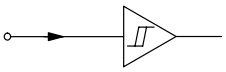


Fig. 5–11: Input Pins 11, 12, 61, and 62 (STANDBYQ, ADR_SEL, RESETQ, TESTEN)

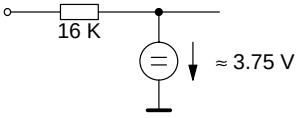


Fig. 5–12: Input Pin 28 (MONO_IN)

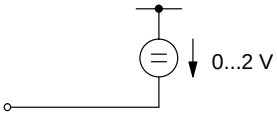


Fig. 5–13: Capacitor Pins 44 and 46 (CAPL_M, CAPL_A)

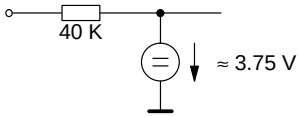


Fig. 5–14: Input Pins 30, 31, 33, 34, 36, and 37 (SC1–3_IN_L/R)

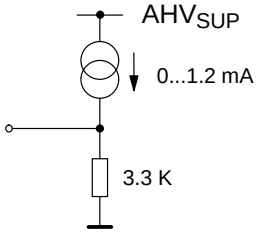


Fig. 5–15: Output Pins 56, 57, 59, and 60 (DACA_L/R, DACM_L/R)

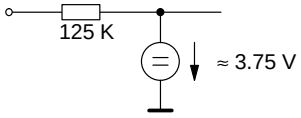


Fig. 5–16: Pin 42 (AGNDC)

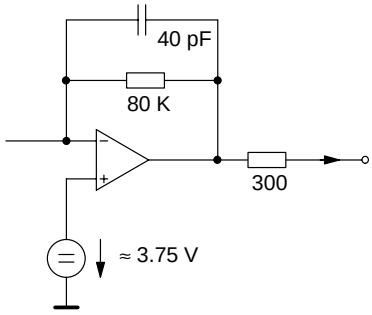


Fig. 5–17: Output Pins 47, 48, 50 and 51 (SC_1/2_OUT_L/R)

5.5. Electrical Characteristics

5.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	70	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP1}	First Supply Voltage	AHVSUP	–0.3	9.0	V
V_{SUP2}	Second Supply Voltage	DVSUP	–0.3	6.0	V
V_{SUP3}	Third Supply Voltage	AVSUP	–0.3	6.0	V
dV_{SUP23}	Voltage between AVSUP and DVSUP	AVSUP, DVSUP	–0.5	0.5	V
P_{TOT}	Chip Power Dissipation PLCC68 without Heat Spreader	AHVSUP, DVSUP, AVSUP		1100	mW
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA[1]
V_{Iana}	Input Voltage, all Analog Inputs	SCn_IN_s,[2] MONO_IN	–0.3	V_{SUP1}+0.3	V
I_{Iana}	Input Current, all Analog Inputs	SCn_IN_s,[2] MONO_IN	–5	+5	mA[1]
I_{Oana}	Output Current, all SCART Outputs	SCn_OUT_s[2]	[3], [4]	[3], [4]	
I_{Oana}	Output Current, all Analog Outputs except SCART Outputs	DACp_s[2]	[3]	[3]	
I_{Cana}	Output Current, other pins connected to capacitors	CAPL_p,[2] AGNDC	[3]	[3]	

1) positive value means current flowing into the circuit
2) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”
3) The Analog Outputs are short circuit proof with respect to First Supply Voltage and Ground.
4) Total chip power dissipation must not exceed absolute maximum rating.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

5.5.2. Recommended Operating Conditions

(at T_A = 0 to 70 °C)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP1}	First Supply Voltage	AHVSUP	7.6	8.0	8.4	V
V_{SUP2}	Second Supply Voltage	DVSUP	4.75	5.0	5.25	V
V_{SUP3}	Third Supply Voltage	AVSUP	4.75	5.0	5.25	V
V_{REIL}	RESET Input Low Voltage	RESETQ			0.45	V_{SUP2}
V_{REIH}	RESET Input High Voltage		0.8			V_{SUP2}
t_{REIL}	RESET Low Time after DVSUP Stable and Oscillator Startup		5			µs
V_{DIGIL}	Digital Input Low Voltage	STANDBYQ, ADR_SEL, TESTEN			0.25	V_{SUP2}
V_{DIGIH}	Digital Input High Voltage		0.75			V_{SUP2}
t_{STBYQ1}	STANDBYQ Setup Time before Turn-off of Second Supply Voltage	STANDBYQ, DVSUP	1			µs
I^2C-Bus Recommendations						
V_{IMIL}	I^2C-BUS Input Low Voltage	I^2C_CL, I^2C_DA			0.3	V_{SUP2}
V_{IMIH}	I^2C-BUS Input High Voltage		0.6			V_{SUP2}
f_{IM}	I^2C-BUS Frequency	I^2C_CL			1.0	MHz
t_{I2C1}	I^2C START Condition Setup Time	I^2C_CL, I^2C_DA	120			ns
t_{I2C2}	I^2C STOP Condition Setup Time		120			ns
t_{I2C3}	I^2C-Clock Low Pulse Time	I^2C_CL	500			ns
t_{I2C4}	I^2C-Clock High Pulse Time		500			ns
t_{I2C5}	I^2C-Data Setup Time Before Rising Edge of Clock	I^2C_CL, I^2C_DA	55			ns
t_{I2C6}	I^2C-Data Hold Time after Falling Edge of Clock		55			ns

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Crystal Recommendations						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–100		+100	ppm
D_{TEM}	Frequency Variation versus Temperature		–50		+50	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
Load Capacitance Recommendations						
C_L	External Load Capacitance[2)]	XTAL_IN, XTAL_OUT	PSDIP 1.5 PLCC 3.3			pF pF
Amplitude Recommendation for Operation with External Clock Input (C_{load} after reset = 22 pF)						
V_{XCA}	External Clock Amplitude	XTAL_IN	0.7			V_{pp}
Analog Input and Output Recommendations						
C_{AGNDC}	AGNDC-Filter-Capacitor	AGNDC	–20%	3.3		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
C_{inSC}	DC-Decoupling Capacitor in front of SCART Inputs	SCn_IN_s[1)]	–20%	330	+20%	nF
V_{inSC}	SCART Input Level				2.0	V_{RMS}
V_{inMONO}	Input Level, Mono Input	MONO_IN			2.0	V_{RMS}
R_{LSC}	SCART Load Resistance	SCn_OUT_s[1)]	10			kΩ
C_{LSC}	SCART Load Capacitance				6.0	nF
C_{VMA}	Main/AUX Volume Capacitor	CAPL_M, CAPL_A		10		µF
C_{FMA}	Main/AUX Filter Capacitor	DACM_s, DACA_s[1)]	–10%	1	+10%	nF

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”

2) External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal oscillator. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match 18.432 MHz as closely as possible. Due to different layouts of customer PCBs, the matching capacitor size should be defined in the application. The suggested values (1.5 pF/3.3 pF) are figures based on experience with various PCB layouts.

5.5.3. Characteristics at T_A = 0 to 70 °C, f_{CLOCK} = 18.432 MHz

(Typical values are measured at T_A = 25 °C, AHVSUP = 8 V, DVSUP = 5 V, AVSUP = 5 V.)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
DCO							
f_{CLOCK}	Clock Input Frequency	XTAL_IN		18.432		MHz	
D_{CLOCK}	Clock High to Low Ratio		45		55	%	
t_{JITTER}	Clock Jitter (verification not provided in production test)				50	ps	
V_{xtalDC}	DC-Voltage Oscillator			2.5		V	
$t_{Startup}$	Oscillator Startup Time at VDD Slew-rate of 1 V / 1 µs	XTAL_IN, XTAL_OUT		0.4	2.0	ms	
Power Supply							
I_{SUP1A}	First Supply Current (active) Analog Volume for Main and Aux at 0dB Analog Volume for Main and Aux at –30dB at T_j = 27 °C	AHVSUP	 8.2 5.6	 14.8 10.0	 22.0 15.0	 mA mA	f = 18.432 MHz AHVSUP = 8 V DVSUP = 5 V AVSUP = 5 V
I_{SUP2A}	Second Supply Current (active)	DVSUP	60	65	70	mA	f = 18.432 MHz DVSUP = 5 V
I_{SUP3A}	Third Supply Current (active)	AVSUP		25		mA	f = 18.432 MHz AVSUP = 5 V
I_{SUP1S}	First Supply Current (standby mode) at T_j = 27 °C	AHVSUP	2.8	5.0	7.2	mA	STANDBYQ = low VSUP = 8 V
Audio Clock Output							
V_{APUAC}	Audio Clock Output AC Voltage	AUD_CL_OUT	1.2			V_{pp}	40 pF load
V_{APUDC}	Audio Clock Output DC Voltage		0.4		0.6	V_{SUP1}	
Digital Output							
V_{DCTROL}	Digital Output Low Voltage	D_CTR_OUT0 D_CTR_OUT1			0.4	V	I_{DDCTR} = 1 mA
V_{DCTROH}	Digital Output High Voltage		4.0			V	I_{DDCTR} = –1 mA
I^2C Bus							
V_{IMOL}	I^2C-Data Output Low Voltage	I^2C_DA	0.4			V	I_{iMOL} = 3 mA
I_{IMOH}	I^2C-Data Output High Current				1	µA	V_{IMOH} = 5 V
t_{IMOL1}	I^2C-Data Output Hold Time after Falling Edge of Clock	I^2C_DA, I^2C_CL	15			ns	
t_{IMOL2}	I^2C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{IM} = 1 MHz DVSUP = 5 V
Analog Ground							
V_{AGNDC0}	AGNDC Open Circuit Voltage	AGNDC	3.64	3.73	3.84	V	$R_{load} \geq 10$ MΩ
R_{outAGN}	AGNDC Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C		 70 70	 125	 180 180	 kΩ kΩ	3 V ≤ V_{AGNDC} ≤ 4 V

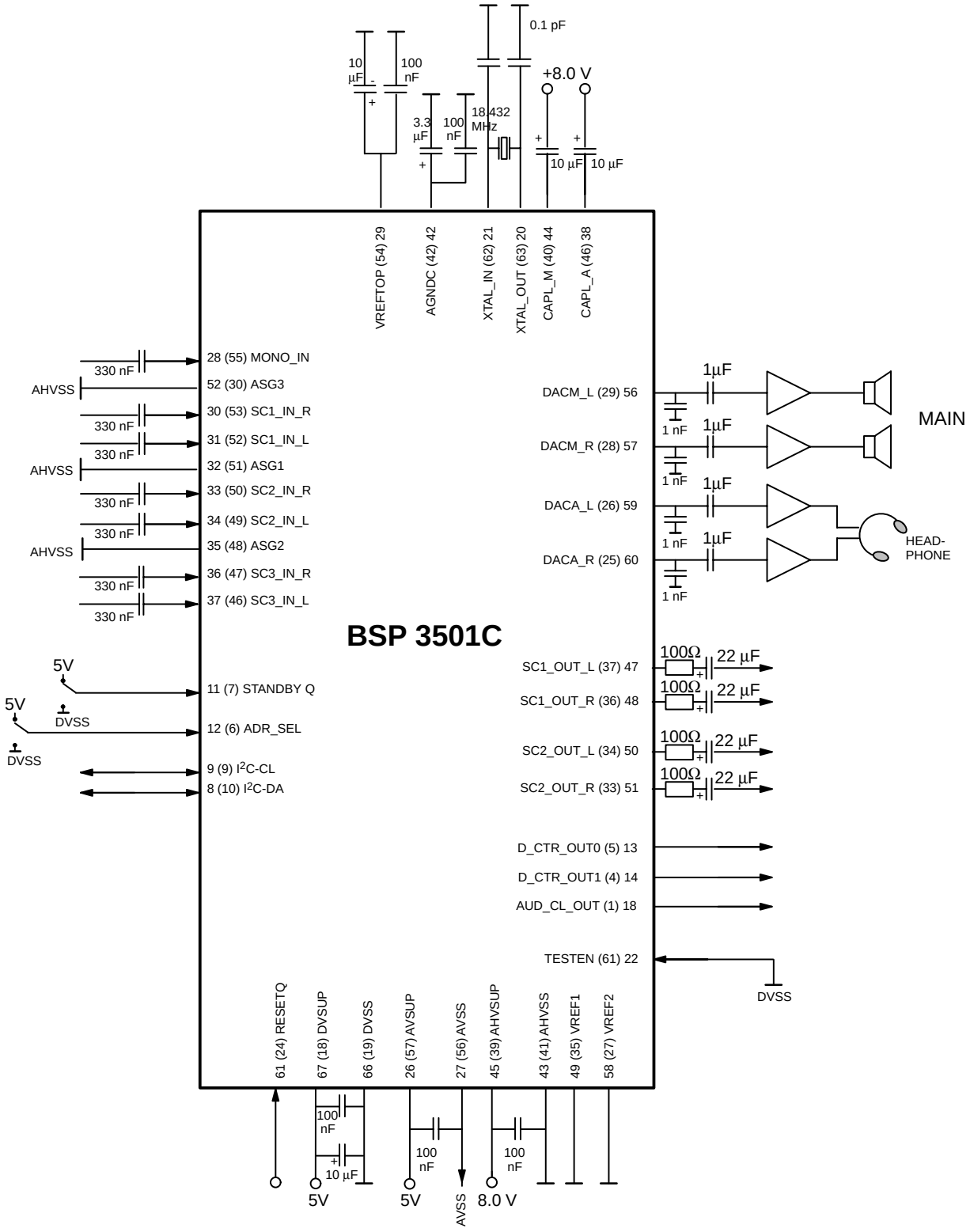
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Input Resistance							
R_{inSC}	SCART Input Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SCn_IN_s[1)]	 25 25	40	 58 58	 kΩ kΩ	f_{signal} = 1 kHz, I ≤ 0.05 mA
R_{inMONO}	MONO Input Resistance at T_j = 27 °C from T_A = 0 to 70 °C	MONO_IN	 10 10	16	 23 23	 kΩ kΩ	f_{signal} = 1 kHz, I ≤ 0.1 mA
Audio Analog-to-Digital-Converter							
V_{AICL}	Analog Input Clipping Level for Analog-to-Digital-Conversion	SCn_IN_s,[1)] MONO_IN	2.02	2.12	2.22	V_{RMS}	f_{signal} = 1 kHz
SCART Outputs							
R_{outSC}	SCART Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SCn_OUT_s[1)]	 0.20 0.20	0.33	 0.46 0.5	 kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
dV_{OUTSC}	Deviation of DC-Level at SCART Output from AGNDC Voltage		–70		+70	mV	
A_{SCtoSC}	Gain from Analog Input to SCART Output	SCn_IN_s[1)] MONO_IN → SCn_OUT_s[1)]	–1.0	0	+0.5	dB	f_{signal} = 1kHz
$f_{rSCtoSC}$	Frequency Response from Analog Input to SCART Output bandwidth: 0 to 20000 Hz		–0.5	0	+0.5	dB	with respect to 1 kHz
V_{outSC}	Signal Level at SCART-Output during full-scale digital input signal from DSP	SCn_OUT_s[1)]	1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz
Main and AUX Outputs							
R_{outMA}	Main/AUX Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	DACp_s[1)]	 2.1 2.1	3.3	 4.6 5.0	 kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
$V_{outDCMA}$	DC-Level at Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at –30 dB		 1.74 –	 1.94 61	 2.14 –	 V mV	
V_{outMA}	Signal Level at Main/AUX-Output during full-scale digital input signal from DSP for Analog Volume at 0 dB		1.23	1.37	1.51	V_{RMS}	f_{signal} = 1 kHz

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Performance							
SNR	Signal-to-Noise Ratio						
	from Analog Input to Main/AUX/ SCART Output via DSP	MONO_IN, SCn_IN_s[1)]	80	85		dB	Input Level = –20 dB with resp. to V_{AICL}, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz
	from Analog Input to SCART Output (analog)	MONO_IN, SCn_IN_s[1)] → SCn_OUT_s[1)]	93	96		dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz
THD	Total Harmonic Distortion						
	from Analog Input to Main/AUX/ SCART Output via DSP	MONO_IN, SCn_IN_s[1)]			0.10	%	Input Level = –3 dBr with resp. to V_{AICL}, f_{sig} =1kHz, equally weighted 20 Hz ...16 kHz, R_{Load} = 30 kΩ
	from Analog Input to SCART Output (analog)	MONO_IN, SCn_IN_s → SCn_OUT_s[1)]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz, R_{Load} = 30 kΩ
XTALK	Crosstalk attenuation – PLCC68 – PSDIP64						Input Level = –3 dB, f_{sig} = 1 kHz, unused analog inputs connected to ground by Z<1 kΩ
	between left and right channel within SCART Input/Output pair (L→R, R→L)						equally weighted 20 Hz ... 20 kHz
	SCn_IN → SCn_OUT[1)]	PLCC68 PSDIP64	80 80			dB dB	
	SCn_IN → DSP → SCn_OUT	PLCC68 PSDIP64	74 74			dB dB	
PSRR: rejection of noise on AHVSUP at 1 kHz							
PSRR	AGNDC	AGNDC		80		dB	
	from Analog Input to SCART Output	MONO_IN SCn_IN_s,[1)] SCn_OUT_s[1)]		74		dB	
	from Analog Input to Main/AUX/ SCART Output via DSP	DACp_s[1)]		63		dB	

[1)] “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”

6. Application of the BSP 3501C



Note: Pin numbers refer to PLCC packages, pin numbers for PSDIP packages in brackets.
not connected pins are 2,10,15,16,17,38,39,40,41,53,54,55,62,63,64 (2,3,8,21,22,23,31,32,43,44,45)

7. Data Sheet History

1. Preliminary data sheet: “BSP 3501C Baseband Sound Processor”, March 16, 1998, 6251-469-1PD. First release of the preliminary data sheet.

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