2-input, 1-output video signal switcher

BA7654F

The BA7654F is video signal switch consisting of two input pins (IN1 and IN2), one CTL pin (CTL), and one output pin (OUT). The inputs are sync-tip clamped (synchronous edge of the video input signals are aligned to the same voltage), and as the input impedance is extremely large, it is possible to use a small value for the clamp capacitor (the recommended capacitor is 0.01μF (FZ) ceramic).

●Applications

VCRs, TVs, and other equipment using video signals

●Features

1) Small clamp capacitors can be used (ceramic, 3000pF (Min.), 0.01μF (FZ) (recommended)).
2) Low supply voltage operation possible supply voltage range is 3.7V to 7.7V.
3) Superimposition used for fast switching speed with low switching noise (70ns Typ.).
4) Low power consumption (when V_{CC} = 5V, 25mW Typ.).
5) Wide dynamic range (when V_{CC} = 5V, 3.1V_{P-P} Typ.).
6) Excellent frequency characteristics (10MHz, 0dB Typ.).
7) Low interchannel crosstalk (– 70dB Typ.).
8) Voltage can be applied to the control pins even when V_{CC} is not applied.

●Selected output mode setting table

CTL	OUT
L	IN1
H	IN2

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V_{CC}	9	V
Power dissipation	Pd	500*	mW
Operating temperature	Topr	– 25 ~ + 75	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

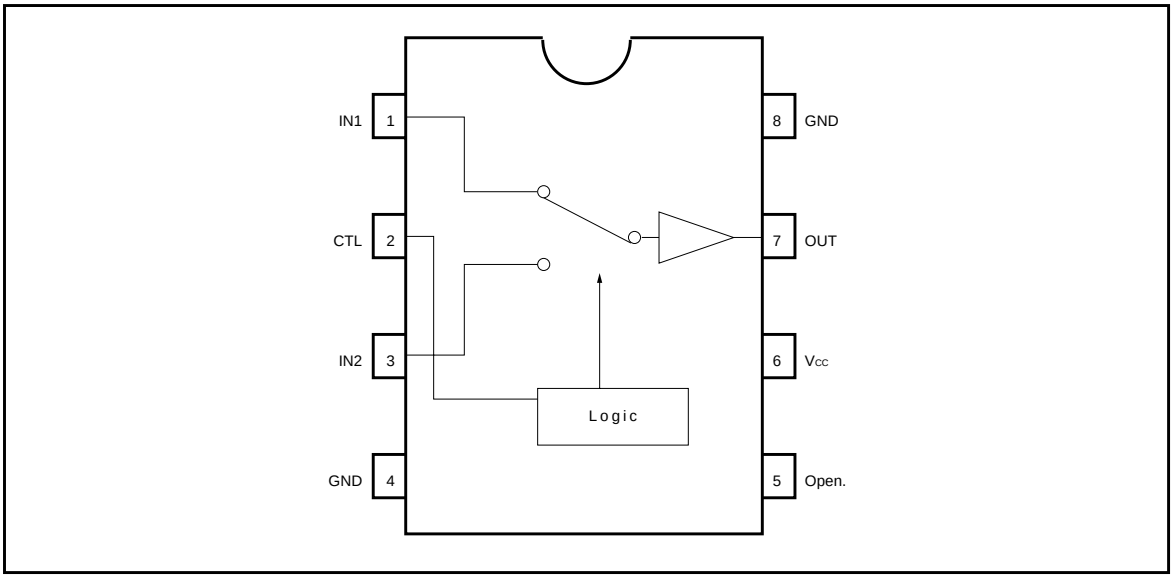
* Reduced by 50mW for each increase in Ta of 1°C over 25 °C.

●Recommended operating conditions (Ta = 25°C)

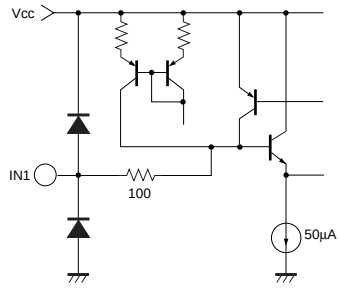
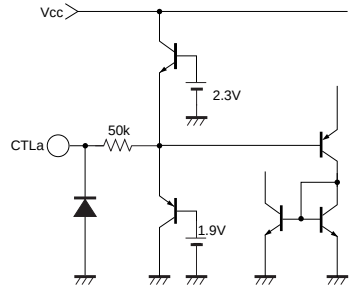
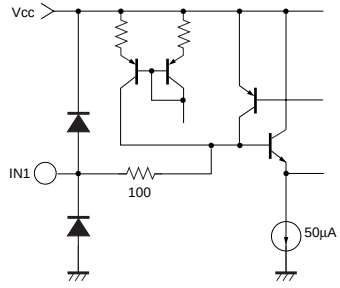
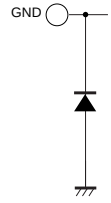
Parameter	Symbol	Limits	Unit
Operating power supply voltage	V_{CC}	4.0 ~ 7.0	V

○Not designed for radiation resistance.

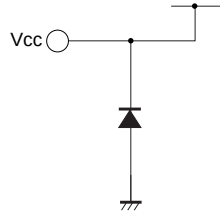
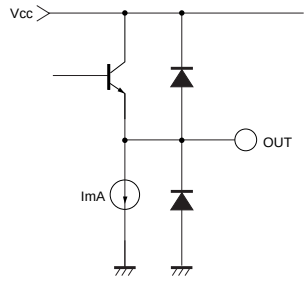
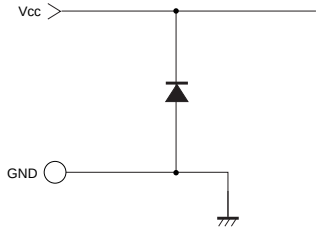
●Block diagram



●Input / output circuits (1 / 2)

Pin No.	Pin name	Reference voltage (V_{CC} = 5V)	Input/output impedance	Equivalent circuit
1	IN 1	1.65V	10MΩ or more	
2	CTL	—	—	
3	IN 2	1.65V	10MΩ or more	
4	GND	—	—	

●Input / output circuits (2 / 2)

Pin No.	Pin name	Reference voltage (V_{CC} = 5V)	Input/output impedance	Equivalent circuit
6	V_{CC}	0.5V	—	
7	OUT	0.95V	26Ω	
8	GND	0V	—	

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage	V_{CC}	3.7	—	7.7	V	—
Circuit current	I_{CC}	2.7	5.0	8.2	mA	—
Maximum output level	Vom	2.6	3.1	—	V_{P-P}	f = 1kHz, THD = 1.0%
Voltage gain	G_V	– 0.5	0	+ 0.5	dB	f = 1MHz, V_{IN} = 1.0V_{P-P}
Interchannel crosstalk	Cta	—	– 70	—	dB	f = 4.43MHz, V_{IN} = 1.0V_{P-P}
Frequency characteristics	Gf	– 3.0	0	+ 1.0	dB	f = 10MHz/1MHz, V_{IN} = 1.0V_{P-P}
CTL switching voltage	VthL	—	—	1.0	V	*
	VthH	2.5	—	—		

* Vcc-CTL Threshold Level

$$Vth = \frac{Vcc\text{-}V_F}{45} \times 20\ (V)$$

●Guaranteed design parameters (unless otherwise noted, Ta = 25°C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential gain	DG	—	0	0.5	%	V_{IN} = 1.0V_{P-P} standard staircase signal
Differential phase	DP	—	0.5	1.0	deg	V_{IN} = 1.0V_{P-P} standard staircase signal

●Measurement circuit

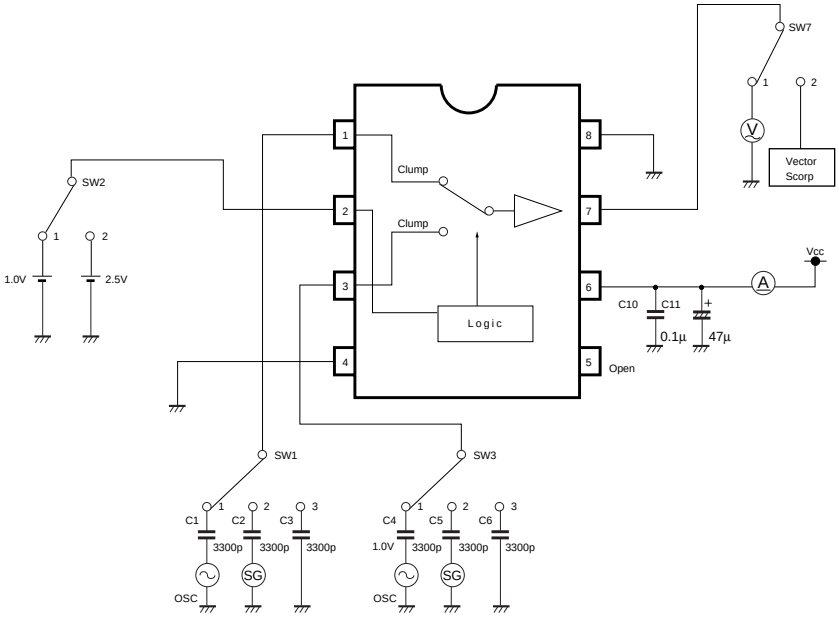


Fig. 1

●Measurement conditions

Parameter		Symbol	SW1	SW3	SW2	SW7	Conditions
Circuit current		Icc	3	3	2	—	—
Maximum output level	IN 1 IN 2	Vom 1 Vom 2	1 3	3 1	1 2	1 1	f = 1kHZ THD = 1.0%*1
Voltage gain	IN 1 IN 2	Gv 1 Gv 2	1 3	3 1	1 2	1 1	V_{IN} = 1.0V_{P-P} f = 1MHz*2
Frequency characteristics	IN 1 IN 2	Gf 1 Gf 2	1 3	3 1	1 2	1 1	V_{IN} = 1.0V_{P-P} f = 1MHz and 10MHz*3
Interchannel crosstalk	IN 1→IN 2 IN 2←IN 1	Cta1 – 2 Cta2 – 1	1 3	3 1	2 1	1 1	V_{IN} = 1.0V_{P-P} f = 4.43MHz*4
Differential gain	IN 1 IN 2	D_G 1 D_G 2	2 3	3 2	1 2	2 2	V_{IN} = 1.0V_{P-P} standard staircase signal
Differential phase	IN 1 IN 2	D_P 1 D_P 2	2 3	3 2	1 2	2 2	V_{IN} = 1.0V_{P-P} standard staircase signal

∗ CTL switching level is substituted by performing the above measurements.

∗1 Connect a distortion meter to the output. After adding a f = 1kHz sine wave input from the OSC, adjust the input level so that the output distortion is 1.0%. The output voltage at that time is the maximum output level Vom [V_{P-P}].

∗2 Apply to the input pin a V_{IN} = 1.0V_{P-P}, f = 1MHz sine wave input.
Voltage gain G_V = 20-log (V_{OUT} / V_{IN})

∗3 Apply to the input pin VIN = 1.0V_{P-P}, f = 1MHz and 10MHz sine wave inputs.
Frequency characteristics Gf = G_V (f = 1MHz) – G_V (f = 10MHz)

∗4 Apply to the input pin a V_{IN} = 1.0V_{P-P}, f = 4.43MHz sine wave input.
Interchannel crosstalk Cta = 20log (V_{OUT} / V_{IN})

●Application examples

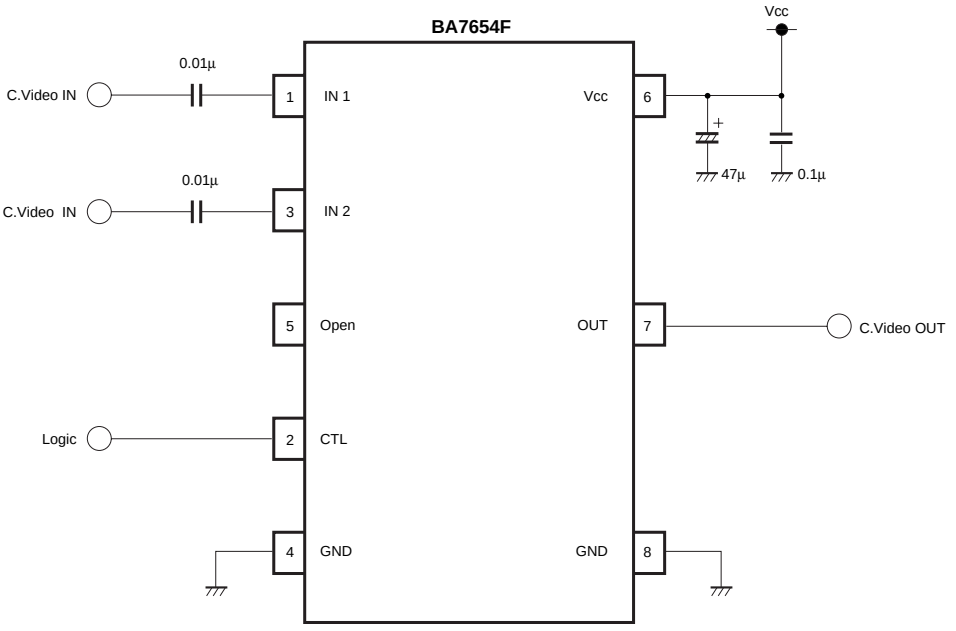


Fig. 2

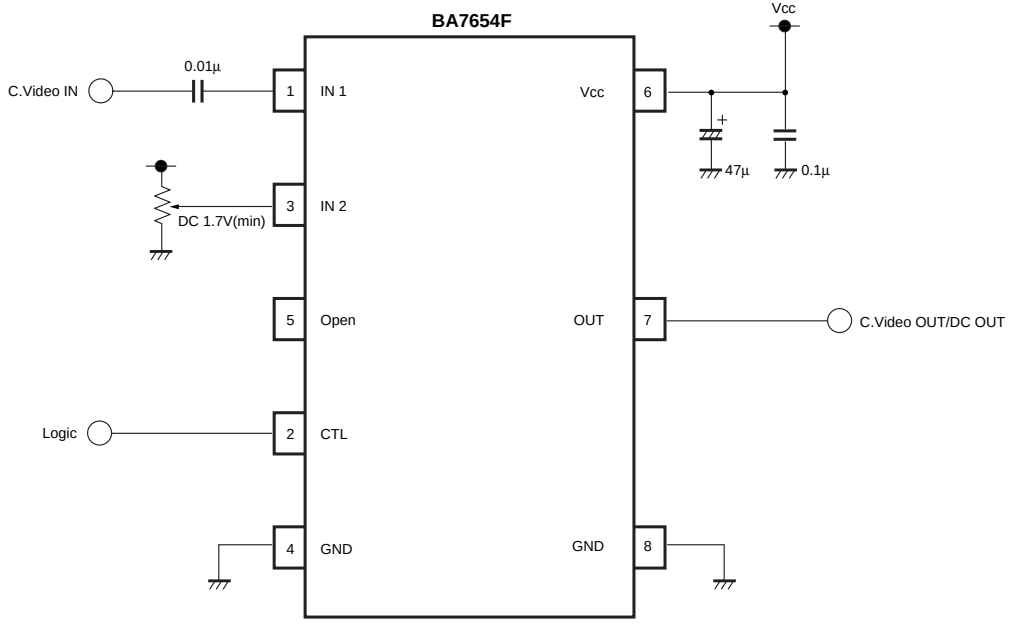


Fig. 3

●Operation notes

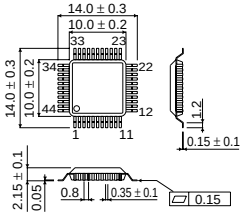
(1) To ensure stable clamp operation, the output impedance of the previous stage connected to the inputs should be 1kΩ or lower.

(2) If large input clamp capacitors are used, the time constant of the circuit will mean that some time will be required until stable operation after power is applied. The value for the input clamp capacitors is 0.1μF max. (0.01μF (FZ) ceramic capacitor recommended).

(3) If CTL pins are unstable when open. Set them to either H or L.

(4) When using superimposition, the DC voltage directly applied to the inputs should be at least 1.7V.

●External dimensions (Units: mm)



QFP44