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50W Current Mode Controlled Offline Switch Mode Power Supply Working over 50% duty cycle using the UC3842A

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The design of a medium power OFFLINE Switch Mode Power Supply based on the Fly-back architecture has been widely developed for the voltage controlled PWM technique.

This application note describes a way to improve the dynamic characteristics of this power supply using a technique called "Current Controlled PWM". A dedicated bipolar integrated circuit, UC 3842A, has been used to achieve the current control, regulation and safety features.

This paper covers the following aspects:

- Power elements dimensioning for a given specification (power switch/inductor)
- Building the current mode regulation
  Current sensing loop
  Feed back loop
- Description of instability occurring at duty cycles greater than 50%
- Description of a compensation network to cancel the instability phenomenon
- Discussion on the compensating network impact on power supply performances

FLYBACK CURRENT MODE CONTROL STRUCTURE

·rent sensing is performed by means of a low value series resistor as shown in Figure 1.

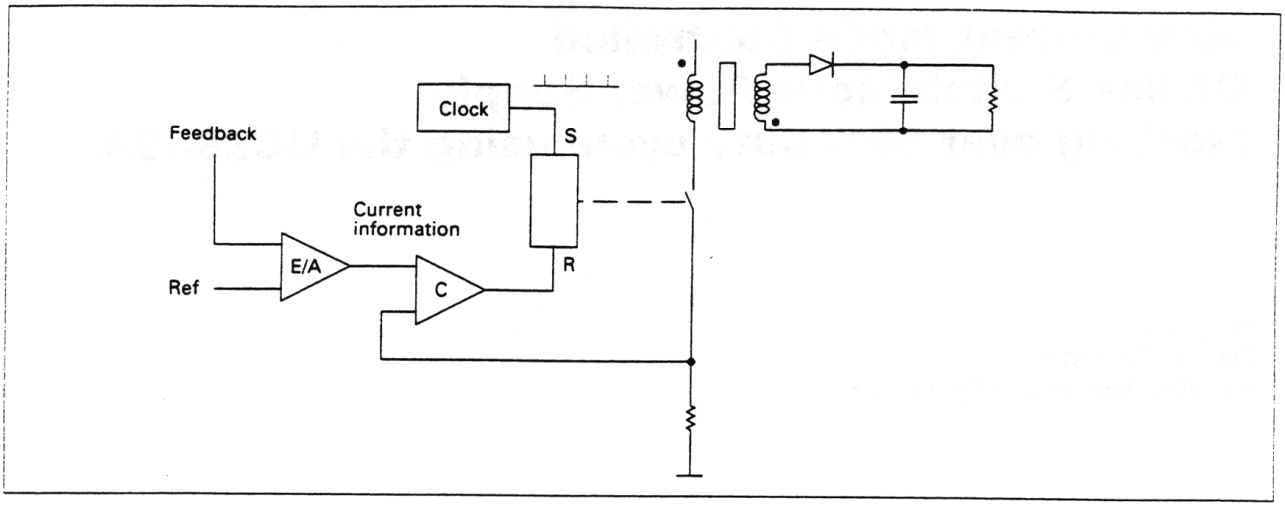

Figure 1
Flyback Current Mode Control Structure

power switch can be a high voltage bipolar transitor or a high voltage N channel MOSFET.
ı ne switch choice is a compromise between performances, safety margin and cost. However these three aspects are not discussed in this study. The adopted switch is a TMOS transistor. The bipolar NPN transitor could also have been selected.

POWER ELEMENTS DIMENSIONING

Power supply specification:

V_{mains} : 85Vac to 245Vac
P_{out} : 50W nominal
100mW standby mode
V_{out} : 5V

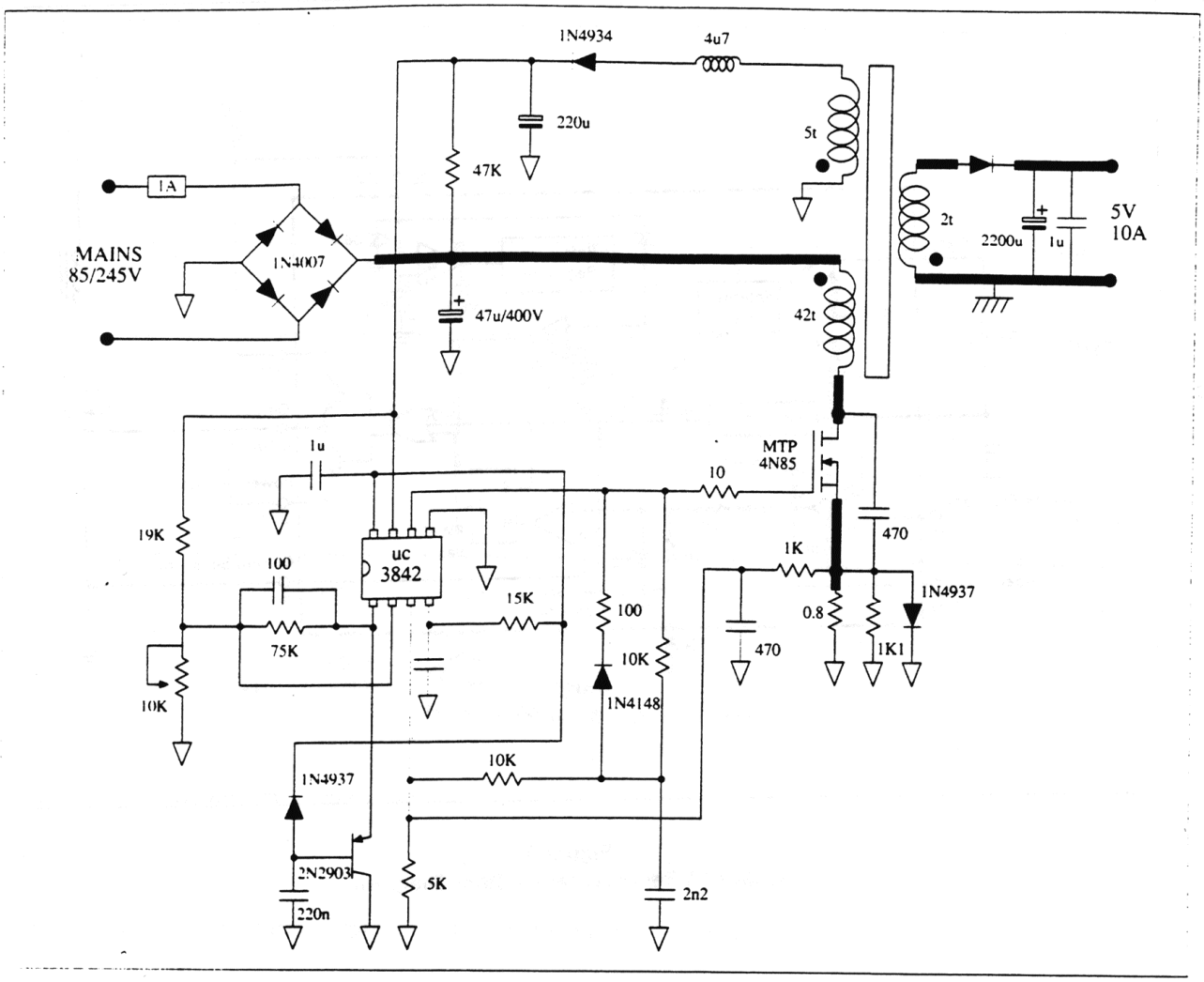

Figure 2
Bi-mains 50W Flyback Power Supply

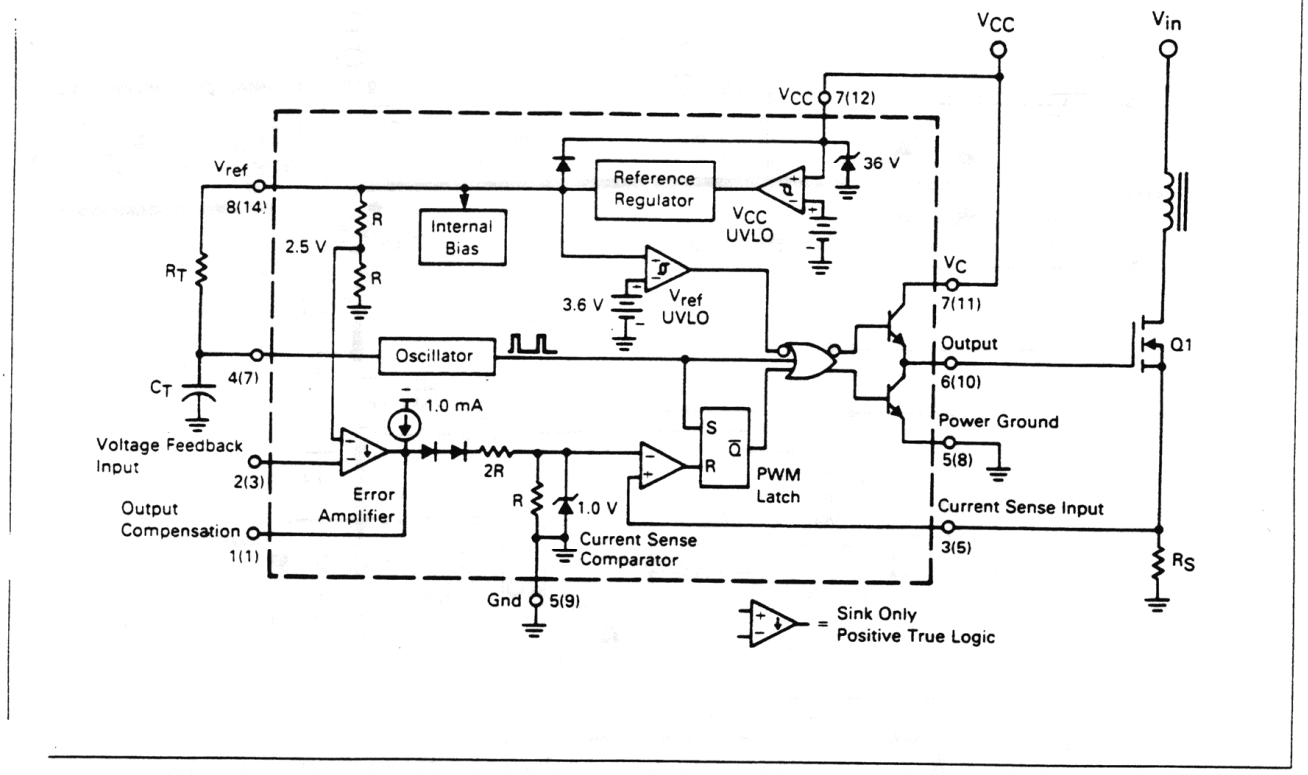

Figure 3
UC3842A Representative Block Diagram

The current flowing in the primary winding is represented by Figure 4.

When the power switch achieves the ON state the current starts climbing from a level which represents the valley current value.

The average current (I_{av}) represented by the dotted line is related to the following working parameters:

P_{max}	maximum output power
$V_{in\ min}$	minimum rectified mains voltage
d	duty cycle
F	working frequency
L_p	inductance of primary winding

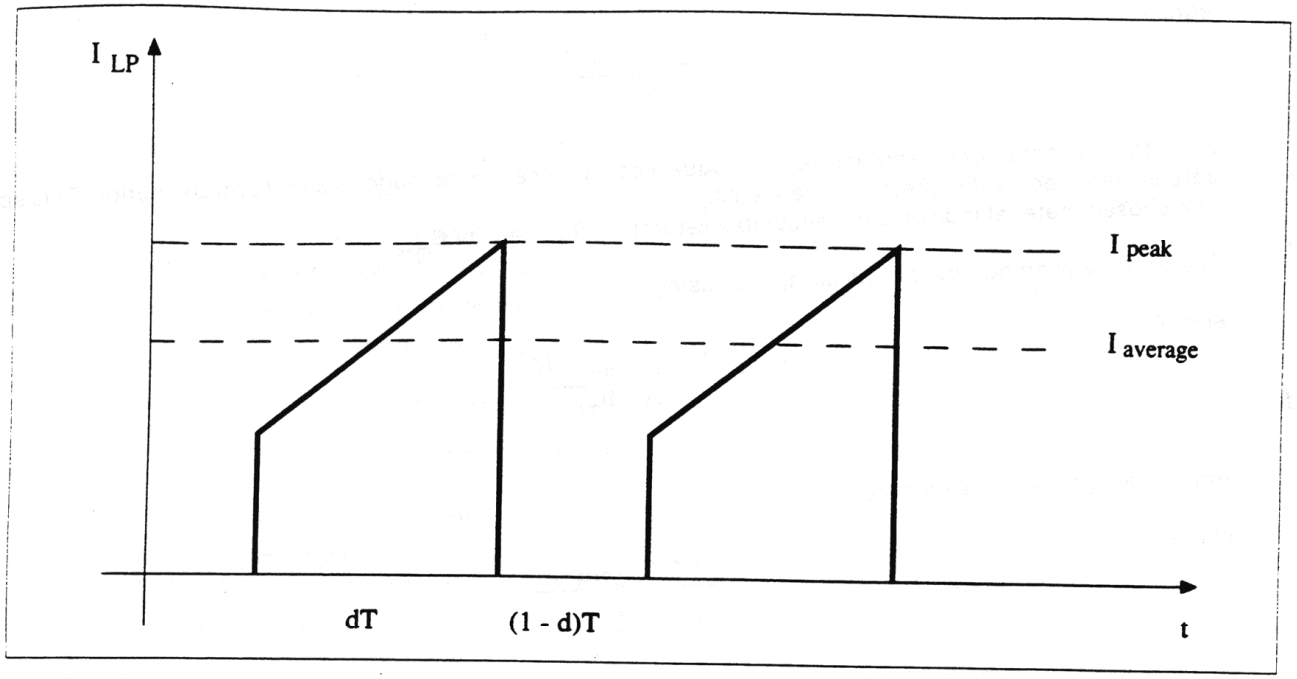

Figure 4
Primary Winding Current Flow

From the current waveform we can write

eqn. 1

$$I_{av} = \left(I_{peak} - \frac{\Delta I_p}{2}\right) d$$

where ΔI_p represents the current ripple of the primary inductor current.

The current ripple is :

eqn. 2

$$\Delta I_p = \frac{V_{in}\ d}{L_p\ F}$$

The energy stored in the primary inductor during one switching period is given by:

eqn. 3

$$W_p = \frac{1}{2}\ L_p \left(I_{peak}\right)^2$$

This energy can also be expressed as a function of the output power divided by the efficiency of the power supply:

eqn. 4

$$W_p = \frac{P_{out}\ T}{\eta}$$

From the equations 2, 3 and 4 we can extract the peak current value:

eqn. 5

$$I_{peak} = \sqrt{\frac{2\ P_{out}\ \Delta I_p}{\eta\ V_{in}\ d}}$$

From the equations 3 and 4 we can extract the required primary inductor value:

eqn. 6

$$L_p = \frac{2\ P_{out}\ T}{\eta\ (I_{peak})^2}$$

From the magnetic core manufacturer catalogue a core choice can be made as a first approximation. This specific core is identified by the effective core area A_e.
The chosen material indicates the allowable saturation flux density B_{max}.

The primary winding now can be computed using:

eqn. 7

$$N_p = \frac{L_p\ I_{peak\ max}\ \ 10^8}{A_e\ B_{max}}$$

And the air gap length becomes:

eqn. 8

$$l_g = \frac{0.4\ \pi\ N_p\ I_{peak\ max}}{B_{max}}$$

The next step is the primary/secondary winding ratio calculation.

The input and output voltages are governed by the relationship:

eqn. 9

$$N_s = \frac{N_p (V_{out} + V_F)(1 - d_{max})}{V_{in\ min}\ d_{max}}$$

In this formula the power transistor saturation voltage has been neglected.

The voltage V_{out} is relatively low and thus the diode forward voltage drop (V_F) cannot be neglected.

The primary/secondary transformer ratio is:

eqn. 10

$$N = \frac{N_p}{N_s}$$

CALCULATION PROCESS

Figure 5 shows the process to be followed to make the optimum choice for every power element.

As a switchmode power supply is largely a compromise between every working parameter, the designer will first have to establish a requirement priority list.

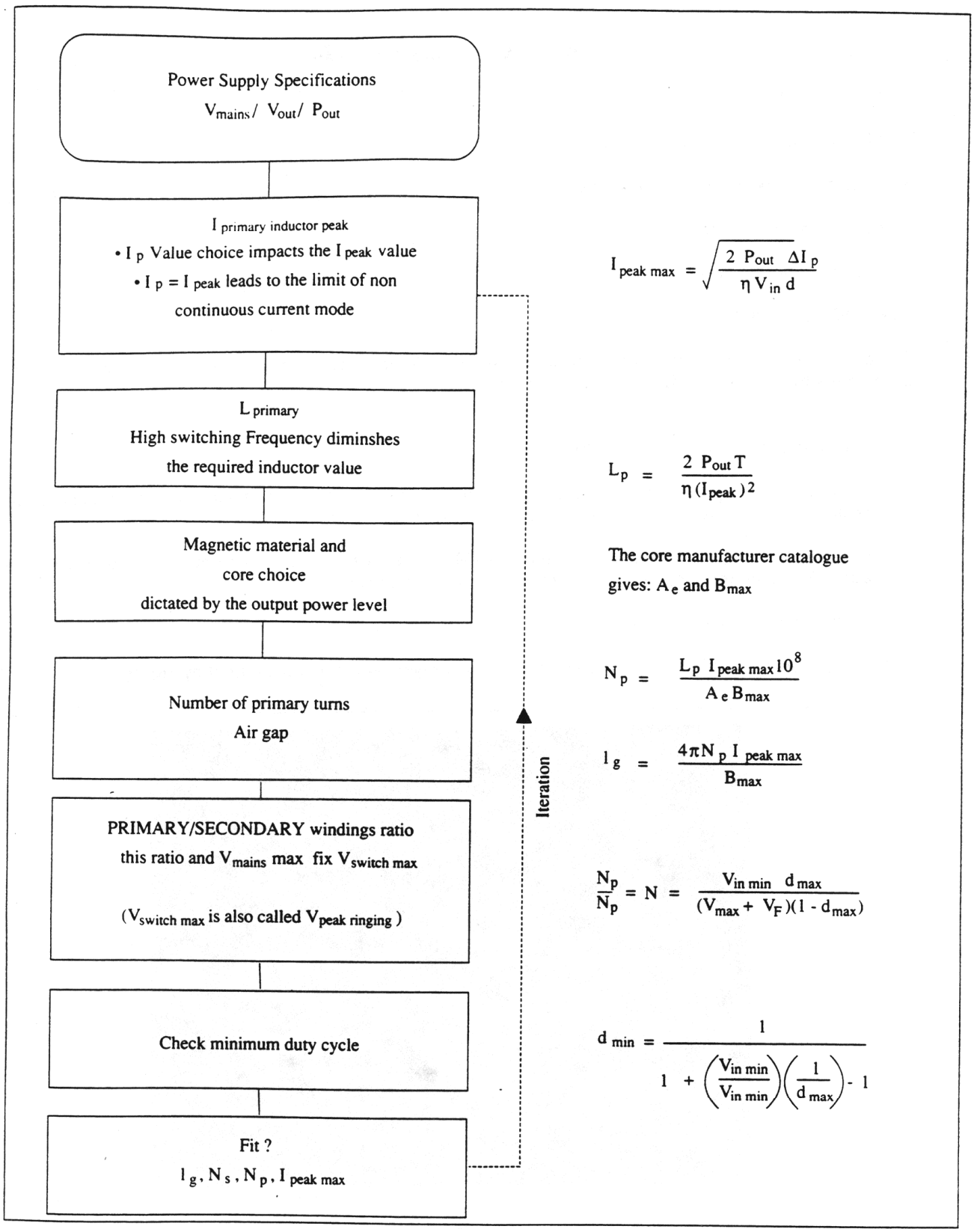

Figure 5
Calculation and Choice Process Chart

The main difficulties encountered in a Switch Mode Power Supply are:

- high dV/dt and dI/dt
- high voltages on the power switch
- rejected interferences on mains line
- conduction and switching losses
- power supply recovery time

PARAMETER CHOICE

The above items are related to the working parameters. What follows is a discussion on the way to adapt these parameters to reduce the impact of the listed difficulties.

a) The high dI/dt can be reduced in two ways:

- diminishing the I_{peak} value - a large L_p value will keep the current ripple at a lower level, but consequently a large inductor value will increase the power supply recovery time.
- lowering the switching speed. When using a TMOS, a series resistor in the gate connection will soften the edge. As a counter effect this will increase the switching losses.

b) High voltage on the power switch

The voltage waveform that has to be sustained by the power switch is represented by Figure 6.

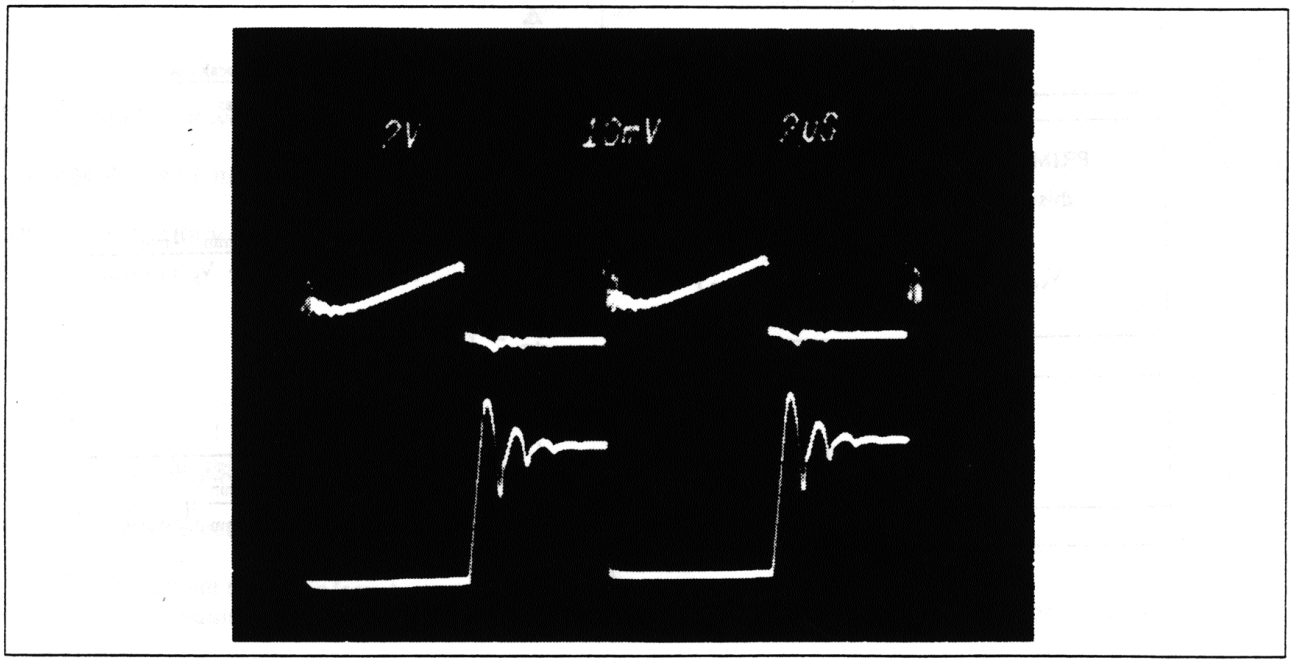

Figure 6
High Voltage on Power Switch

Two voltage levels have to be considered:

1. The *settled voltage* whose value is given by:

eqn. 11
$$V_{settled} = V_{in} + N\left(V_{out} + V_F\right)$$

Substituting the ratio N from equation 9 into equation 11 gives:

eqn. 12
$$V_{settled\ max} = V_{in\ max} + V_{in\ min} * \frac{d_{max}}{1 - d_{max}}$$

2. The *peak voltage* (ringing peak voltage)

The switch-off sequence is shown enlarged in Figure 7.

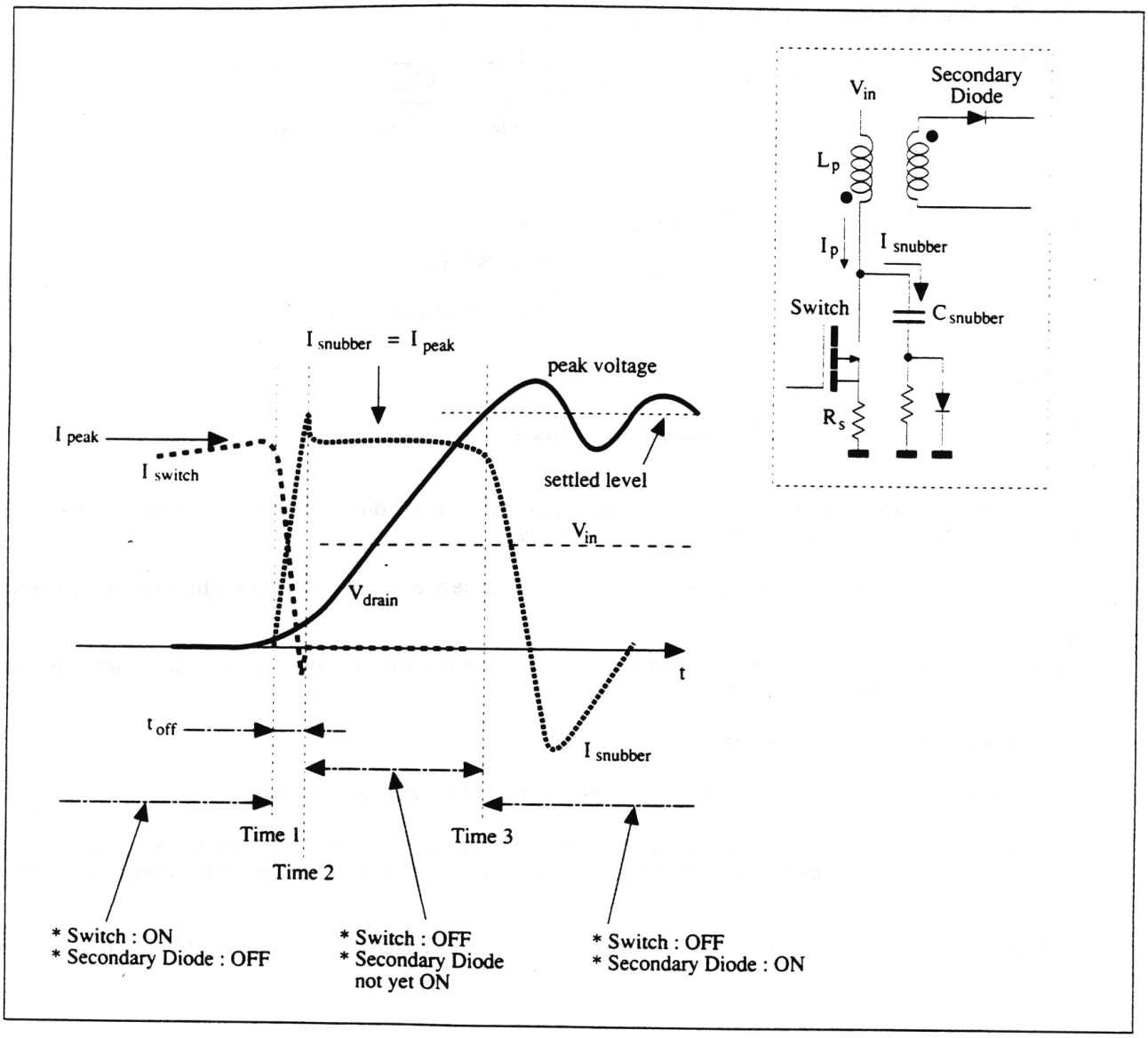

Figure 7
Switch-off Sequence

Time 1: The current flowing through the snubbing capacitor exhibits a shape which is dictated by $L_p + L_{leakage}$ and $C_{snubber}$ added to the transformer stray capacitance and transistor heatspreader capacitance (dotted curve in Figure 7).

Time 2: The switch is OFF. The secondary diode is not yet conducting. The snubbing capacitor receives the whole inductor current.

Time 3: The secondary diode begins conducting.
The voltage across L_p remains constant.
The current flowing through the snubbing capacitor is roughly equal to I_{peak}.
An oscillating energy transfer takes place between $L_{leakage}$ and $C_{snubber}$.
The ringing decay is controlled by the snubbing resistor (only active during the negative conduction).

The peak ringing voltage is given by:

eqn. 13

$$V_{ringing} = I_{csnub} \sqrt{\frac{L_{leakage}}{C_{snub} + C_{oss} + C_{stray}}}$$

eqn. 14

with $I_{csnub} = I_{peak}$

C_{oss} = output TMOS capacitance

C_{stray} = transformer stray capacitance

It becomes:

eqn. 15

$$V_{peak\ ringing} = V_{settled} + V_{ringing}$$

So the designer can try to lower the peak voltage by choosing a low duty cycle in order to reduce the N ratio. As a counter effect the transistor peak current will be higher.

It is clear that special care in the coupled inductors will reduce the leakage inductance thus reducing the ringing.

Note:
Assuming a correct transistor switching behaviour i.e. no current and voltage appearing simultaneously, the t_{OFF} switching time has no impact on the peak voltage.

c) Rejected interferences on mains line

The primary current is flowing in the power network 300V rail and ground rail.

This current is delivered by the rectifying bridge and smoothed by the large value electrolytic smoothing capacitor. This kind of capacitor presents a high ESL (equivalent series inductor) which largely diminishes its high frequency smoothing properties.

Thus the high dI/dt developed by the switch are creating noise voltages which are directly rejected on the mains line.

There are two ways to reduce these interferences :

- lower the dI/dt by decreasing the switching speed.
- insert a symmetrical low pass filter in the mains line.

POWER COMPONENT CALCULATION

Table 1
Units used for Power Components Calculation

Variable	Unit	Abbreviation
I_{peak}	Amperes	A
P_{out}	Watts	W
V_{in}	Volts	V
T	Microseconds	µS
A_e	Square Centimetres	cm2
B_{max}	Gauss	G
N_p	Number of turns	-
L_p	millHenrys	mH
d	decimal notation	-
η	percent	%

We can adopt an estimated efficiency of 75% and a maximum duty cycle of 0.6.

Let us choose a current ripple of ΔI_p = 0.5A and a Period T = 10µs

Switch peak current:

eqn. 16

$$I_{peak\ max} = \sqrt{\frac{2 \times 50\,W \times 0.5A}{75\,\% \times 85V \times \sqrt{2} \times 0.9 \times 0.6}}$$

$$I_{peak\ max} = 1\ A$$

The factor 0.9 gives an estimation of the V_{in} valley ripple voltage.

Primary inductance:

eqn. 17

$$L_p = \frac{2 \times 50\,W \times 10\,\mu s}{75\,\% \times (1\,A)^2}$$

$$L_p = 1.30\,mH$$

We choose the ETD34 core in B52 material.

From the manufacturer's catalogue we get:

Effective core area: 0.97 cm^2
Maximum Flux density: 3200 Gauss

Number of primary turns:

eqn. 18

$$N_p = \frac{1.30\,mH \times 1\,A \times 10^8}{0.97\,cm^2 \times 3\,200\,G}$$

$$N_p = 42\ turns$$

Core air gap:

eqn. 19

$$l_g = \frac{0.4 \times \pi \times 43\ turns \times 1A}{3\,200\,G}$$

$$l_g = 0.17\,mm$$

Primary/Secondary winding ratio:

eqn. 20

$$N = \frac{85V \times \sqrt{2} \times 0.9 \times 0.6}{(5V + 0.5V)(1 - 0.6)}$$

$$N = 30$$

Hence:

eqn. 21

$$N_{5V} = \frac{N_p}{N} = \frac{43}{30} = 1.44\ turns$$

We can now check if there is no saturation problem for this peak current value. It becomes:

eqn. 22

$$N_p = I_{peak\ max} = 43\ turns \times 1\ A = 43\ A \times turns$$

The ETD34 in B52 material fits our power supply requirements.

POWER SWITCH CHOICE

From equation 15 we can compute the maximum voltage which will be withstood by the switch in normal and extreme conditions.

eqn. 23 $$V_{peak\ ringing} = 245V \times \sqrt{2} + \frac{85V \times \sqrt{2} \times 0.9 \times 0.6}{(1 - 0.6)} + 1\ A \times \sqrt{\frac{20\ \mu H}{470\ pF + 150\ pF + 100\ pF}}$$

$$V_{peak\ ringing} = 722\ V$$

Thanks to its "easy to drive" capabilities the power MOSFET is a good choice. A high voltage TMOS should be chosen in order to get maximum safety margin. The MTP4N85 fits our requirements.

For this transistor we get :

eqn. 24 $$R_{DSON} = 4\ \Omega$$
$$V_{DSS} = 850\ V$$

SECONDARY DIODE CHOICE

The current flowing in the secondary side is directly related to the primary current amplitude and the primary/ secondary winding ratio.

The peak value is given as follows:

eqn. 25 $$I_{peak\ diode} = I_{primary\ peak}\ N$$

WIRE SIZE

Let us calculate the skin depth for the considered frequency of 100kHz.

The equation is as follows:

eq. 26 $$\delta = \sqrt{\frac{2\rho}{\omega\ \mu_0}} \quad \text{with} \quad \omega = 2\ \pi F \text{ and } F = \frac{1}{T}$$

where
ρ is the copper resistivity in ohm/metre
μ_o is the absolute vacuum permeability
ω is the working radian frequency

eqn. 27 $$\delta = \sqrt{\frac{2 \times 1.7\ 10^{-8}\ \Omega/m}{2\ \pi \times 100\ kHz \times 4\ \pi 10^{-7}}}$$

$$\delta = 0.2\ mm$$

This skin depth implies the use of multi-layer metal foil or multi-strand Litz wire for the secondary winding.

The winding space for the ETD34 is 20.9mm.

Considering a 0.2mm skin depth we can use a 0.3mm copper foil.

To comply with the isolation norms we have to keep 2mm free space on the two bobbin edges, so the useful winding space becomes:

W = 20.9 - (2 * 2mm)
= 16.9mm

The corresponding copper area is

A_{cu} = 16.9 x 0.3 = 5mm^2

For the 10A average output current we get a current density of 2A/mm^2 which is largely acceptable.

Auxiliary winding:

This winding performs two functions:

- Self powering after power supply start-up
- Feedback voltage sensing

The working voltage of the UC3842A is around 15V, so the number of turns is:

$N_{aux} = 3 * N_{5V} = 5$ turns

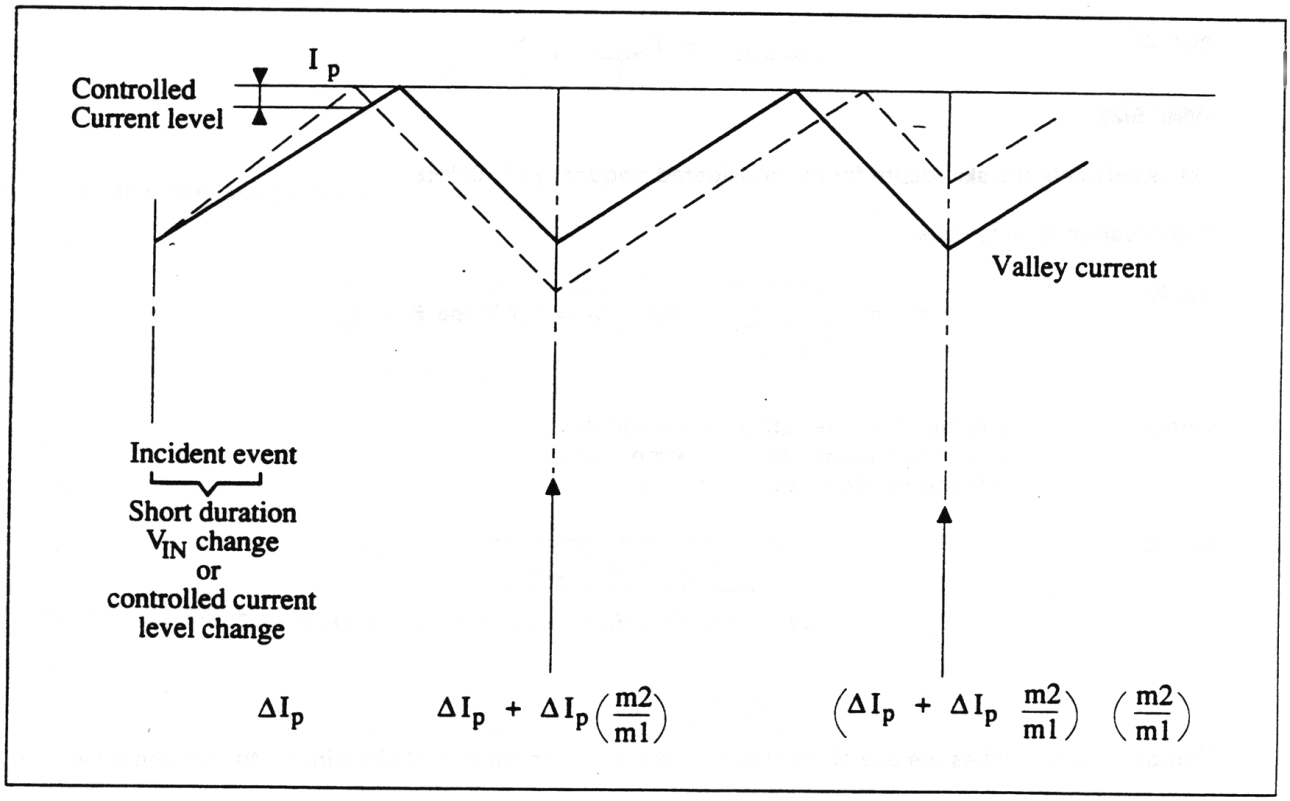

Figure 8
Power Supply Instability

Stability considerations

Constant frequency and controlled current mode power supplies used at duty ratios above 50% exhibit instability even in open-loop configuration.

The nature of the instability appears in Figure 8.

The "ON" current has a rising slope m_1.
The "OFF" current is the secondary current seen from the primary side and scaled with the primary/secondary winding ratio. The OFF slope is m_2 (see equation 35).

The unstable condition is encountered when a short variation in V_{in} or in the controlled current level arises.

This incident ΔI_o is reflected at the end of the ON period and thus the valley current just before the turn ON is increased in amplitude up to $\Delta I\ (m_2/m_1)$.

This variation is also reflected in the next switching cycle and thus the next valley current will be $[\Delta I\ (m_2/m_1)](m_2/m_1)$.

The perturbation is then multiplied on each cycle by m_2/m_1 and alternately increases and decreases the valley inductor current.

After n cycles the inductor current will reach zero and the process recommences until the feedback loop reacts.

This phenomenon is normally not destructive but produces a switching instability and deteriorates the power supply dynamic performances.

The theory establishes that this instability can be cured for the buck boost and the Fly-back converters by adding to the current sense information a compensating slope m_c such as:

eqn. 28

$$\Delta I_n = \left(\frac{m_2 - m_C}{m_1 + m_C}\right) \Delta I_{n-1}$$

Perturbations decrease when the multiplier of ΔI_{n-1} is less than one.
We can also write after n cycles:

eqn. 29

$$\Delta I_n = (-1)^n \cdot \left(\frac{m_2 - m_C}{m_1 + m_C}\right)^n \Delta I_{incident}$$

Two kinds of ramp can be considered:

- Ramp to ensure a marginal open loop stability.
- Ramp to ensure optimal open loop stability.

These two ramps are shown in Figure 9.

(d > 50%)

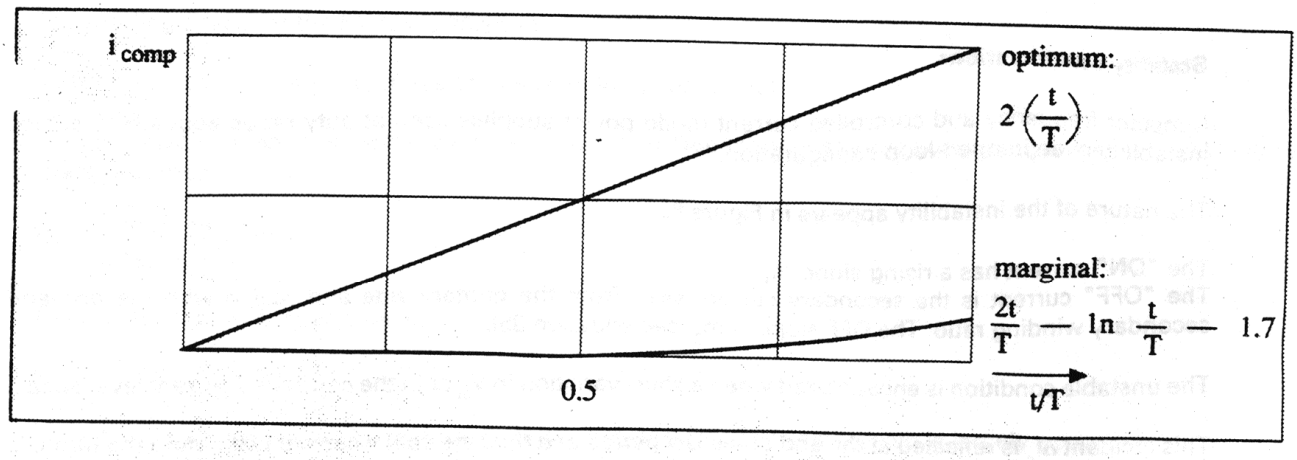

Figure 9
Compensating Ramps

The lowest curve is related to the marginal stability in which the current perturbation remains constant - it neither decreases nor settles down.

We get:

eqn. 30

$$m_c = \frac{m_2 - m_1}{2}$$

The upper curve eliminates any perturbation within one switching cycle. The optimal compensating ramp gives:

eqn. 31

$$m_c\,(opt) = m_2$$

Note that the optimum compensating ramp has a significant impact on the current limiting characteristic.

(d > 50%)

STRUCTURAL INSTABILITY

The working conditions (low mains and high output power) lead to a continuous conduction mode in the core windings. In fact, continuous conduction mode (CCM) in the fly-back structure means that the magnetic field created by the [ampere * turns] never falls down to zero.

In this configuration and using the current mode control technique to achieve the output regulation an instability takes place when the duty cycle exceeds 50% (see previous "d > 50%" section). A way to cure this problem is to modify the current information in such a manner that the ON angle becomes as it should be if the duty cycle was less than 50%.

To perform this angle modification we can act on the error amplifier input or on the current sense input. The data sheet UC3842A/D shows two different ways to set up the current compensation. The described application achieves this compensation in a slightly different manner.

This solution requires some additional low cost components to generate a quasi linear sawtooth only during the t_{on} period. The advantage of this technique is to diminish the dV/dt seen by the current comparator at turn-on. In this way start-up and output short circuit behaviour is improved.

As shown in Figure 10, the sense voltage is the sum of the voltage developed across the sensing resistor R_s which represents the actual primary current and the compensating ramp.

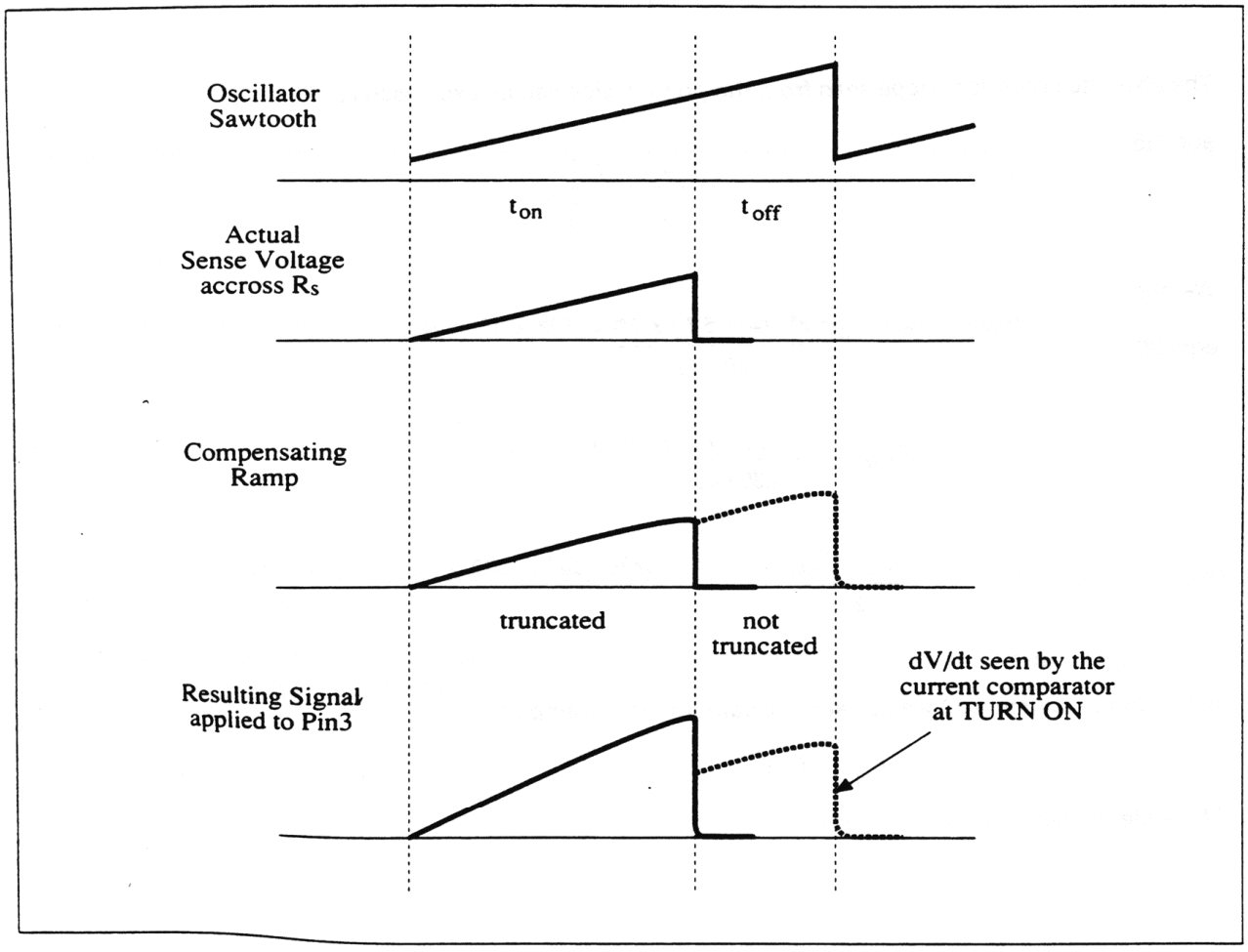

Figure 10
Compensating Signal

COMPENSATION SLOPE CHOICE

As already mentioned, the short circuit current is affected by the additional ramp. In order to lower the compensation impact on the short circuit current limitation but still retain a good stability margin we choose:

eqn. 32 $$\frac{m_2 - m_1}{2} \leq m_C \leq m_2$$

m_2 is the absolute value of the secondary slope.

The secondary diode current is:

eqn. 33 $$I_{diode} = I_{diode\ peak} - \frac{V_{out} + V_{F\ diode}}{L_s} t_{OFF}$$

Seen from the primary side and assuming a tight coupling we can write:

eqn. 34 $$L_S = \frac{L_p}{N^2}$$

The absolute secondary slope seen from the primary side can be expressed as:

eqn. 35 $$m_2 = \frac{\left(V_{out} + V_F\right) N}{L_p}$$

We get:

eqn. 36 $$m_2 = \frac{(5V + 0.5V) \times 30}{1.30\ mH} = 125 \times 10^3$$

$$m_{1\ min} = \frac{110\ V}{1.30\ mH} = 83 \times 10^3$$

$$\frac{m_2 - m_1}{2} = \frac{(124 - 83)}{2}\ 10^3 = 20 \times 10^3$$

According to equation 32 we can adopt a compensating ramp of:

$$m_c = 80.10^3$$

The adder circuit is shown in Figure 11.

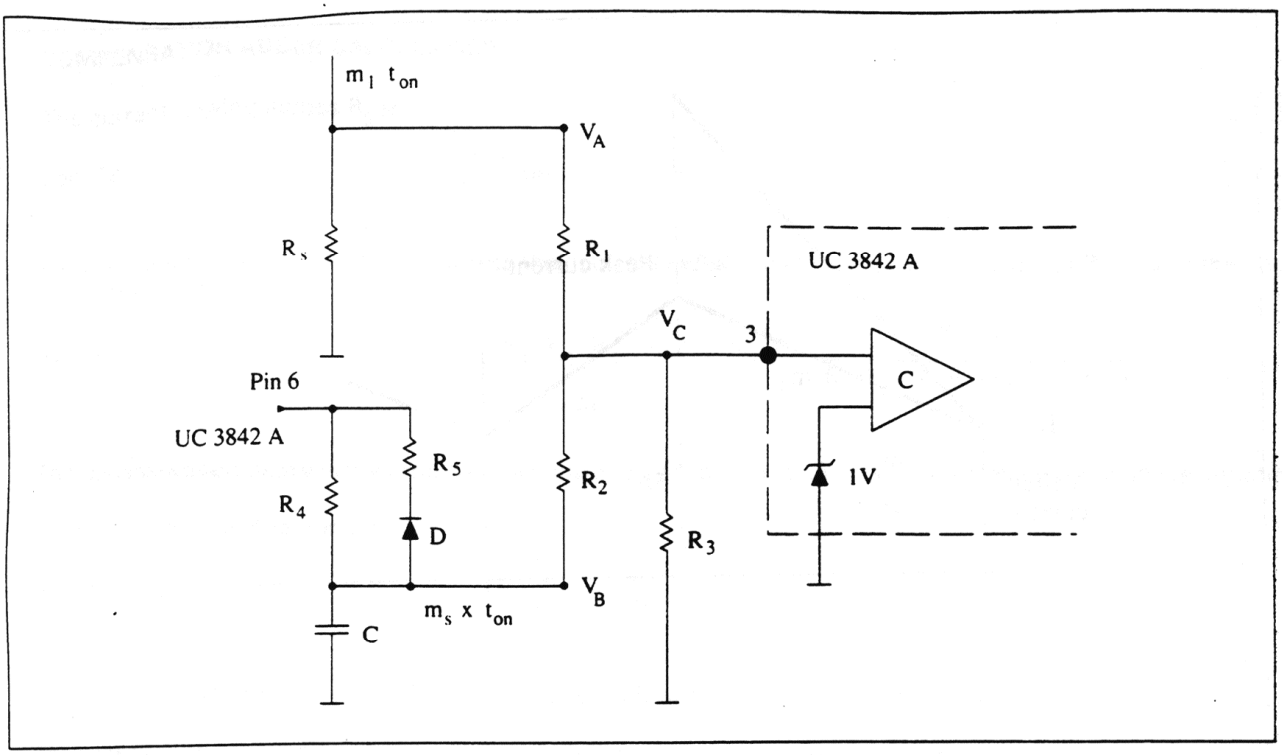

Figure 11
Adder Circuit

The resistors R_1, R_2 and R_3 perform the actual current signal and the compensating slope addition.

The adder equation is :

eqn. 37

$$V_C = \frac{R_3 \left(R_1 V_B + R_2 V_A \right)}{R_1 R_2 + R_1 R_3 + R_2 R_3}$$

The network R_4, R_5, C and D connected on the drive output Pin6 build the compensating waveform. Figure 12 shows the resulting quasi sawtooth.

The power supply voltage feedback is made by means of an auxiliary winding working in the fly-back way. Consequently the V_{cc} voltage is constant and the square wave Pin 6 signal amplitude is constant.

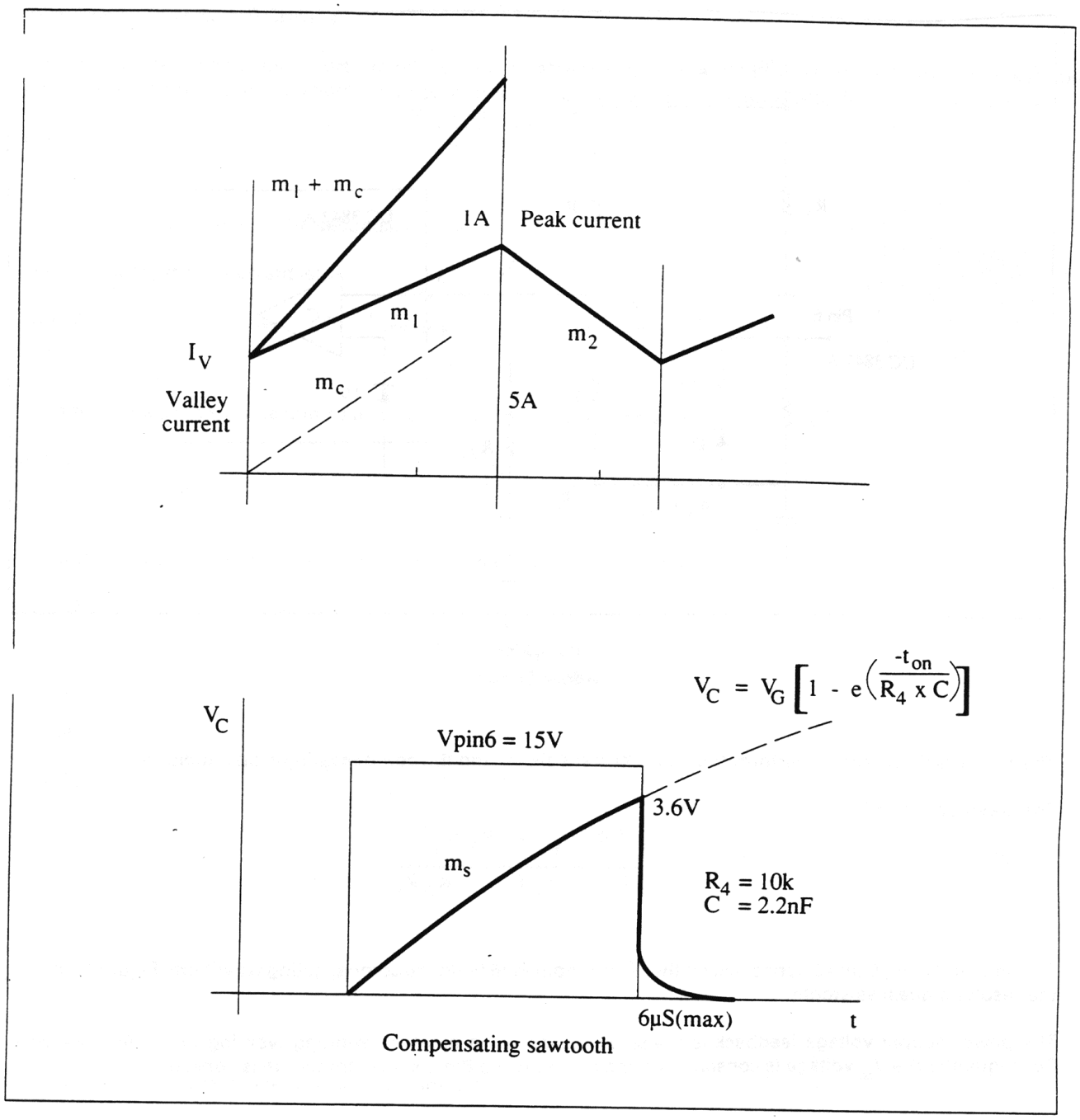

Figure 12
Quasi Sawtooth

Thus the compensating signal has a constant slope m_s whose value is:

1. 38

$$m_s = \frac{3.6\ V}{6\mu s} = 0.6\ V/\mu s$$

COMPENSATION ADDER CALCULATION

The current flowing across R_S is:

eqn. 39

$$I_L = I_{valley} + m_1 \, t_{on}$$

From equations 33 and 37 we can express the "current sense" pin3 voltage as a function of R_S, I_V and the adder network resistors.

eqn. 40

$$V_C = R_S \, I_V + \left(m_1 \, R_S \, R_2 + m_S \, R_1 \right) \frac{R_3 \, t_{on}}{R_1 \, R_2 + R_1 \, R_3 + R_2 \, R_3}$$

The **compensation factor** is the ratio between the two added expressions between brakets in the above equation.

We can define this K factor as:

eqn. 41

$$K = \frac{m_1}{m_c} = \frac{m_1 \, R_S \, R_2}{m_S \, R_1}$$

The "compensation slope choice" section discussed how to choose m_c and the m_c limits.

The compensation slope m_c enables to compute the current sense resistor value R_S.

R_S CALCULATION

Extracting R_2 from equation 41 and solving V_c in equation 40 we can express V_c as a function of I_v, R_1, R_3, R_s, m_1, m_s, and K.

eqn. 42

$$V_c = R_S^2 \left(-\hat{m}_1 \, R_3 \, I_V \right) - R_S \left[(K+1) \, m_1 \, m_S \, R_3 \, t_{on} + K \, m_S \, I_V \, (R_3 + R_1) - m_1 \, R_3 \right] + K \, m_S \, (R_3 + R_1)$$

To simply solve this 2nd order equation the R_1 and R_3 choice can be primarily made.

Let us choose:

$$R_1 = 1 \, K\Omega$$
$$R_3 = 5 \, K\Omega$$

eqn. 43

From the sections "Power component calculation" and "Compensation slope choice" we have :

eqn. 44

$$I_{valley} = I_{peak} - I_{ripple} = 0.5 \text{ A}$$
$$K = 1$$

with $m_1 = 80 \; 10^3 \text{ A/s}$

and $m_S = 600 \; 10^3 \text{ V/s}$

The roots of the equation 42 are:

eqn. 45

$$R_S = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

where: $a = m_1 R_3$

$$b = (K+1)\, m_1 m_S R_3 t_{on} + K m_S I_V (R_3 + R_1) - m_1 R_3$$

$$c = K m_S (R_1 + R_3)$$

The sole root is :

$$R_s = 0.81\Omega$$

From equation 41 we get:

eqn. 46

$$R_2 = \frac{K m_s R_1}{m_1 R_s}$$

$$R_2 = \frac{1 * 600 * 10^3\ V/\mu s * 1k\Omega}{80 * 10^3\ A/\mu s * .81\ \Omega}$$

$$R_2 = 9.3k\Omega$$

For safety and reliability reasons, the power supply short-circuit behaviour is a key point.

Two kinds of short circuit can be considered:

- on the load
- on the secondary diode

LOAD SHORT CIRCUIT

The first case shows a strong output voltage decrease. The control voltage reacts dictating a high primary current level. The current sense comparator works at the Pin 3 clamped voltage i.e. 1 volt.

The primary inductor current appears in Figure 13.

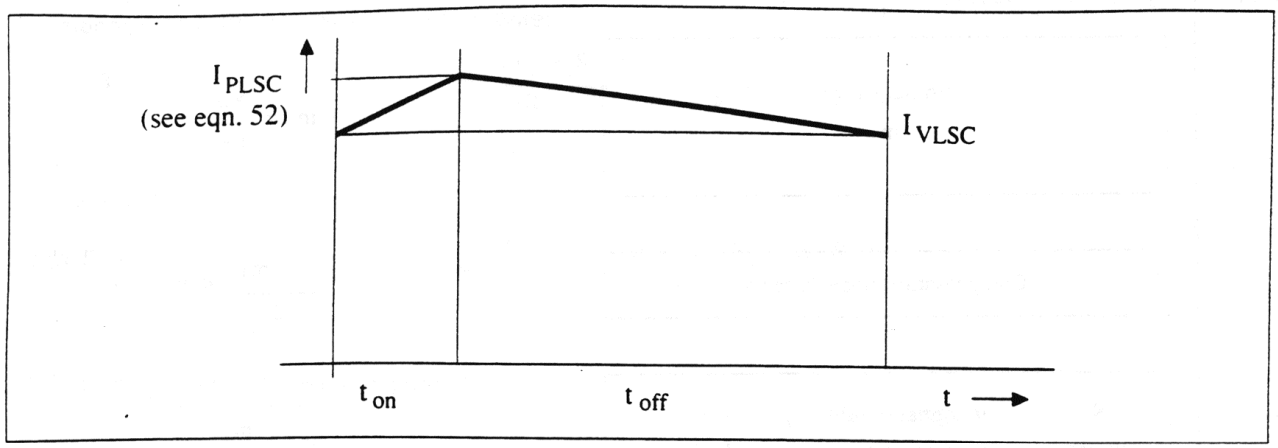

Figure 13
Primary Inductor Current

In this configuration the duty cycle is:

eqn. 48

$$d = \frac{V_F \ N}{V_{in}}$$

For the minimum mains we get:

eqn. 49

$$d_{max} = \frac{0.6V \times 30}{85V \times \sqrt{2} \times 0.9} = 0.17$$

which gives:

eqn. 50

$$t_{on\ max\ load\ sh.\ ckt} = 1.7\mu S$$

From equation 39 we can get the valley current I_V and can express the Load Short Circuit peak current as follows:

Load Short Circuit Valley Current: I_{VLSC}
Load Short Circuit Peak Current: I_{PLSC}

eqn. 51

$$I_{VLSC} = I_{PLSC} - \frac{V_{in}\sqrt{2}\ 0.9\ t_{on}}{L_m}$$

From equation 40 and taking V_{cmax} = 1 volt with the previously chosen and computed values R_1, R_2, R_3 and R_s we get:

eqn. 52

$$I_{PLSC} = \frac{0.835 + 0.14}{R_s} \text{ Amperes}$$

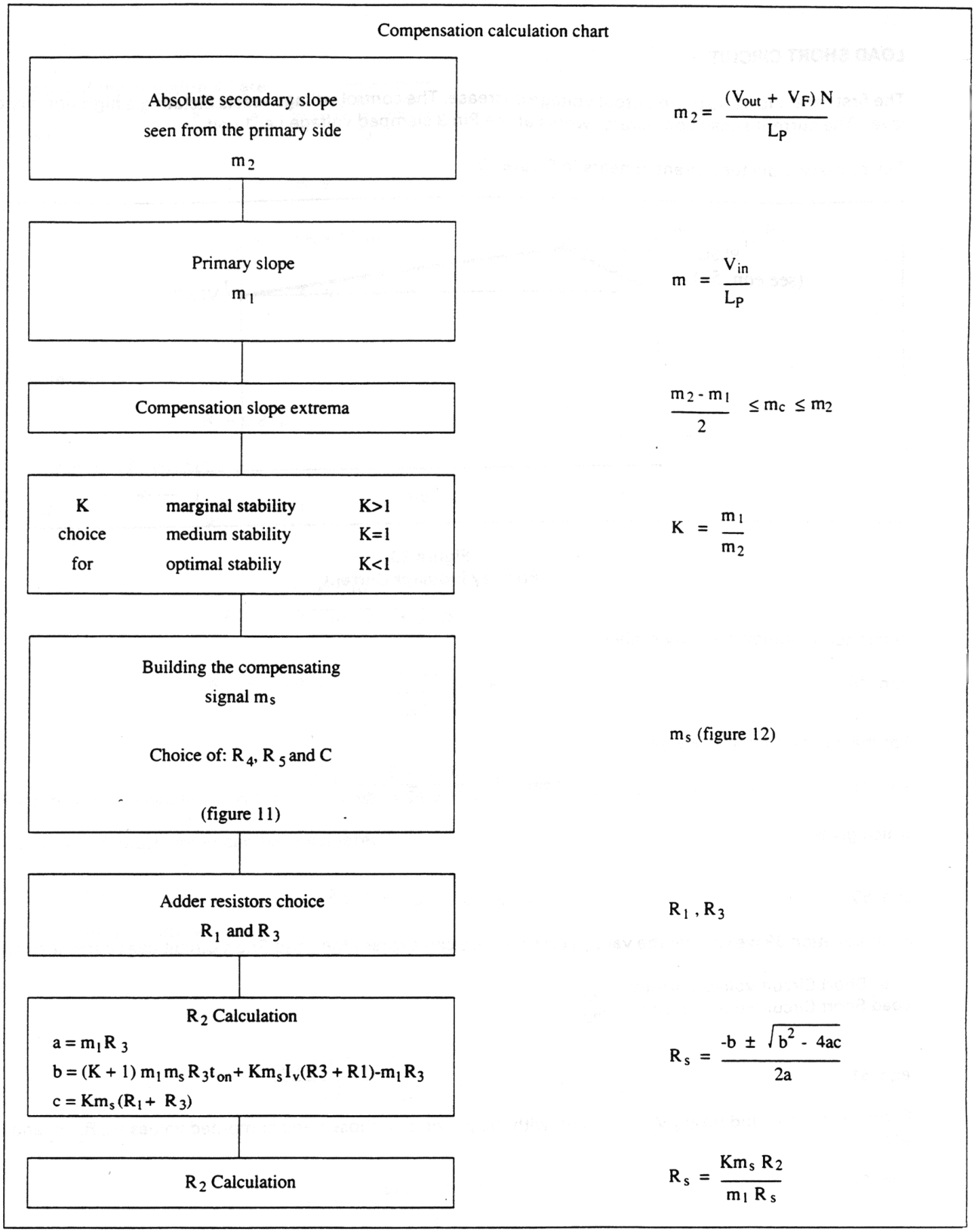

Figure 14
Compensating Calculation Chart

DIODE SHORT CIRCUIT

Diode Short Circuit Peak Current: I_{PDSC}

This particular configuration can be encountered subsequently to a load short circuit in which case the power switch current is mainly dictated by the leakage inductance. The resulting current rising slope is much higher than the compensation slope and we can approximate:

eqn. 53
$$I_{PDSC} = \frac{(R_1 + R_3 // R_2)\ V_{cmax}}{(R_1 + R_3 // R_2)\ R_5}$$

which gives:

eqn. 54
$$I_{PDSC} = \frac{V_{cmax}\ (R_1 R_3 + R_1 R_2 + R_3 R_2)}{R_s R_2 R_3}$$

This current slope is shown in Figure 15.

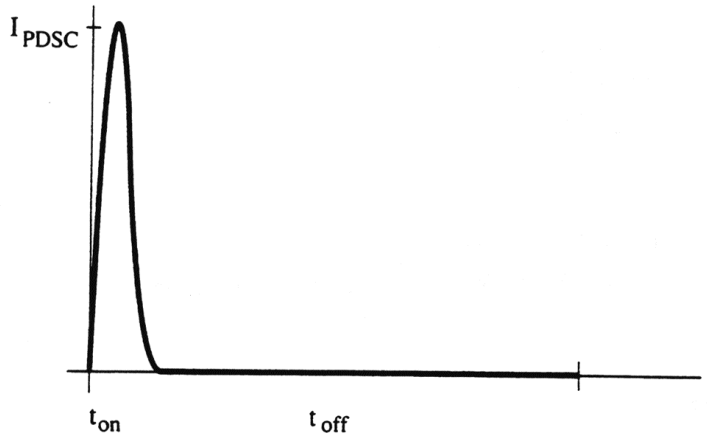

Figure 15
Diode Short Circuit Peak Current

We can summarize the above results for 3 different K factors :

			For V_{mains} = 85 V	
K	R_S	R_2	I_{PDSC}	I_{PLSC}
Marginal stability K = 4	1 Ω	30 KΩ	1.23 A	0.97 A
Medium stability K = 1	0.8 Ω	9.5 KΩ	1.63A	1.18 A
Optimal stability K = 0.64	0.7 Ω	7 KΩ	1.92 A	1.33 A

eqn. 55

$$R1 = 1\ k\Omega$$
$$R3 = 5\ k\Omega$$
$$k = \frac{m_1}{m_c}$$

$$m_1 = 80\ 10^3\ A/S$$
$$m_S = 600\ 10^3\ V/S \qquad \frac{m_1 - m_2}{2} < m_c \leq m_2$$

PERFORMANCES

LINE REG	P_{out} = 50W	V_{mains} = 85Vac V_{mains} = 245Vac	V_{out} = 5.16V V_{out} = 5V
LOAD REG	V_{mains} = 220Vac	P_{out} = 20W P_{out} = 40W	V_{out} = 6V V_{out} = 5.6V
d_{max}	P_{out} = 50W	@ 85 Vac	0.6
d_{min}	P_{out} = 50W	@ 245 Vac	0.34

CONCLUSION

A complete Switch Mode Power Supply has been described. The aim of this study was not to obtain the best load and line performances and for this reason a very simple feedback network has been adopted. Excellent start-up and short-circuit behaviour have been obtained by the use of the current control mode technique. Unfortunately this high performance technique exhibits a major problem of instability which appears when the duty cycle exceed 50%. This application note has explained this instability inherent to the current control mode. A compensating network has been implemented and a discussion allows the designer to predict its impact on the power supply general performances.

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