ANE402

130W Ringing Choke Power Supply using TDA4601

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This application note describes a multiple output switch-mode power-supply delivering a total output power of 130 Watts.

The architecture is based on the fly-back mode working in a free switching mode. Frequency range varies between 20 kHz at full load and 70 kHz in the stand-by condition (also called sleep-mode). Input power is from the mains (220V ac) and is completely isolated from the output. Control and regulation are achieved by the IC TDA4601.

The power-supply presents a linear foldback characteristic and is short-circuit proof. An under-voltage inhibit provides a protection against low mains level.

The complete system is an excellent compromise between complexity, cost and performance.

PRELIMINARY

TV and computer monitor requirements for a power supply are:

- Primary/Secondary isolation
- Wide mains voltage range including European 220V mains.
- Output power 50W to 150W.
- 1% output voltage precision.
- Good efficiency 80%.
- Low volume.
- Low cost.

The self-oscillating fly-back converter approach provides isolation. See Fig. 1. Using a direct sawtooth modulation with no dead time in the switching sequence, a wide mains variation can be achieved.

The power switch in a fly-back configuration has to withstand a voltage which is roughly twice as big as the rectified mains line i.e. 650V. Because of ringing and safety margin, designers generally consider 1200V BVCES as a minimum requirement. In this range, the bipolar transistor is still the solution.

The bipolar high voltage transistor implies a low switching frequency due to rather high $t_{STORAGE}$ and t_{FALL}.

In order to minimize the external component count the simplest feedback method has been chosen. This choice is a compromise between set up simplicity and good regulation performance.

The application described in this note is built around the IC TDA4601. The following aspects will be discussed:

- Feed forward action,
- Output regulation,
- Self IC powering after start-up,
- Power transistor drive,
- Output power limitation,
- Fold back characteristic,
- Start-up and stand-by mode.

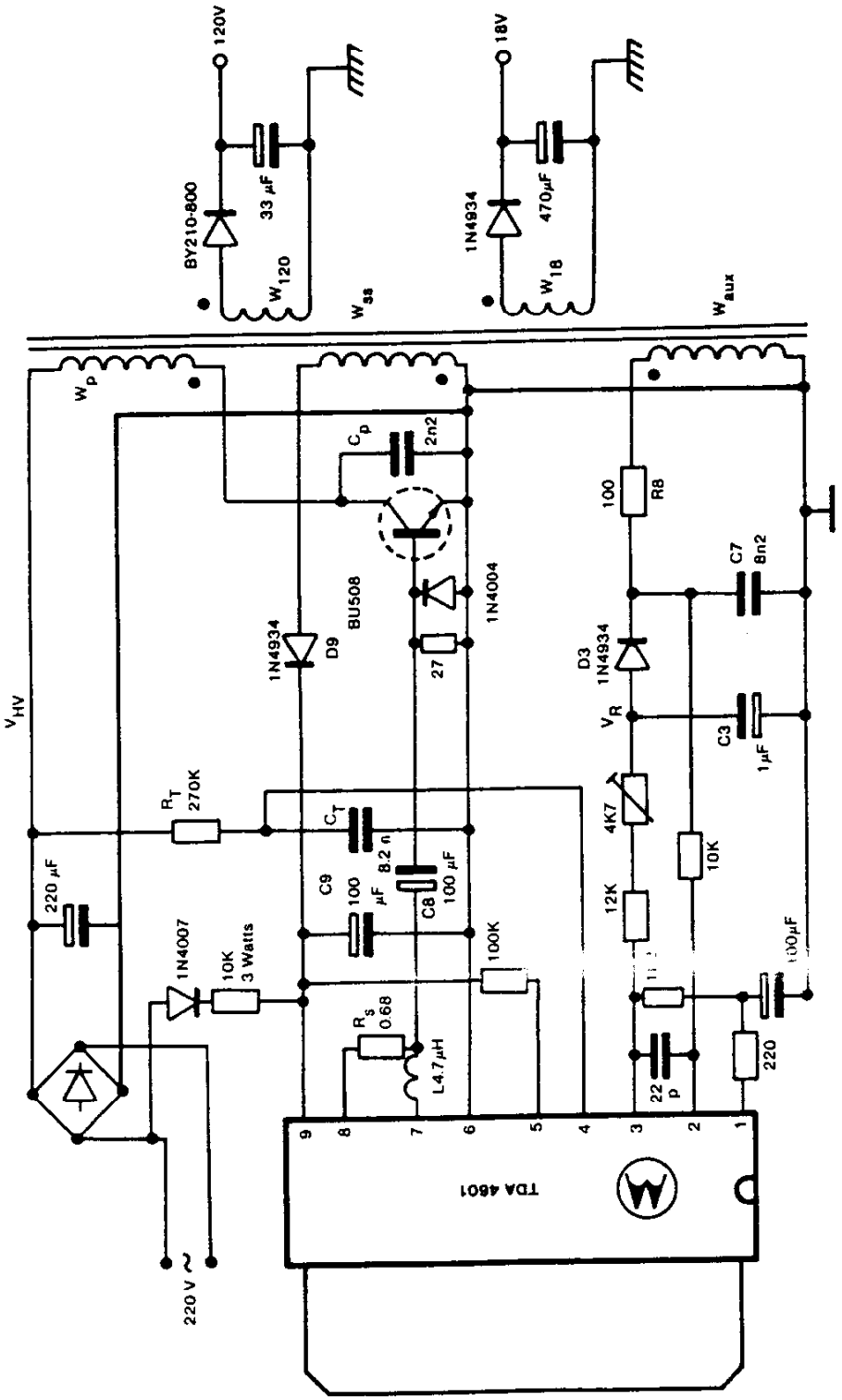

120V
18V
BY210-800
33 µF
1N4934
470µF
W120
W18
Wss
Waux
Wp
Cp
2n2
100
R8
C7
8n2
1N4004
BU508
D9
1N4934
27
D3
1N4934
VHV
VR
C3
1µF
RT
270K
CT
8.2 n
4K7
220 µF
C9
100 µF
C8
100 µF
10K
12K
1N4007
10K
3 Watts
100K
Rs
0.68
L4.7µH
22 p
220
TDA 4601
220 V ~

Figure 1

TDA4601 IC

This IC is built in low voltage bipolar technology (20 V). It is supplied in two different packages:

- SIL 9 pins.
- DIL 18 Pins.

The internal architecture appears in Fig. 2.

THEORY OF OPERATION

The system works in a fly-back configuration on the verge of continuous - discontinuous inductor current.

The switching period is divided into two different periods:

- t_{ON} power switch is ON
- t_{OFF} power switch is OFF

Assuming that the primary winding is a linear power inductor, during the ON period the primary current is dictated by the high voltage input source and by the magnetizing inductance value.

The secondary windings are connected to the output diodes so that no current can flow during the ON time.

When the power switch turns OFF the amount of energy stored in the magnetic core is directly related to the inductance current peak value.

The current interruption in the primary winding generates a reverse voltage variation on the secondary side and thus an energy transfer into the load is activated. During the OFF time the current is dictated by the output voltage level and by the secondary inductance value.

After transfer completion, the secondary voltage collapses. This voltage variation is fed by means of an auxiliary winding to the TDA4601, thus reactivating a new ON period.

The SMPS is therefore working in a self-oscillating mode in which the working frequency depends on input voltage and output power level.

Output voltage regulation is achieved using again the auxiliary winding which provides after rectification and smoothing (Diode D3 and capacitor C3) a negative voltage V_R proportional to the output voltage value.

The accuracy of this technique is not great but is good enough to meet such an application requirement. Input regulation is acomplished by a "feed forward action" through the sawtooth generator.

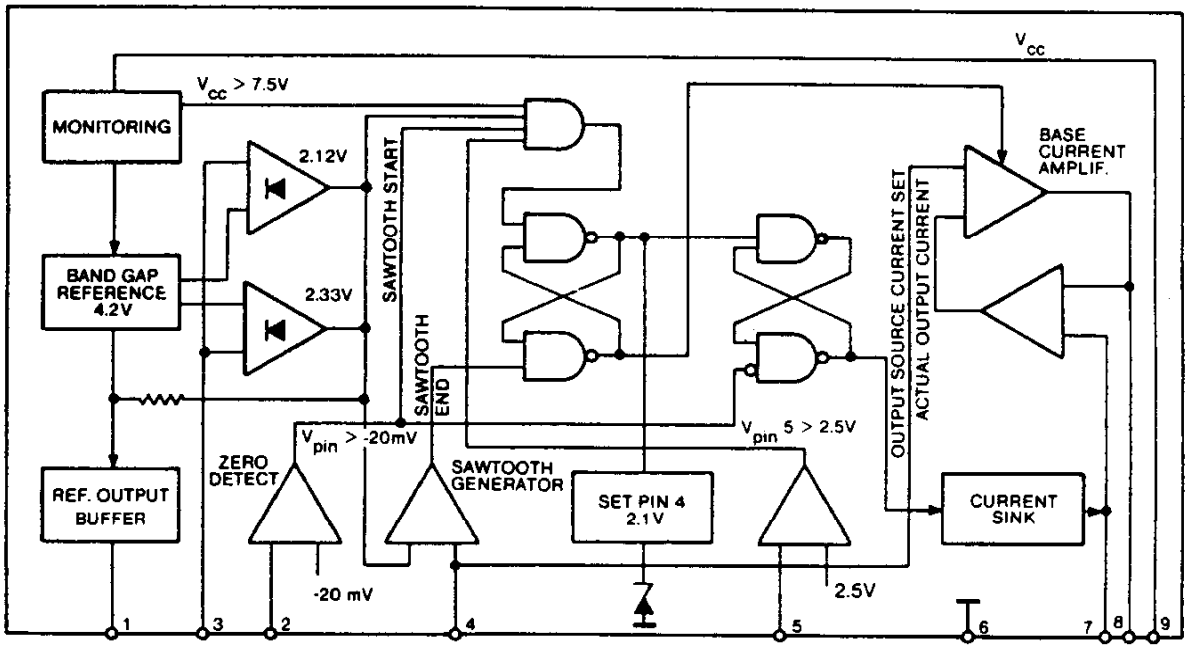


Figure 2

FEED FORWARD INPUT REGULATION

Sawtooth generator (Figure 3)

An RC network is provided on Pin 4 (C_T R_T). The sawtooth slope during t_{ON} is given by equation 1

$$i_{C_T} \times t_{ON} = C_T \times V_{pin4} \qquad \text{Eq. 1}$$

where

$$i_{C_T} = \frac{V_{HV}}{R_T} \qquad \text{Eq. 2}$$

therefore the sawtooth slope is $\frac{V_{HV}}{R_T C_T}$

When the voltage across C_T reaches V_c the capacitor is rapidly discharged and its voltage remains at 2.1 V until a new ON period occurs. So we can see that t_{ON} is directly related to V_{HV}.

The advantage of this technique is a direct V_{HV} sensing, eliminating any reaction delay - t_{ON} is directly modulated by mains line voltage variations. This is the feed forward action. The sawtooth generator appears as if it is the theoretical primary inductor current. Fig. 4 shows a comparison between a real controlled current source architecture and the TDA4601 approach.

Sawtooth Generator

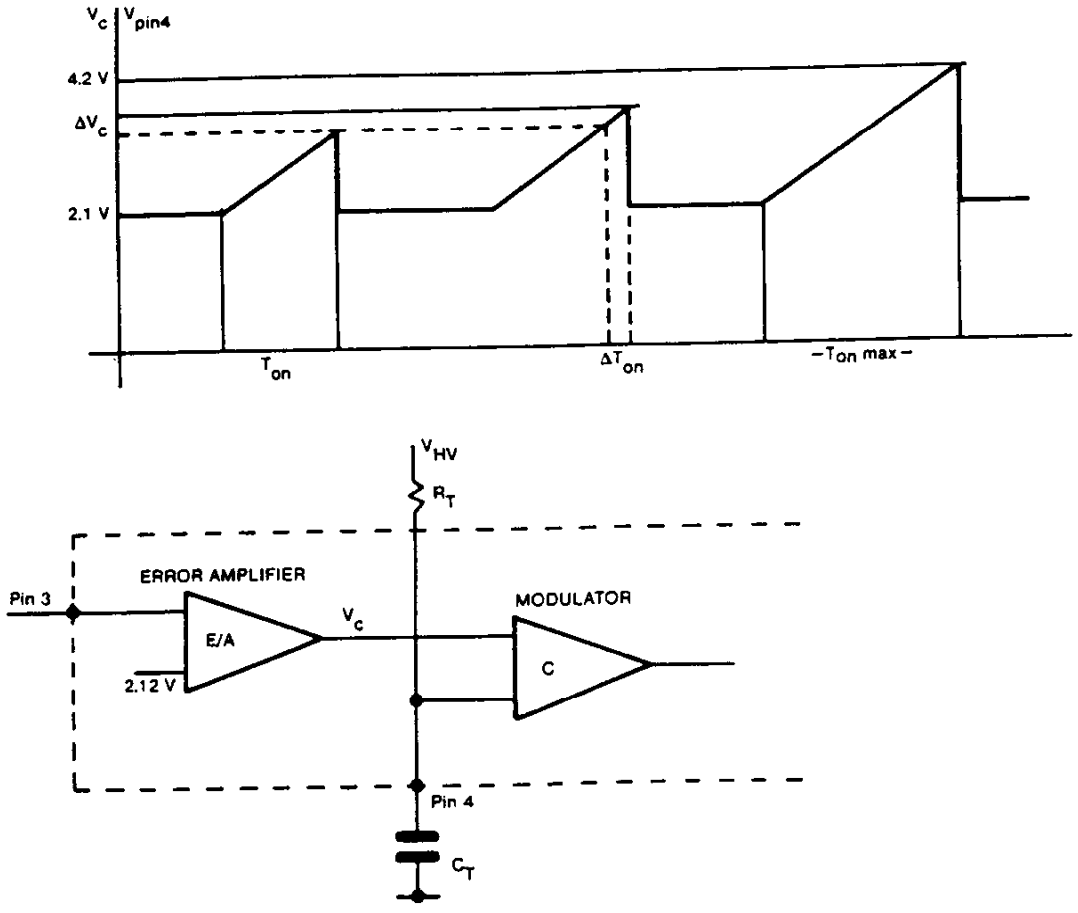


Figure 3

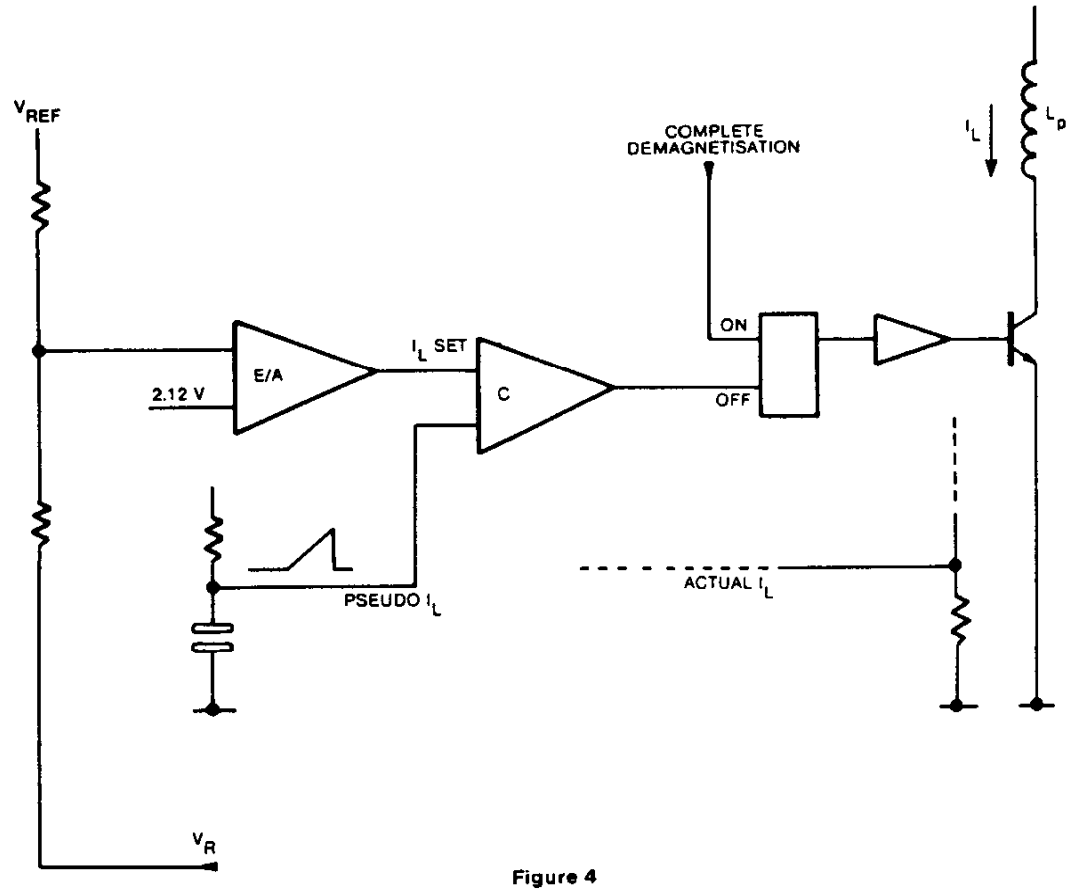


Figure 4

POWER SWITCH BASE DRIVE

The chosen power switch is the TO3P BU508. The choice has been dictated by several reasons:

- high voltage technology required by the European mains voltage 220 vac $BV_{CEO(SUS)}$ 700 V.
- low cost compared to Darlington or TMOS devices.
- BU508 is also the switch for TV deflection.

This power supply was primarily developed only for TV applications.

BU508 main characteristics.

V_{CES}	1550 V
I_C continuous	8 Adc
T_F	0.5 μSec @ I_C = 4.5A
$H_{FE\ min}$	2.25 @ I_C = 4.5A and V_{CE} = 5V

Medium switching characteristics and low HFE imply designating an optimised base drive in order to diminish switching losses.

PROPORTIONAL BASE DRIVE

This is achieved by the TDA4601 output buffer.

The sawtooth waveform on Pin 4 is converted internally into a sawtooth current pulse sourced from Pin 8.

This pulse is driven through capacitor C8 to BU508 base. So choosing the right R_TC_T value produces a base current proportional to collector current.

CALCULATION R_TC_T · SAWTOOTH WAVEFORM

The primary inductor current in the flyback configuration is given by Eq. 3.

$$I_{peak\ prim} = \frac{V_{HV}}{L_p} \times t_{ON} \qquad \text{Eq. 3}$$

Where

- V_{HV} is the rectified a.c. mains voltage
- L_p is the primary magnetizing inductance
- t_{ON} is max when V_{HV} is min and P_{OUT} max
- t_{ON} is chosen in the application at 20 μsec

Substituting Eq. 2 in Eq. 1 and solving for ΔV_C

$$\Delta V_{C(max)} = \frac{V_{HVmin}}{R_T C_T} \times t_{ON(max)} \qquad \text{Eq. 4}$$

$$\text{Hence } R_T = \frac{V_{HV(min)}}{C_T \times \Delta V_{C(max)}} \times t_{ON(max)} \qquad \text{Eq. 5}$$

Taking $C_T = 8.2$ nF we can work out:

$$R_T = \frac{230}{8.2 \times 10^{-9} \times 2} \times 20 \times 10^{-6} = 280\ K\Omega$$

$R_T = 270\ K\Omega$ will be chosen.

OUTPUT BUFFER

During the ON time Pin 8 output current is controlled by means of a series resistor Rs connected between Pin 7 and Pin 8.

The ratio $I_{COLLECTOR} / I_{BASE}$ is constant and is fixed by the value of R_s.
See Fig. 5.

CHOOSING Rs FOR A GIVEN BASE CURRENT

The collector current reaches 3.4 A for maximum output power. (See Chapter Transformer Design).

Let us consider the BU508 HFE of 3. Base current (i.e. Pin 8 current) is related to $V_{pin\,4}$ voltage by the transconductance equation:

$$I_{pin8} = \frac{0.7}{R_s} \times \left(\frac{V_{pin4}}{2} - 1 \right) \qquad \text{Eq. 6}$$

So the forced beta is $I_{Cmax} / I_{pin\,8} = 3$

$$I_{pin\,8} = I_{Cmax} / 3\ A$$
$$= 1.13\ A$$

Choosing Rs = 0.68 Ω the base current will reach at the end of T_{ON} max.

$$I_{pin8} = \frac{0.7}{0.68} \times \left(\frac{4.2}{2} - 1 \right) = 1.13\ A$$

This turning ON current is IB_1. Capacitor C8 inserted in the base path gets charged up during I_{B1}. At the end of this ON period, the energy stored in C8 is related to the voltage appearing on C8.

TURNING OFF ENERGY CALCULATION

Substituting V_{pin4} Eq. 1 into Eq. 6 and solving for I_{pin8} gives:

$$I_{pin8} = \frac{0.35\ V_{HV}\ t_{ON}}{R_S\ R_T\ C_T} - \frac{0.7}{R_S} \qquad \text{Eq. 7}$$

Voltage across C8 can be expressed as:

$$dV_{C8} = \frac{I_{p8}}{C8} \times dt_{ON}$$

Hence

$$dV_{C8} = \frac{0.35\ V_{HV} t_{ON}}{R_S R_T C_T} - \frac{0.7}{R_S}$$

After integration over time we get:

$$V_{C8} = \frac{0.36\ V_{HV}}{2.C8.R_S.R_T.C_T} t^2_{ON} \qquad \text{Eq. 8}$$

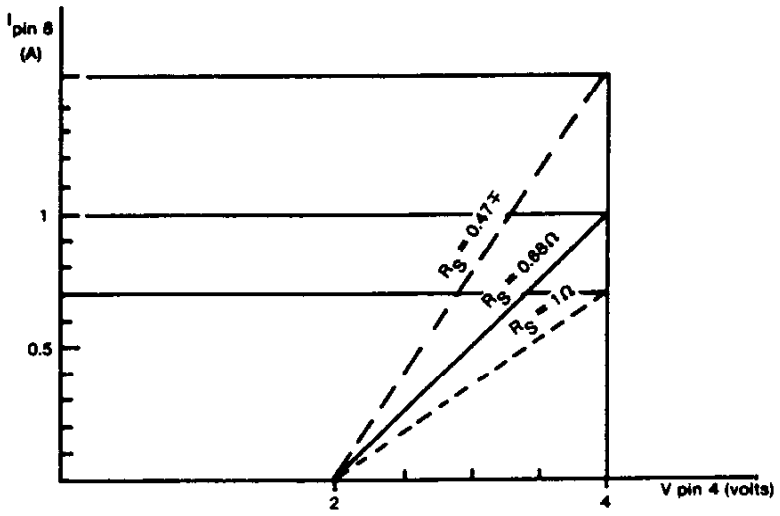
Taking $t_{ON} = 20\ \mu$sec and C8 = 100 μF

$$V_{C8} = \frac{0.35 \times 300\ V}{2 \times 100\ \mu F \times 0.68 \times 270\ K\Omega \times 8\ nF} \times (20\ \mu sec)$$

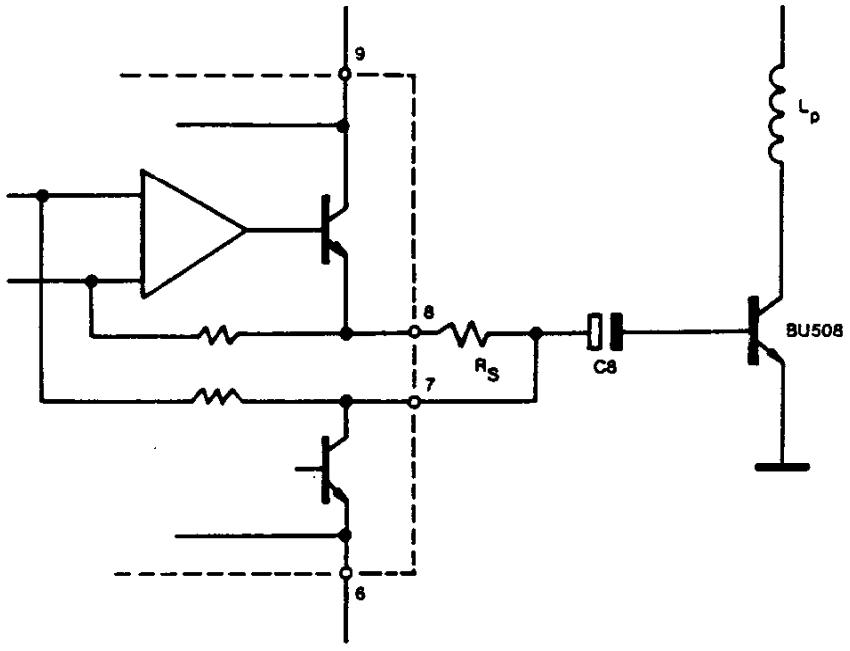
$V_{C8} = 0.14$ V

The available energy stored during t_{ON} in capacitor C8 is:

$W_{C8} = \frac{1}{2}\ C8 \times V^2 C8$



Output Buffer Current Versus R_S



Output Buffer

Figure 5

POWER SWITCH TURNING OFF

When the OFF decision is taken Pin 8 is turned OFF abruptly stopping I_{B1}. Simultaneously Pin 7 turns into a low impedance state. This causes a negative potential on the base of BU508, creating a negative current I_{B2}. This current is not controlled and its value depends on the OFF loop impedance.

NOTE:
In the final application a small value inductance L has been inserted in this loop.

Its effect is to build a delay on I_{B2} in order to synchronise I_c and I_{B2} and optimize the BU508 turning OFF sequence. Typical value for L is 4.7 μH. Figure 6 shows I_{B1} and I_{B2} on the upper trace.

$$W_{OFF} = \frac{1}{2} 100\ \mu F \times (0.14\ v)^2$$
$$= 1\ \mu J$$

A 10 μF would have exhibited

$$\Delta v = 1.4\ V$$

Giving $W_{OFF} = \frac{1}{2} 10\ \mu F \times (1.4\ v)^2$
$W_{OFF} = 10\ \mu J$

Capacitor quality will also impact impedance OFF loop quality. So choosing capacitor C8 is dictated by the required power switch performance.

OPERATING FREQUENCY

The basic equations for the ringing choke architecture are as follows:

- Primary inductor current

$$I_{prim} = \frac{V_{HV}}{L_p} \times t_{ON} \qquad \text{Eq. 9}$$

When turning OFF the stored energy is

$$W_{ON} = \frac{1}{2} L_p I^2_{peak\ max} \qquad \text{Eq. 10}$$

- Secondary inductor current is

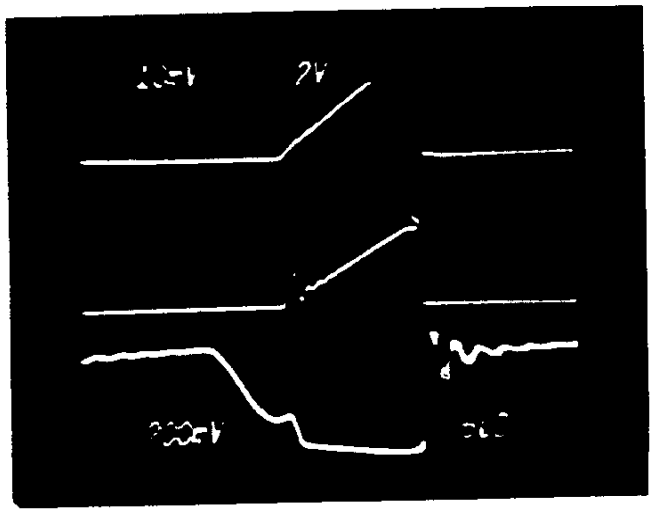
$$I_{second} = I'_{peak\ max} - \frac{V_{OUT}}{L_{second}} \times t_{OFF} \qquad \text{Eq. 11}$$

$$\text{where } I'_{peak\ max} = N I_{prim\ peak\ max} \qquad \text{Eq. 12}$$

$$\text{with } N = \frac{N_{second}}{N_{primary}}$$

It can also be written so that the output voltage appears on the primary side with a factor N.

$$t_{OFF} = \frac{N}{V_{OUT}} \times L_{prim} \times I_{peak\ max}$$



Ib - .5A/div
Ic - 2A/div
Vce - 200V/div

Figure 6

So we can see from Fig. 7 that:

- I_{ON} slope depends on V_{HV} and I_{peak}.
- I_{OFF} slope is constant and equal to $\frac{V'_{OUT}}{L_{prim}}$
- V'_{OUT} is the output voltage seen from the primary side
- f_{min} will be met when I_{peak} is max and V_{HV} min.

If we take into account t_{rise} and t_{fall}, the operating frequency can be written as follows:

$$\frac{1}{f} = \frac{L_p \cdot I_{peak}}{V_{HV}} + \frac{L_p \, I_{peak} \times N}{V_{OUT}} + t_{rise} + t_{fall} \qquad \text{Eq. 13}$$

Refer now to Figure 9.

*t_{rise} is dictated by the collector load at t_{OFF} and by the transistor switching OFF characteristic. The collector load is mainly given by the ringing circuit $L_{leakage}$ and Cp + transformer stray capacitance Cs.

*t_{fall} is also dictated by the collector load and transistor switching OFF time. At that time, the energy has just reached the zero level and the induced voltage collapses with a shape given mainly by the ringing circuit Lp and Cp + Cs. These two phenomena are shown in Figure 10.

To visualize this, the board was put in open loop configuration and a single shot was correctly applied to Pin 2. An auxiliary external V_R voltage was applied to control t_{ON}. See Fig. 8 and Fig. 9.

We can express the V_{CE} fall time as being the half discharge ringing wave.

$$t_{fall} = \tfrac{1}{2}(2\pi \sqrt{L_p \times C_p}) \qquad \text{Eq. 14}$$

$$= \pi \sqrt{1.3 \times 10^{-3} \times 2.2 \times 10^{-9}} = 5.3\ \mu\text{sec}$$

NOTE:

- It is to be noticed that V_{CE} during t_{OFF} is the sum of V_{HV} + V'_{OUT}. Collector voltage during t_{OFF} is approximately twice the input source voltage V_{HV}. This constraint implies using a high voltage power switch.
- The use of C_p is to diminish dV/dt appearing between collector and emitter. Its value depends on the transformer and transistor characteristics:
  - leakage inductance
  - t_s and t_f.

CHOOSING C_p

At zero crossing (see Fig. 9) BU508 collector voltage is equal to V_{HV}. Turning ON would lead to transistor destruction, so a delay R8C7 has been introduced between the auxiliary winding W_{AUX} and Pin 2 - hence diminishing the voltage V_{CE} at turning ON.

So Cp is a compromise between acceptable dV/dt on the collector and the discharge peak current at turning on.

Fig. 11 and 12 show the switching characteristics with two different snubber capacitor values 660 pf and 2200 pf.

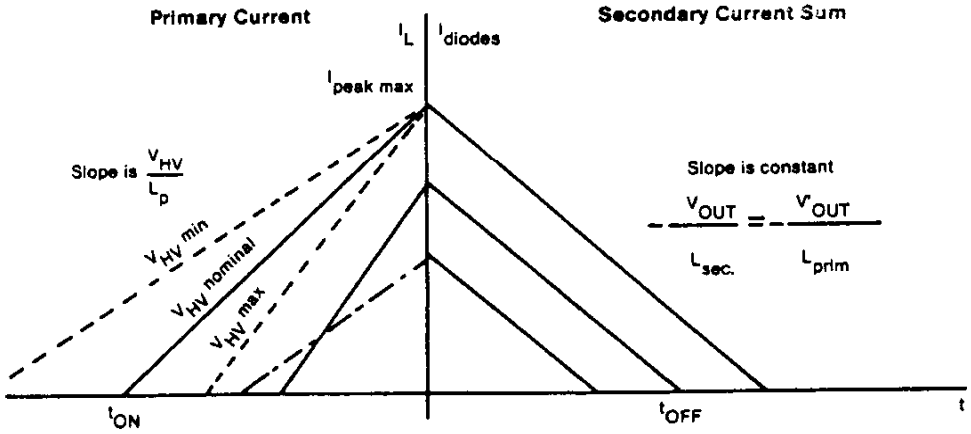


Figure 7

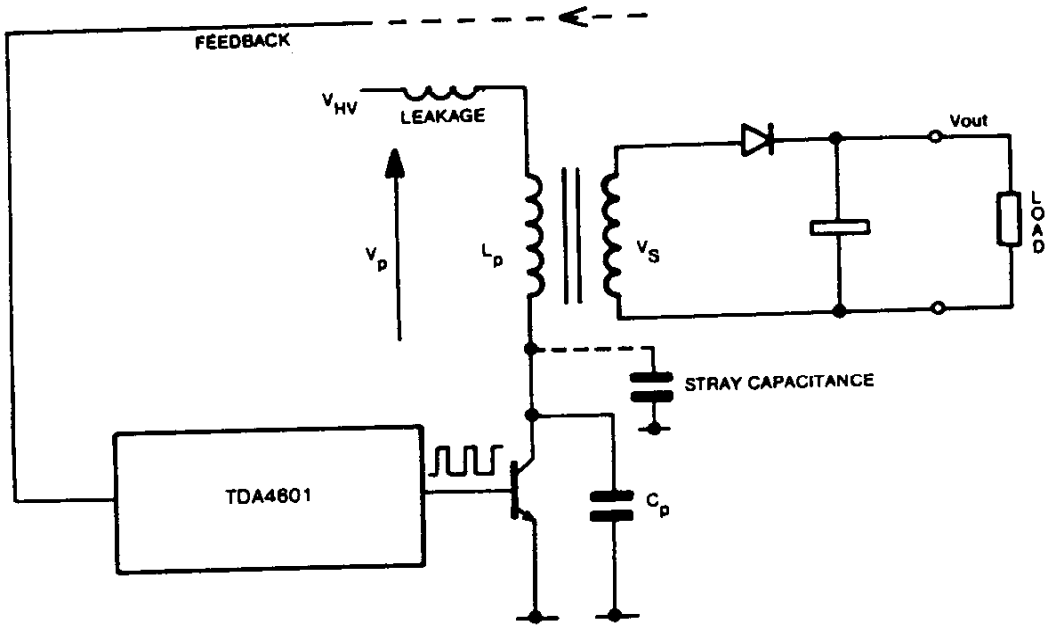


Figure 8

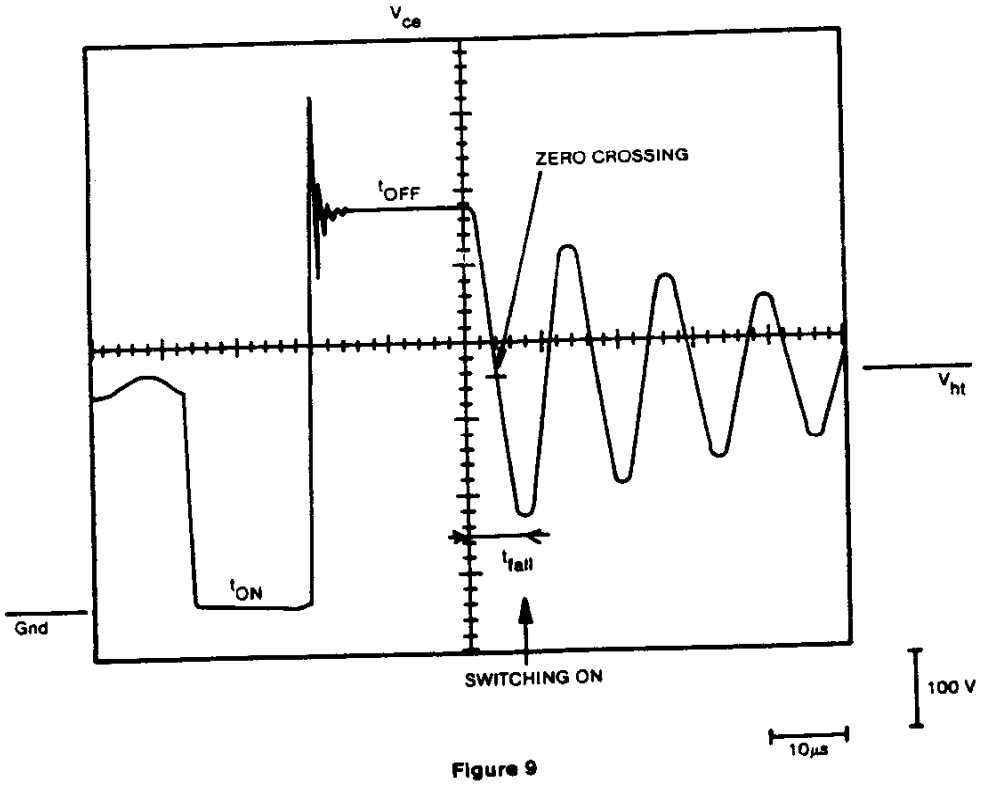
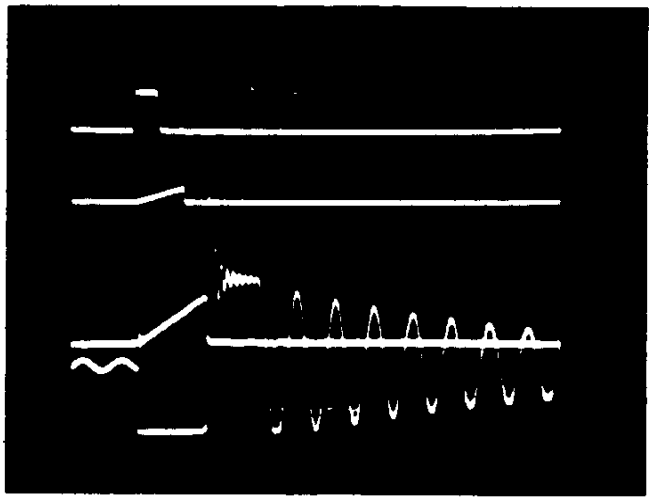


Figure 9

Single shot configuration

$V_{pin\ 9} = 15\ V$

$V_R = -20\ V$



Pin 2 - 0.5V/div

Pin 4 - 5V/div

I_L - 1A/div

V_{CE} - 50V/div

Figure 10

TRANSFORMER DESIGN

System Specifications

$P_{OUT} = 130\ W$
$V_1 = 120\ V/0.78A$
$V_2 = 18\ V/2\ A$

Switching frequency: 20 kHz min

Input source mains line 245 v ac max
185 v ac min

Input-output isolation to the Standard VDE 883

After rectifying and smoothing we get

$V_{HVmin} = 230\ V$
$V_{HVmax} = 375\ V$

Lp and Ipeak Calculation

Assuming an 80% efficiency, the input power becomes

$$P_{in} = \frac{P_{OUT}}{\eta} = \frac{130}{0.8} = 162.5\ \text{Watts} \qquad \text{Eq. 15}$$

Corresponding energy per switching cycle is

$$W = P_{in} \times T = 162.5 \times 50\ \mu\text{sec} = 8.125\ \text{mJ} \qquad \text{Eq. 16}$$

This energy has to be stored during the ON time.

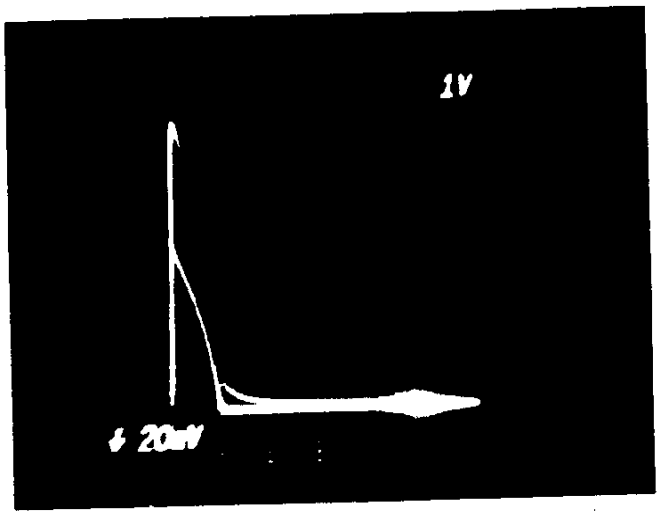
The switching sequence is depicted on Figure 9.

t_{ON} primary loading energy
t_{OFF} energy is dumped to the load
t_{fall} can be considered as dead time

Timing assumption

Duty cycle max for minimum mains: $\delta = 0.5$

$$\text{So } t_{ONmax} = \frac{T - t_{fall}}{2} = \frac{50\ \mu\text{sec} - 5\ \mu\text{sec}}{2} = 20\ \mu\text{sec} \qquad \text{Eq. 17}$$

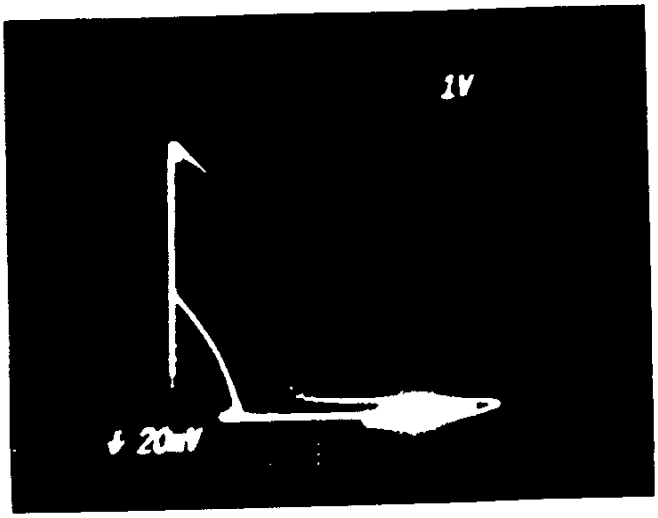


C_p = 2200 pf

0.2A/div

100V/div

Figure 11



C_p = 660 pf

Figure 12

BU508 LOAD LINE

240 ~ ac/50 W

Substituting Eq. 9 into Eq. 10 and solving for Lp

$$Lp = \frac{(V_{HV} \times t_{on})^2}{2W_{ON}} \qquad \text{Eq. 18}$$

$$Lp = \frac{(230 \times 20 \times 10^{-6})^2}{2 \times 8.125 \times 10^{-3}} = 1.3 \text{ mH}$$

Using equation 9 with max. duty cycle and minimum ac main

$$I_{peakmax} = \frac{230 \times 20 \times 10^{-6}}{1.3 \times 10^{-3}} = 3.5 \text{ A}$$

From the manufacturer's catalog* the core that meets the output power requirements is the GER 41 x 21 x 20 in B50 material.

Having chosen the core size and the material, the minimum primary turns number can be determined from

$$Np = \frac{Lp \times I_{peak\ max}}{Ae\ B_{max}} (10^8) \qquad \text{Eq. 19}$$

where Np: primary turns
Lp: primary inductance (H)
Ae: effective core area (cm^2)
Bmax: saturation flux density (Gauss)

Hence

$$Np = \frac{1.3 \text{ mH} \times 3.5 \text{ A}}{2.33 \text{ cm}^2 \times 3200 \text{ G}}$$

$$= 61 \text{ turns}$$

Since 5 A/mm^2 (3225A/in^2) is chosen to be the maximum wire current density d for this design the primary winding requires a wire whose size is:

$$I_{primary\ average} = \frac{I_{peak\ max} \times \delta\ max}{2} = \frac{3.5A \times 0.5}{2} = 0.875 \text{ A}$$

$$\text{Selection: } \frac{0.875}{5} = .175 \text{ mm}^2 \quad \text{Wire size: } 2\sqrt{\frac{175}{\pi}} = 0.48 \text{ mm}$$

This size from the magnet wire specifications correspond to No. 26 AWG. In order to get 2 complete layers of 30 turns each, No. 21 AWG was chosen.

Since the core size has to be chosen as small as possible, the core must be gapped to a length lg given by:

$$lg = \frac{(0.4\pi\ Lp\ I_{peak\ max})\ 10^8}{Ae\ B^2_{max}} \qquad \text{Eq. 20}$$

$$= \frac{(0.4\pi \times 1.3 \text{ mH} \times 3.5A^2) \times 10^8}{2.33 \times 3200} = 8.10^{-2}$$

$$= 0.8 \text{ mm}$$

Secondary number of turns if bound to the primary number of turns by Eq.

$$N_S = \frac{Np \times (V_{OUT} + V_D)\ (1 - \delta\ max)}{V_{in}\ min \times \delta\ max} \qquad \text{Eq. 21}$$

It can be assumed that V_D is low compared to 120 V. So for 120 V output voltage, we get:

$$N_{120} = \frac{61 \times 120\ (1 - 0.5)}{230 \times 0.5}$$

$$N_{120} = 32 \text{ turns}$$

A single-stranded wire can be used.

The size is given by:

$$\text{Section: } \frac{I_{120\ av}}{d} = \frac{0.78A}{5A/mm^2} = 0.156 \text{ mm}^2 \qquad D_{120V} = 0.44 \text{ mm}$$

Which corresponds to wire gauge No. 26 AWG. Again to get one complete layer No. 21 AWG was also chosen.

In the same way the 18 volts secondary winding can be calculated:

$$N_{18} = \frac{61\ (18 + 0.7)\ (1 - 0.5)}{230 \times 0.5)} = 4.96$$

$$N_{18} = 5 \text{ turns}$$

In order to improve coupling factor each of the 5 turns should be built with two-strands wire.

So maximum current density in each wire is chosen current density of $5A/mm^2$ divided by two.

Average current in winding 18 V is: 2 A. In each wire 1 A will flow.

Winding 18 V wire size is:

$$\frac{I_{18\ ac}}{d} = \frac{1A}{5A/mm^2} = 0.2 \text{ mm}^2 \qquad D_{18V} = 0.50 \text{ mm}$$

So chosen wire gauge No. 21 AWG will be sufficient to withstand the current in the 18 V winding.

*LCC Ferrites Doux "Ferrinox ®"

Using the same method the auxiliary winding can be calculated.

In the application V_R was chosen to be −20 V when working in normal regulation mode.

So we can write:

$$N_{AUX} = \frac{61\ (20 + 0.6)\ (1 - 0.5)}{230 \times 0.5} = 5.46$$

$$N_{AUX} = 6 \text{ turns}$$

No power is required from this winding, thus any wire gauge number will fit. The same wire gauge as primary winding was chosen i.e. No. 21 AWG.

Calculating the self supply winding requires a different approach because this winding delivers energy during the ON time. The following equation is used:

$$\frac{N_{primary}}{N_{self\ sup}} = \frac{V_{HV}\ min}{V_{pin\ 9}} \qquad \text{Eq. 22}$$

Solving for $V_{pin\ 9} = 15$ V yields

$$N_{self\ sup} = 61 \times \frac{15}{230} = 3.97$$

$$N_{self\ sup} = 4 \text{ turns}$$

Wire size has been chosen to be No. 21 AWG.

To verify the number of turns for the bobbin, the following equation is used:

$$A_B \geqslant \frac{Np}{T_{21}} + \frac{Nss}{T_{21}} + \frac{Naux}{T_{21}} + \frac{N_{120}}{T_{21}} + \frac{N_{18}}{T_{21}} \qquad \text{Eq. 23}$$

with T_{21} being the number of turns per square inch for No. 21 AWG.

$$A_B \geqslant \frac{61 + 4 + 6 + 32 + 5}{1014} = 0.106 \text{ inch}^2$$

From the core catalog $A_B = .75 \text{ cm}^2$

$$\frac{1.75 \text{ cm}^2}{2.54^2} = 0.27 \geqslant 0.106 \text{ inch}^2$$

In order to meet Standard VDE 883 a shield must be added. A 4 mm space between bobbin and wire has also to be allowed.

So the calculated fit which seems too large for the design is in fact properly specified.

The complete transformer specification is represented in Table 1.

TABLE 1

Transformer Specification

Core E Shape GER 42 x 21 x 20 from L.C.C. Thomson Bobbin CAR 4420A Air Gap: 0.8 mm		
Primary	W_p	61 turns # 21 AWG ϕ 0.75 mm
Shield		Copper band 0.1 mm width
Self Supply	W_{ss}	4 turns # 21 AWG ϕ 0.75 mm
Auxiliary	W_{aux}	6 turns # 21 AWG ϕ 0.75 mm
Output 120 V	W_{120}	32 turns # 21 AWG ϕ 0.75 mm
Output 18 V	W_{18}	5 turns # 21 AWG ϕ 0.75 mm
Shield		Copper band 0.1 mm width

Insulation between every layer 0.1 mm Mylar

Core Specification

Material	Ferrinox B50
A_l (mH)	6500
μAv	2000
B_{max} @ 100°C (Gauss)	>3200
A_e (cm²)	2,33
A_{CB} (cm²)	1,75
l_m (cm)	10

START UP SEQUENCE

The Pin 9 of TDA4601 is fed by two different sources. See Fig. 13

The *first one* is produced by the mains line through one diode 1N4007 and one 10K/3W resistor. Smoothing is achieved by a 100 μF electrolytic capacitor.

The *second one* comes from an extra winding W_{ss} which will deliver energy when the SMPS has started up.

The start-up current delivered to Pin 9 can be written as follows:

$$V_{av} = (i_{startup} \times R_{STUP}) + V_{9STUP} \qquad \text{Eq. 24}$$

$$V_{av} = \frac{V_{acpk}}{\pi}$$

The start-up threshold voltage is 12.5 V.
The voltage/current characteristic at Pin 9 is:

$V_9 = 2\ V \rightarrow I_9 = 0.5\ mA$
$V_9 = 5\ V \rightarrow I_9 = 1.5\ mA$
$V_9 = 10\ V \rightarrow I_9 = 2.4\ mA$

A rough approximation of I_9 before start-up gives 1 mA.

$$I_{STUP} = \frac{V_{acpk}}{\pi \times R_{STUP}} \qquad \text{Eq. 24}$$

The current equation on Pin 9 gives:

$$\frac{C_9 \times V_{STUP}}{T_{STUP}} = I_{C9} - I_{STUP}\ I_{gSTUP} \qquad \text{Eq. 25}$$

Substituting Eq. 24 into Eq. 25 and solving for R_{STUP}

$$R_{STUP} = \frac{V_{RMS}\sqrt{2}}{\pi} \times \frac{1}{\frac{C9 \times V_{STUP}}{T_{STUP}} + I_{gSTUP}} \qquad \text{Eq. 26}$$

Solving for $V_{mains} = 220$ vac $C9 = 100\mu F$
$T_{STUP} = 0.15$ sec.

$$R_{STUP} = \frac{220\sqrt{2}}{\pi} \times \frac{1}{\frac{100 \times 10^{-6} \times 12.5}{0.15} + 1 \times 10^{-3}} = 10.6\ K\Omega$$

Used value $R_{START\ UP} = 10\ K\Omega$

Power dissipated in R_{stup} is:

$$P_{STUP} = \frac{V^2av}{R_{STUP}} = \frac{(100\ V)^2}{10\ K\Omega} = 1\ Watt$$

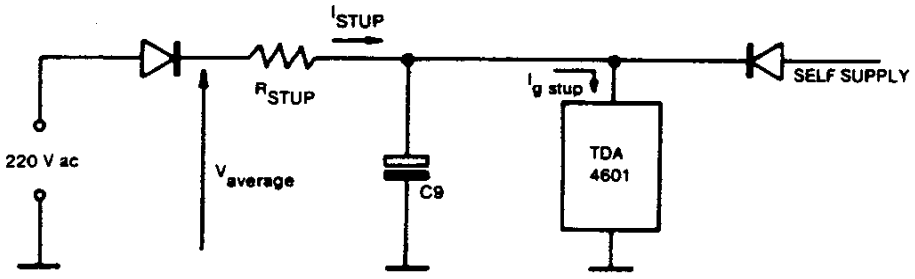


Figure 13

Regulation and Overload Thru VPIN 3

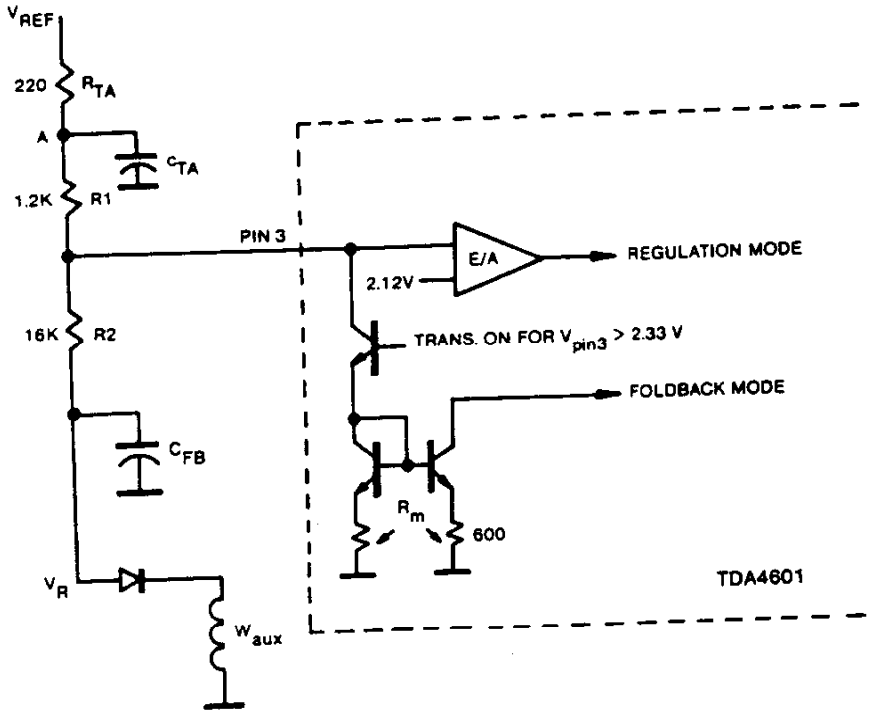


Figure 14

- Regulation $V_3 = \left[(V_A - V_R) \times \frac{R2}{R1 + R2}\right] + V_R < 2.33$ volts

- Overload V3 > 2.33 V

$$I_{pin\ 3} = \frac{V3 - V_{be}}{R_m} \qquad \text{Eq. 27}$$

Summing the currents at Pin 3, we can show that:

$$V_{pin\ 3} = V_3 = R1//R2//R_m \times \left(\frac{V_{REF}}{R1} + \frac{V_R}{R2} + \frac{V_{be}}{R_m}\right) \qquad \text{Eq.28}$$

with $R_m = 600\Omega$

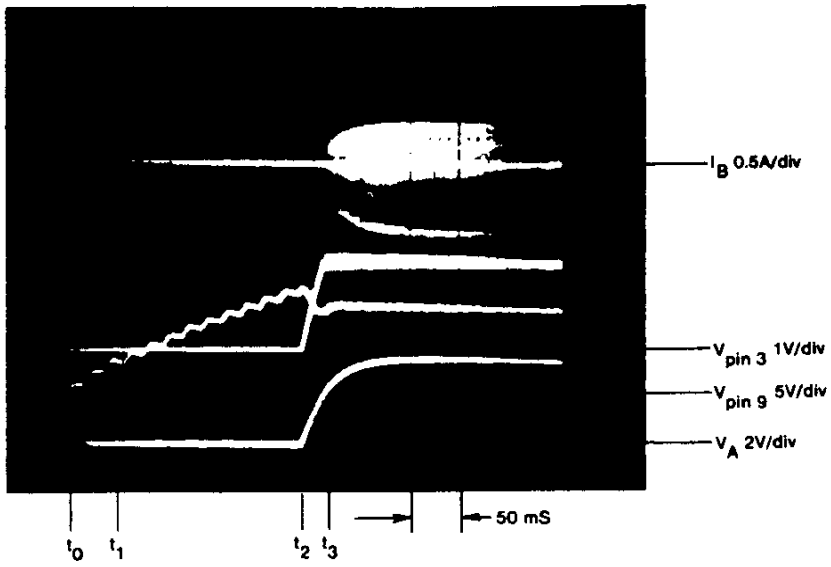


Figure 15

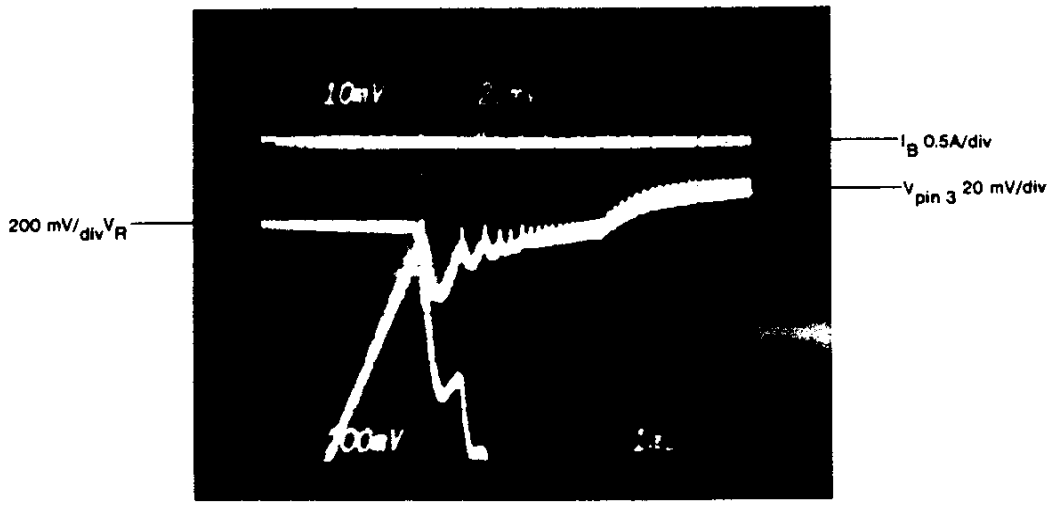


Figure 16

Refer to Figure 15.

t0 - MAINS VOLTAGE IS APPLIED

V9 (VPIN9) increases slowly according to the time constant of equation 25.

t1 - V9 REACHES 4 V

- A $2V_{be}$ internal voltage reference is established.
- Capacitor C7 begins charging up to $2\,V_{be}$. This capacitor pre-charge will prepare the first BU508 switching ON.
- The band-gap reference is enabled.

t2 - V0 REACHES 12.5 V

- The internal V_{REF} of 4.2 is distributed to every functional block. The IC is ready to start.
- V_{return} = 0 V as long as no pulse is delivered to the power switch.
- $V_{pin\ 3}$ is V3 = 0 V.
- Due to capacitor C_T, the A voltage V_A (see Fig. 14) increases exponentially at a rate depending on $R_{TA}C_{TA}$.
- The voltage appearing on Pin 3 is a proportion of V_A.
- As long as V3 is less than 2.12 V, (see Fig. 17) no pulse appears on Pin 4.

t3 - V3 REACHES 2.12 V

- The first pulse appears on Pin 4. The output stage converts this triangular voltage pulse into a proportional current pulse through the base emitter junction of the BU508. The corresponding energy is stored in W_p and finally dumped to all secondary windings and also to the auxiliary feedback winding.
- During the ON time, winding W_{ss} working in the *forward mode* begins delivering energy to capacitor C9 via D9.
- Return voltage begins increasing. V_R is a negative voltage relative to ground.

Now V_A is ramping up and
V_R is ramping down.
Fig. 16 magnifies this soft-start sequence.

The ringing appearing in this sequence is directly related to:

- V_R path time constant
- Secondary power level
- Coupling between W_{aux} and each secondary winding.

OVERLOAD MODE

Maximum power delivered by this SMPS is obtained when the sawtooth on Pin 4 reaches 4.2 V.

An internal clamping circuit prevents $V_{pin\ 4}$ from exceeding V_{REF}.

- At that moment if the output power demand still increases, the regulation process cannot react any more and the output voltage falls down.
  This decay is proportionally reflected to V_R.
- V3 increases.
- When V3 reaches 2.33 V, Pin 3 becomes the low resistance input of the overload circuitry. (See Figure 14).
- V3 becomes less than 2.12 V and thus disabling the E/A.

The overload sawtooth characteristic is linear. Sawtooth size is now specified by current i_3 flowing into Pin 3 through the external resistor divider.
Resistor R1 and R2 therefore have two roles:

1) *Regulation Mode*
   Ratio R1/R2 sets the SMPS steady state.
2) *Overload mode*
   R1 and R2 according to equation 28 set Pin 3 current level as a function of V_R.

These two roles are depicted on Fig. 17 (Pin 3 characteristic). The overload mode exhibits a linear foldback characteristic. Fig. 19.

OVERLOAD MODE LIMIT

The limit is reached when V_R exhibits a level which pulls down V3 to 2.12 V. Using equations 27 and 28 and replacing V3 by 2.12 V, we get:

$V_R = -16V$
$i_3 = 2.4\ mA$

This can be seen on Figure 18 in which there is no capacitor C_T. As long as V_R does not reach -16 V, the base current remains at low level dictated by equation 28 and C_{FB} is charged slowly.

STANDY-BY MODE

When the TV set is switched OFF by remote control, the power supply is still running in order to be ready to restart when receiving the remote control order "ON".

During this stand-by mode, the SMPS has to consume a power as low as possible. Figure 20 shows this mode.

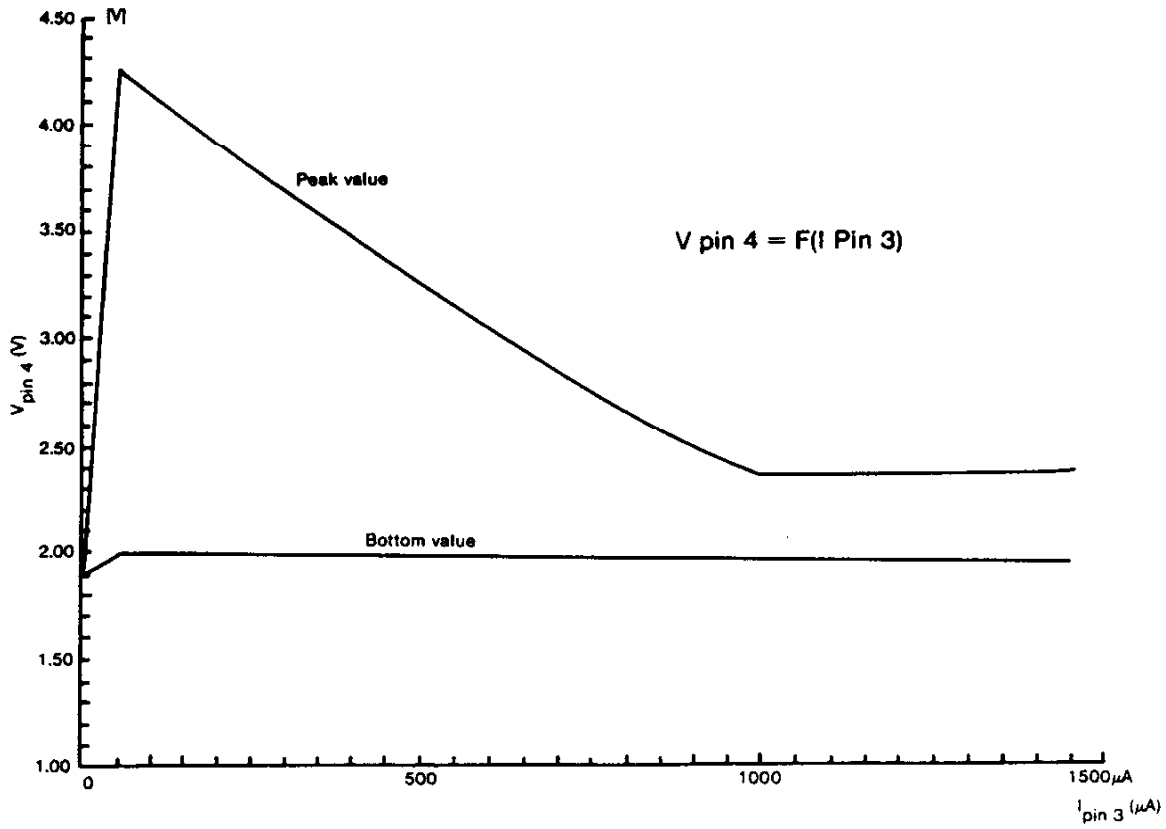
Pin 4 delivers very small sawtooth pulses.

The power transistor leaves the saturation mode and works in the linear mode, i.e. current and voltage appear simultaneously, heating up the transistor.

In order to minimize this power loss the modulator has to be very sensitive even at low levels.

The role of the ceramic capacitor between pin 2 and pin 3 is to disturb for a very short time the steady-state equilibrium thus eliminating any hazardous modulator decision and slightly improving the overall stability.

With only 3 Watts on the output, switching frequency is fully determined by the natural time constants of the external components. The SMPS is more like a free oscillator than a real switchmode.


M
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
Peak value
Bottom value
V pin 4 = F(I Pin 3)
$V_{pin\ 4}$ (V)
0
500
1000
1500μA
$I_{pin\ 3}$ (μA)

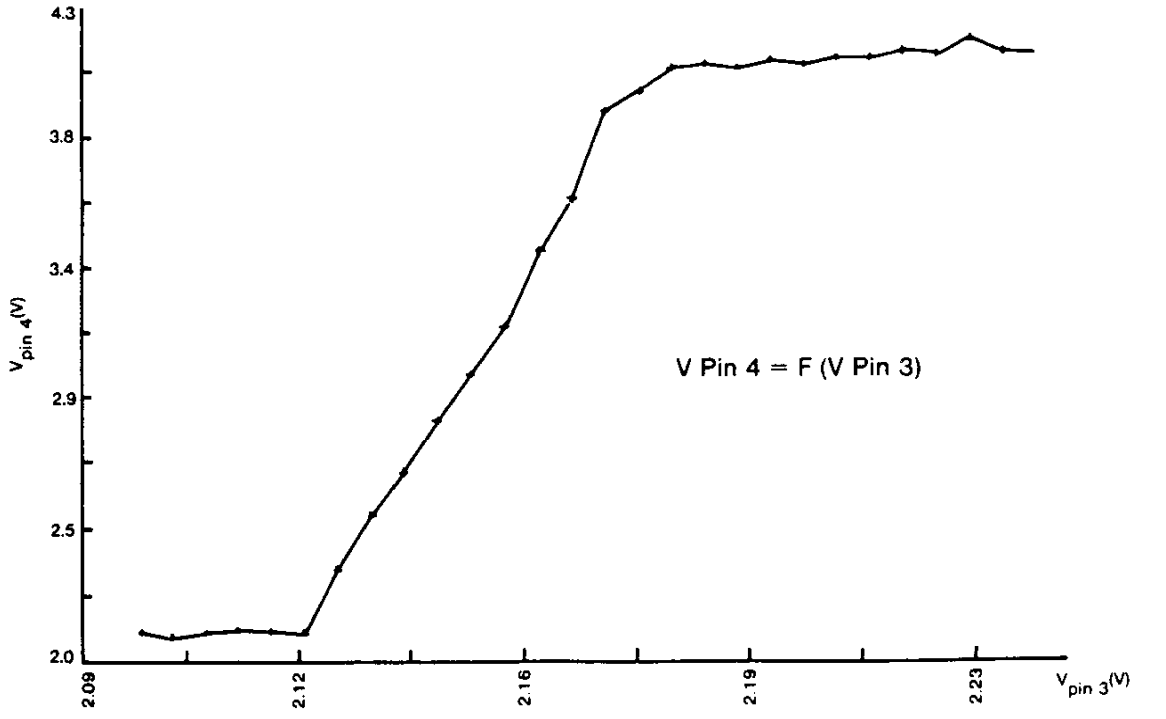

4.3
3.8
3.4
2.9
2.5
2.0
V Pin 4 = F (V Pin 3)
$V_{pin\ 4}$(V)
2.09
2.12
2.16
2.19
2.23
$V_{pin\ 3}$(V)

Figure 17

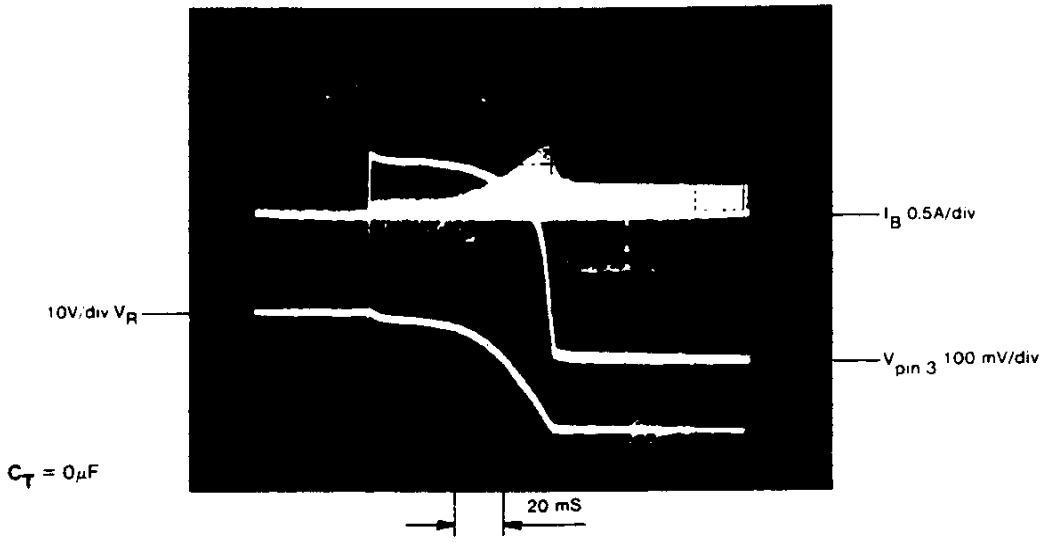
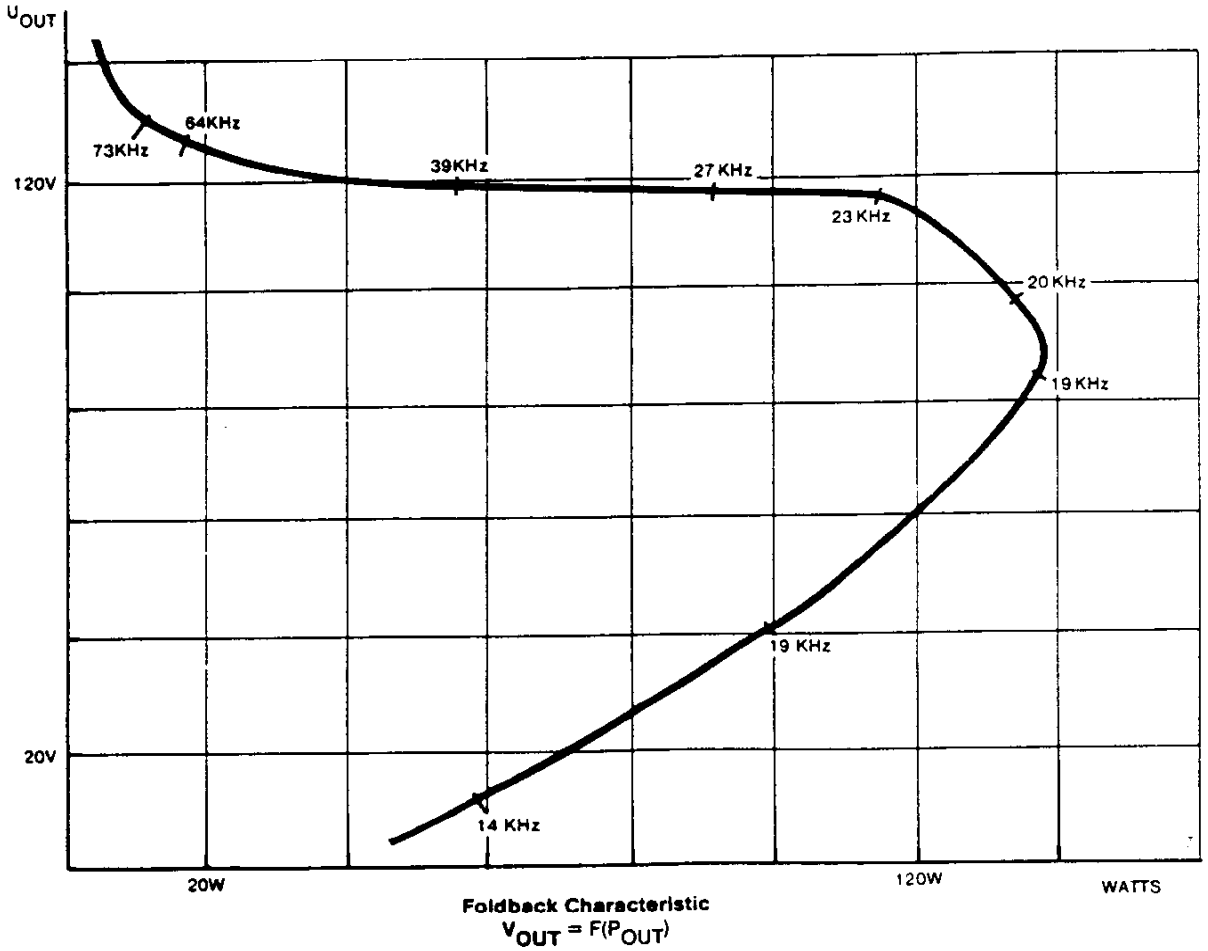


Figure 18



Foldback Characteristic
$V_{OUT} = F(P_{OUT})$

Figure 19

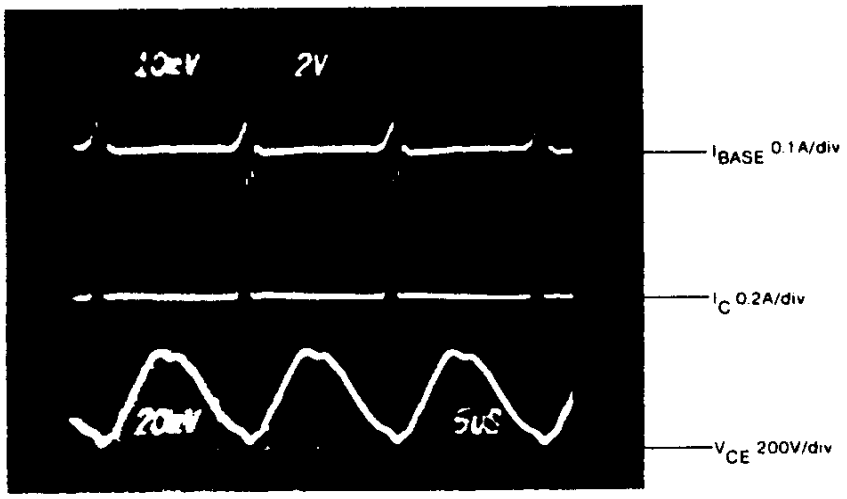


Figure 20

Performance

Line Regulation	185 V~ to 245 V~ P = 60 W ΔVout = 2 V on 120 V
Load regulation	220 V~ ΔP = 60W/120W ΔVout = 0.5 V on 120 V
Frequency full load	20 KHz
stand-by (3 W)	70 KHz
Output ripple	0.3 V on 120 V output
Efficiency	P = 120 W η = 80%

CONCLUSION

The described power supply was primarily designed for TV set application. Any other application could be realized using the TDA4601.

The feedback loop can be improved using an opto coupler working simultaneously with an auxiliary winding. In this improved configuration the output voltage precision becomes dependant on the feedback loop only.

REFERENCES

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3 George Chryssis High Frequency switching power supplies McGraw-Hill Book Company.