



ULTRAFAST RECOVERY RECTIFIERS EXTEND POWER TRANSISTOR SOA

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Traditionally, bipolar power transistors have been limited to collector-emitter breakdown ($V_{(BR)CEO(sus)}$) ratings at turn-on. Since $V_{(BR)CEO(sus)}$ is typically only half the bulk breakdown rating $V_{(BR)CBO}$, this limitation can have a strong influence on power conversion equipment design. However, new developments are changing the rules. Test results indicate that the sub 100 ns recovery times of today's ULTRAFAST recovery rectifiers can be used to eliminate the $V_{(BR)CEO}$ limitation. Using ULTRAFAST clamp diodes, third generation bipolars have switched rated current from bus voltages up to bulk breakdown. This ability can have a profound influence upon power conversion efficiency, cost, and the relative merits of bipolars versus other types of power semiconductors.

The purpose here is to examine the improvement in turn-on safe operating area that can be realized with ULTRAFAST clamp diodes. In order to provide a com-

plete analysis, the ULTRAFAST results are preceded with a review of conventional design rules.

CONVENTIONAL DESIGN RULES

Modern power transistors are generally specified for both forward bias safe operating area (FBSOA) and reverse bias safe operating area (RBSOA). In switchmode power conversion systems, allowable stress at turn-on is defined by a 5 to 10 μ s pulsed FBSOA curve. Safe operation is dependent upon keeping the turn-on load line within this boundary. Similarly, safe operating at turn-off depends upon the turn-off load line remaining within the boundaries of the RBSOA curve. These two curves are drawn on the same scale for the MJH16008 Switchmode III transistor in Figure 1. Note that the ability to withstand voltage at turn-off is limited by $V_{(BR)CBO}$ and is roughly twice the $V_{(BR)CEO(sus)}$ limitation that defines the maximum turn-on excursion.

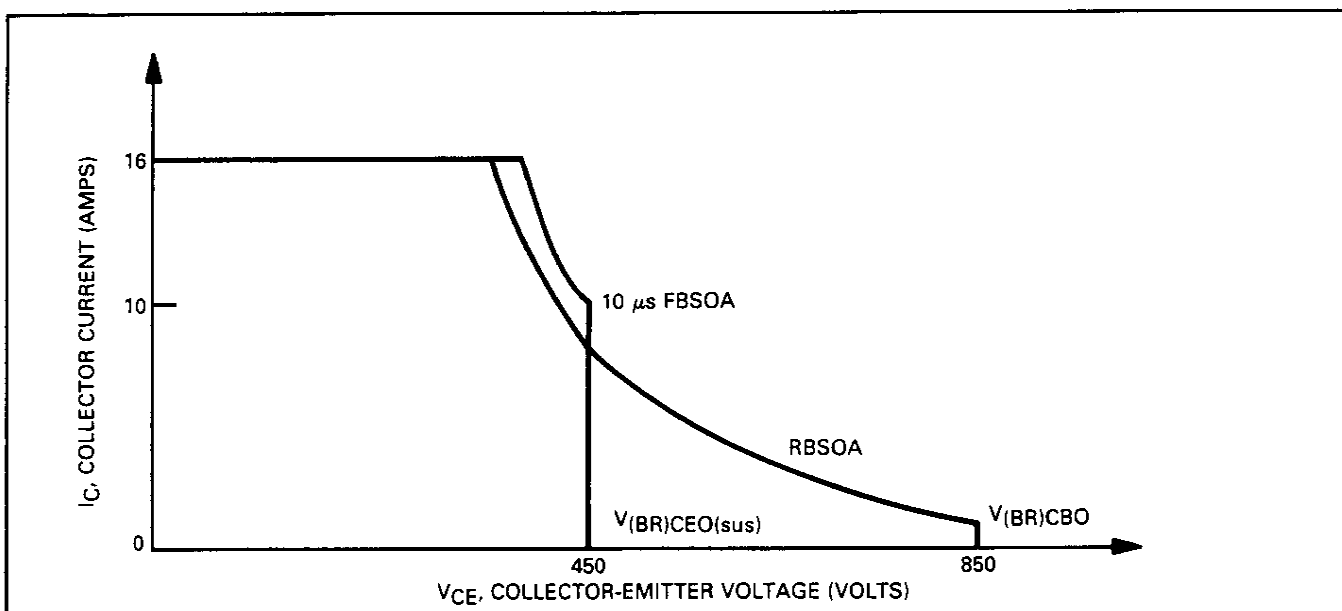


FIGURE 1 — Safe Operating Area

The reason for the difference is related to gain. At turn-off, reverse base current can reduce the transistor's gain below unity, enabling the bipolar structure to block its full collector-base breakdown voltage. Conversely, at turn-on, gain limits the transistor's voltage sustaining ability to $V_{(BR)CEO(sus)}$.

It is helpful to think of the difference in terms of the $V_{(BR)CEO}$ snapback phenomena that is readily seen on a curve tracer. An example is reproduced in Figure 2.

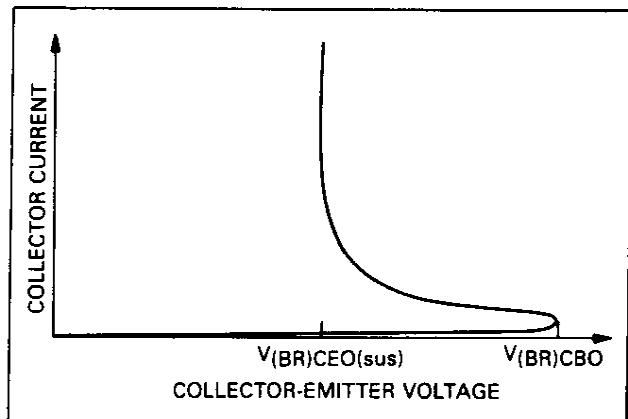


FIGURE 2 — $V_{(BR)CEO}$ Snapback

At currents so low that gain is less than unity, the blocking voltage can extend to bulk breakdown. However, as the transistor is driven into breakdown, collector current increases. When collector current increases sufficiently for gain to climb above unity, the voltage breakdown begins to decrease until $V_{(BR)CEO(sus)}$ is reached. Sustained operation above $V_{(BR)CEO(sus)}$ at any appreciable current is not feasible, due to the breakdown limitation. Therefore, the maximum voltage limit for FBSOA curves in general, and turn-on load lines in particular, is $V_{(BR)CEO(sus)}$.

A NEW HYPOTHESIS

The ability of power MOSFETs to switch turn-on load lines up to bulk breakdown $V_{(BR)DSS}$ is one of the FET's strong suits. It is also a characteristic that encouraged the percolation of some interesting thoughts. Given the FET's abilities, there must be no fundamental limitation which precludes a power transistor from turning-on into its full bulk breakdown voltage.

One can speculate further, and reason that the bipolar's sustaining voltage limitation might be of little consequence if the turn-on transition occurs rapidly enough. Once turned-on, the ability of the transistor to sustain a voltage above $V_{(BR)CEO(sus)}$ is of little importance, since the objective is to reduce the collector voltage as rapidly as possible. The only real concern is safe area.

In this regard, suppose that the turn-on transition can be accomplished in a few tens of nano seconds. At this speed, perhaps the hotspotting phenomena that would otherwise cause the transistor's destruction, does not have time to develop. Presumably, it takes time for one portion of the die to become hotter than its surroundings, and by that time, a sub 100 ns turn-on transition is probably long over. Without hotspotting, the bipolar could have considerably more capability than is generally per-

ceived. In fact, turn-on SOA up to collector-base breakdown is a possibility.

A few years ago, such a hypothesis might have been just an idle speculation. However, with today's ULTRAFAST recovery rectifiers and third generation bipolars, sub 100 ns turn-on transitions can easily be achieved. In fact, a very simple circuit using the MUR8100 (8.0 Amp, 1000 Volt) ULTRAFAST recovery rectifier was built to test the hypothesis. It is shown in Figure 3.

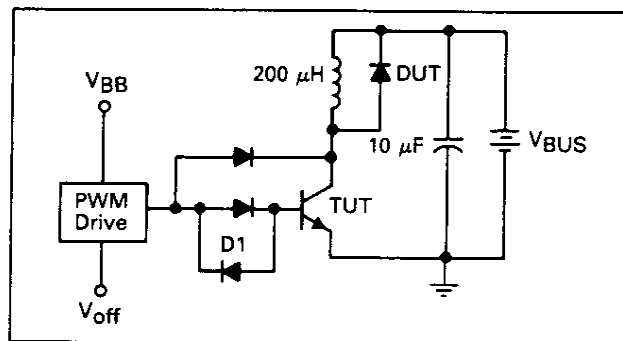


FIGURE 3 — Test Circuit

The test results that have been obtained with this circuit tend to validate the hypothesis. They are described as follows.

TEST RESULTS

For testing purposes, a trapezoidal collector current waveform typical of a switching power supply was used. Pulse width and duty cycle were adjusted for 5.0 amps of peak current at turn-off. No attempt was made to control peak turn-on current. In the circuit of Figure 3 the turn-on spike is a function of the freewheeling diode's reverse recovery characteristics and the transistor's rise time. The resulting waveform appears in Figure 4. Note that the peak turn-on current exceeds 10 Amps.

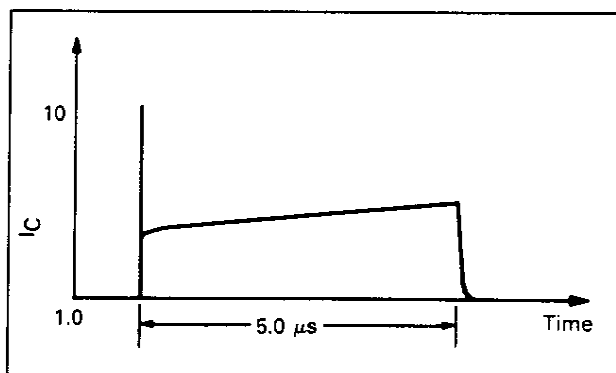


FIGURE 4 — Collector Current Waveform

An expanded view of the turn-on spike appears in Figure 5. This photo shows the kind of turn-on times that are achievable using an MJ16008 third generation power transistor and an MUR8100 ULTRAFAST diode. At 40 ns, the turn-on crossover time is probably more typical of what is expected from power MOSFETs than the usual performance from bipolars. From an SOA point of view, the key parameter is voltage fall time. The more rapidly the voltage falls, the more quickly SOA stress is removed

from the transistor. The 25 ns voltage fall time that is shown is probably the key factor in determining the excellent SOA results that follow.

At the other end of the trapezoidal current waveform, 5.0 Amps is switched through voltages up to bulk breakdown. Therefore, surviving the turn-off transition requires quite a substantial RBSOA capability. This requirement narrows the possibilities to third generation bipolars.

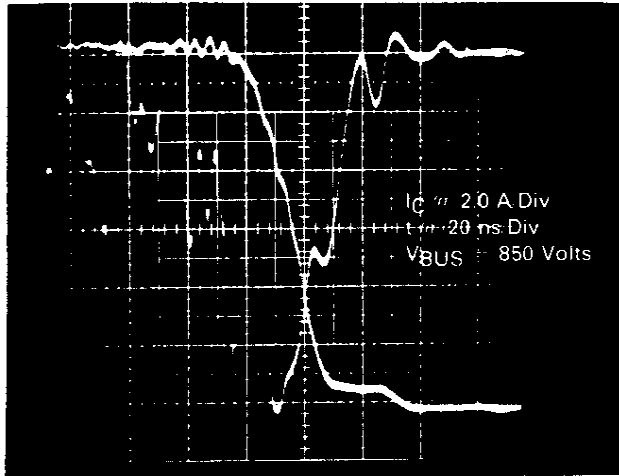


FIGURE 5 — Turn-On Transition

Most of the testing was performed with the MJ16008 Switchmode III transistor. Supplemental information was obtained by using MJ16004 and MJ16016 devices from the same family. Ratings for these transistors are summarized in Table 1. They are needed for comparison with the test results that follow.

TABLE 1. TRANSISTOR RATINGS

Transistor	$I_C(\text{Max})$ (Amps)	$V_{(BR)CEO(sus)}$ (Volts)	$V_{(BR)CBO}$ Volts
MJ16004	5.0	450	850
MJ16008	8.0	450	850
MJ16016	20	450	850

Compared to these ratings, the SOA performance that was measured with the MUR8100 freewheeling diode is quite impressive. The MJ16008 comfortably switched the 5.0 Amp trapezoidal waveform from an 850 volt bus. Considering the 12 Amp clearing current spike, this is quite a feat for an 8.0 A/450 volt transistor. Even more surprising, the smaller MJ16004 does equally as well, passing the 850 volt/5.0 Amp condition with no failures.

A similar test was run on the MJ16016 at double the collector current (10 Amps). The results indicate that the SOA capability does not scale linearly with silicon area. The MJ16016, which contains two MJ16008 die that come from adjacent locations on a wafer, came close but did not quite achieve 10 Amps at 850 volts. Although every device tested exceeded 9.0 Amps at 850 volts, yield to the 10 A/850 volt condition was only 55%. A brief summary of the test results for all three transistors appears in Table 2. These results are based upon a total sample population of 37 devices taken from at least 5 different wafer lots.

TABLE 2. TEST RESULTS SUMMARY

Transistor	Survival to 850 V/2.5 A	Survival to 850 V/5.0 A	Survival to 850 V/10 A
MJ16004	100%	100%	N/A
MJ16008	100%	100%	N/A
MJ16016	100%	100%	55%

The test results in Table 2 are exciting news. They indicate that the ULTRAFast rectifier adds new freedom to bipolar power stage design. However, it is also very desirable to know how much safety margin there is operating at the $V_{(BR)CBO}$ limit. Four indications of safety margin were considered.

1. Bus voltage was raised up to the 1000 volts max imposed by equipment limitations. Of seventeen units that were tested, only 3 failed to reach the 1000 volt limit. The three that did not reach 1000 volts failed at an average of 985 volts. This is quite a respectable safety factor based upon the 850 volt specified $V_{(BR)CBO}$.

2. A measure of safety margin was made by decreasing the base drive compliance voltage (V_{BB} in Figure 3). Since power transistors are sensitive to base drive compliance voltages below 10 volts, reducing this voltage is one way to measure relative stress. Perhaps a few words of explanation are in order.

As a general rule, the fastest drive circuit, when operated from less than a 10 volt source, will provide a base drive pulse which has a slower rise time than the output collector current. This is a very stressful situation for the transistor. With collector current rising faster than base current, there is not enough bias to adequately spread collector current across the emitter fingers. Consequently, current flow is restricted to the edges of the fingers, and dissipation is confined to a relatively small area. As a result, the transistor's power handling ability is greatly reduced.

In circuits that clear standard recovery diodes, it is not unusual for a 5.0 volt base drive compliance to kill bipolars at bus voltages above 75% of $V_{(BR)CEO(sus)}$. Accordingly, a measure of safety margin can be made by reducing V_{BB} from the 25 volts that was used for the bulk of the testing to 10 volts and finally to 5.0 volts.

The results are again very favorable. At 10 volts compliance, 100% of the test devices survived the 850 volt/5.0 Amp condition. When the test was repeated at 5.0 volts, the same results were obtained. 100% of the test devices survived 850 volts/5.0 Amps. The implication here is that even at 850 volts, turning on into the ULTRAFast diode, the Switchmode III transistor is loafing.

3. A measure of safety margin was made by substituting slower diodes for the MUR8100. Again, the results are very favorable. The 200 ns MR826 produced no failures to the 850 volt/5.0 Amp condition when the transistors were driven from a base drive compliance above 10 volts. When the compliance voltage was reduced to 5.0 volts, half the test devices failed. These results show that the ULTRAFast diode really does make a difference while, at the same time, indicating that the ULTRAFast diode is fast enough to protect the transistor with a considerable margin.

4. Life test results are also a very good indication of how safe an applied stress is. To get a handle on this aspect, the life test fixture that is outlined in Figure 6 was constructed. This fixture sequences 4 output devices to run at a combined frequency of 20 kHz. In the process, the three transistors which are off in any given cycle are subject to the same type of dV/dt stress that would be experienced in a bridge.

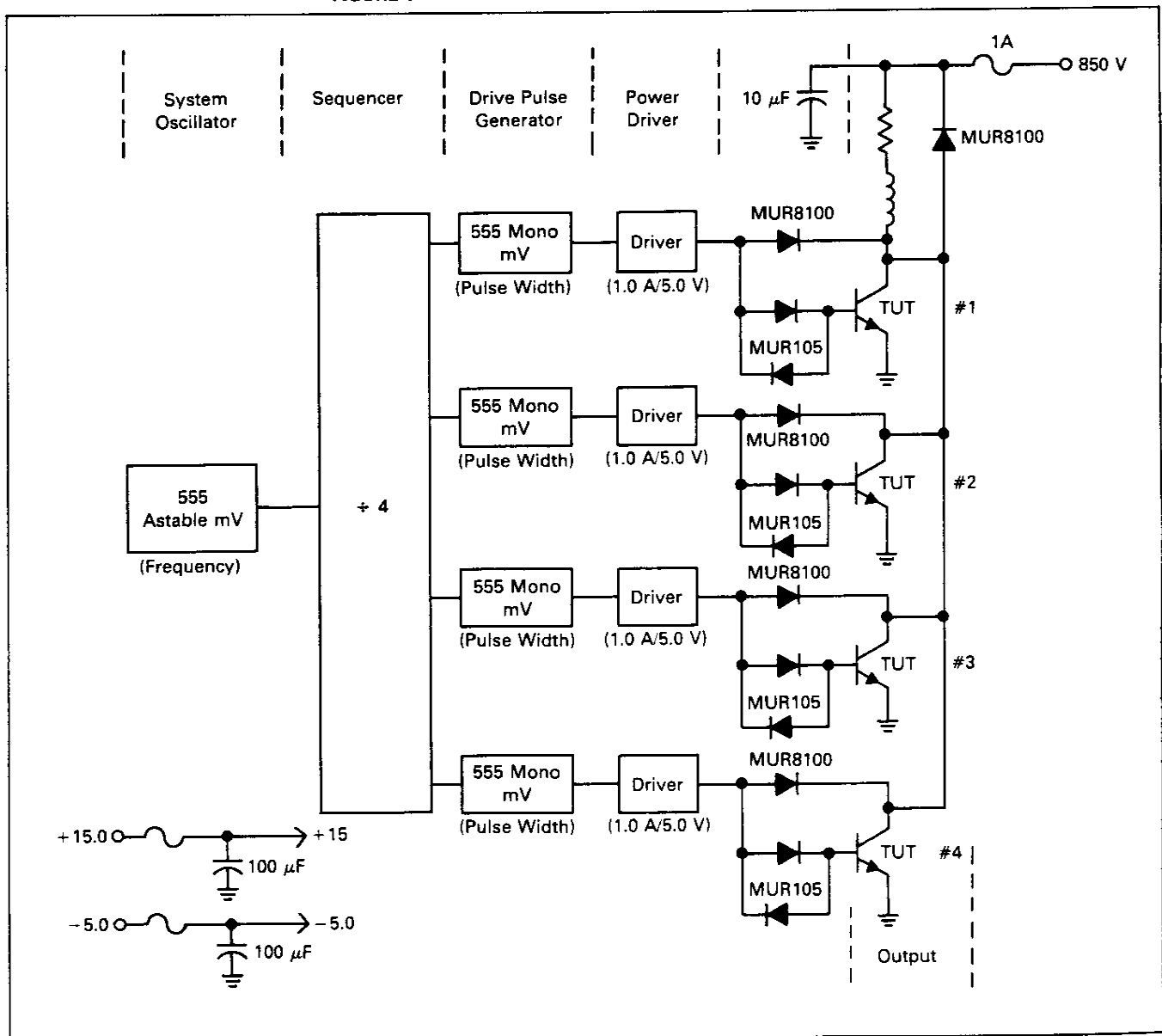
Life testing has centered around a strategy which compares the change in leakage current running off an 800 volt bus to changes in leakage current that are generated from 400 volt operation. Since the 400 volt bus generates load lines that are within the specified ratings, leakage current changes at this level can be considered normal. If the same group of transistors is then run at 800 volts for the same period of time, the two rates of change in leakage can then be compared for an indication of relative stress.

Again, the results are highly favorable. To start, a group of transistors was run for a week (58 hours). Initial and final leakage currents are recorded in Table 3. These transistors were then run for an additional week at 800 volts. The leakage currents are also recorded in Table 3. Note that leakage current actually increased less at 800 volts than it did at 400. This is one more good indication of adequate safety margin.

TABLE 3. PRELIMINARY LIFE TEST RESULTS
(I_{CES} @ 800 V, 25° in μA)

Device	400 Volts			800 Volts		
	Before	After	Δ	Before	After	Δ
1	0.44	0.47	0.03	0.47	0.47	0
2	0.20	0.22	0.02	0.22	0.27	0.05
3	0.40	0.64	0.24	0.64	0.60	-0.04
4	0.42	0.50	0.08	0.50	0.48	-0.01
Group Average	0.37	0.46	0.09	0.46	0.45	-0.01

FIGURE 6 — ULTRAFAST FBSOA LIFE TEST SCHEMATIC



In addition, a second group of transistors is running on a continuing life test, alternating between 400 and 800 volts. After 100 hours of operation at each voltage, the results mirror those of the first group.

BENEFITS

The test results indicate that there is an ability to turn-on into voltages up to $V_{(BR)CBO}$. Using this ability has some big advantages. Suppose, for example, a worst case bus voltage that is 750 volts. Under the old rules, a transistor rated for $V_{(BR)CEO(sus)}$ greater than 750 volts would be required. For purposes of illustration, the MJ16018 can be chosen, based upon an 850 volt $V_{(BR)CEO(sus)}$ rating. Alternately, by making use of an ULTRAFAST diode, the MJ16012 could be selected based upon its 850 volt collector-base rating. This is a good apples & apples comparison, since both parts use the same mask. The differences are listed on Table 4.

TABLE 4. MASK DIFFERENCES

Parameter	MJ16012	MJ16018
Gain @ 10 A 5.0 V	10	4.0
Max $I_C(pk)$ for 1.0 A Base Drive	10 A	5.0 A
Storage Time	600 ns	1200 ns
Crossover Time	50 ns	200 ns
$V_{(BR)CEO(sus)}$	450 V	800 V
$V_{(BR)CBO}$	850 V	1500 V

No matter which one of these parameters is most important, the differences are substantial. Whether switching speeds, the amount of power controlled, or required base drive are considered, the improvement is at least a factor of 2 and perhaps a factor of 4.

PITFALLS


There are two obvious pitfalls to using what can be called ULTRAFAST forward bias safe operating area. First, the amount of test data that has been accumulated is not statistically significant. Designs which use this characteristic are definitely taking a pioneering step. The benefits are considerable, but so are the risks.

There are also risks associated with the base drive. When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as is a stiff negative bias necessary for safe turn-off. Any hiccup in the base drive circuitry that even momentarily violates either of these conditions will likely cause failure of the transistor.

CONCLUSION

The old rule that bipolar transistors could not safely turn-on into voltages above collector-emitter breakdown has been swept away by the tide of new technology. ULTRAFAST recovery rectifiers, by permitting turn-on times well below 100 ns, have made it possible to turn bipolar transistors on into bus voltages up to collector-base breakdown.

There is, however, a distinction to be drawn between possible and guaranteed safe. The results presented here definitely demonstrate that it can be done. By looking for indications of stress from several perspectives, they also suggest that third generation bipolars can be comfortable operating above collector-emitter breakdown. On the other hand, the number of units tested is not statistically sufficient to constitute a guarantee. The possible has been demonstrated, but not guaranteed.

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