INSURING RELIABLE PERFORMANCE FROM POWER MOSFETs

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Due to their many unique advantages, power MOSFETs are being used in an increasing number of applications. To aid the circuit designer in developing reliable power MOSFET circuits, this Application Note examines six potential problem areas and offers suggestions for eliminating or minimizing problems in each area. In addition, as an aid to the many designers who are using power MOSFETs in switched-mode power supplies, this Note includes a section on improving switching power supply circuits.

INTRODUCTION

During the past two years design engineers have witnessed a rapid decrease in the cost and a rapid increase in the performance of power MOSFET devices. As a result of these rapid changes, engineers are finding that some price and performance decisions made within the previous six months are no longer valid — and that a re-evaluation of MOSFET devices is in order.

Whether driven by the search for improved circuit performance, reduced cost, or greater reliability, those desiring to use power MOSFETs must become acquainted with the traits of that technology. Many designers, especially those using MOSFETs for the first time, commonly are concerned that even though their prototypes are operating satisfactorily, the success of their project may be short lived due to some hidden peculiarity of the MOSFET.

Although these concerns are certainly understandable, they are usually without foundation. In both theory and practice, MOSFETs are simple devices and potential subtle problems are well outlined in the literature.

POWER MOSFET BASICS

Fortunately, understanding MOSFET operation is straightforward, and their peculiarities are few. MOSFETs are classified as voltage controlled devices since the drain current, I_D, is controlled by the magnitude of the gate-to-source voltage, V_{GS}. When V_{GS} is high, typically 10 to 15 volts, the MOSFET drain-to-source resistance falls to a very low value and I_D is limited by the impedance of the load and the magnitude of the drain supply voltage. Applying a low voltage across the gate-to-source, often simply 0 volts, increases the drain-to-source resistance to a very high value and turns the transistor off. (The value of the drain-to-source resistance in the "ON" state is called the on-resistance, $r_{DS(on)}$. $r_{DS(on)}$ determines the static losses and is an important figure of merit for a MOSFET device.)

The V_{GS} needed to insure proper switching of a MOSFET can be obtained from the devices' transfer curve. As an example, examination of Figure 1 (transfer characteristic curve of an MTP4N50) reveals that if the desired peak drain current is 7A, the applied V_{GS} must be at least 8.0 volts to keep the device fully on. To provide for device-to-device variation and to minimize $r_{DS(on)}$, designers usually specify a V_{GS} greater than 10 V.

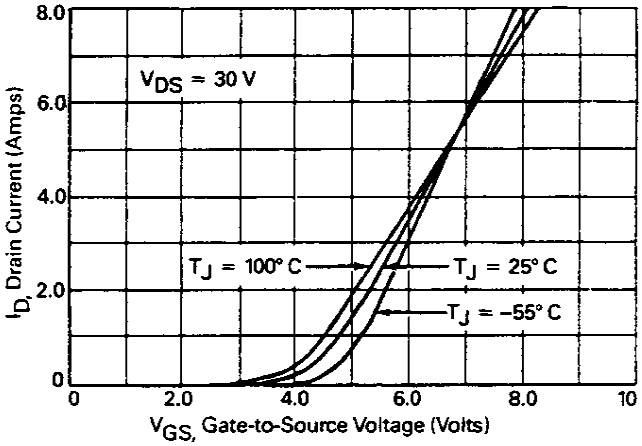

FIGURE 1 — Transfer Characteristics of the MTP4N50

STAYING OUT OF TROUBLE

Six potential trouble areas and recommendations for eliminating or minimizing problems in those areas will be discussed. The six areas are:

1. Excessive drain-to-source voltage, V_{DS}.
2. Excessive gate-to-source voltage, V_{GS}.
3. Handling-related failures.
4. Excessive dv_{DS}/dt.
5. Excessive junction temperature, T_J.
6. Inductance-related switching speed degradation.

1. Excessive V_{DS}

The maximum drain-to-source voltage rating is a particularly important parameter since any excursion beyond the $V_{DS(max)}$ rating is inviting catastrophic failure. Although MOSFETs are not extremely fragile in avalanche, the $V_{DS(max)}$ rating is specified as an instantaneous limit. Excessive drain-to-source voltage is probably the most common way in which power MOSFETs are destroyed.

Due to "flyback" voltages, excessive V_{DS} failures often occur in power MOSFETs during the transition from designing with slower devices. Flyback voltages occur

when current in an inductive load is rapidly interrupted ($v = -L di/dt$). Unless these voltages are clamped or snubbed by circuits with very fast response times, the drain-to-source can be avalanched. A clamp circuit that is adequate for slower devices may be ineffective or marginal for power MOSFETS.

The simplest illustration of a potentially marginal clamp is a clamp diode across an inductive load. Assuming an ideal diode, the voltage induced across the inductor is never greater than the diode drop, and the drain-to-source voltage of the MOSFET is clamped to the positive rail. However, the diode has package, lead and wiring inductance and a forward recovery time, t_{fr}. Their cumulative effect is to render the diode ineffective during the first few tens of nanoseconds of the turn-off transition. If the MOSFET is switching faster than the diode can clamp the load, system reliability is jeopardized.

At very high di/dt, V_{DS} can also be affected by the source and drain inductance of the MOSFET package. Both TO-3 and TO-220 packages exhibit a total source and drain package inductance of approximately 12 nH. During turn-off, the voltages appearing across the package inductances add to that observed at the drain and source terminals to provide the total voltage at the die.*

*NOTE: Measuring V_{DS}.

Voltage measurement techniques appropriate for slower switching devices can underestimate values of peak V_{DS} and give a false sense of security for rapidly switched MOSFETs. Moving into the realm of sub-100 nsec switching transitions requires new methods for monitoring V_{DS} and flyback voltage.

Since MOSFETs are capable of producing surprisingly high di/dt's, V_{DS} should be monitored as closely as possible to the device. If the V_{DS} measurement includes the voltage appearing across a parasitic inductance in the source or drain (as illustrated in Figure 2), at turn-off the magnitude of the drain-to-source voltage actually appearing at the device terminals is greater. Any lead, wiring or package inductance adds approximately 1 nH per millimeter. Especially for the new, low voltage, high current MOSFETs (I_D > 20 A), voltages induced in the parasitic inductances may be a significant percentage of the V_{DS} rating.

For accurate measurements, a high frequency oscilloscope (B.W. > 150 MHz), a voltage probe with similar bandwidth, and correct probe placement are important. The preferred method is to use a scope probe such as the Tektronix Model #P6106 miniature voltage probe (B.W. = 250 MHz) inserted into a chassis mount test jack (for example, Tektronix Test Jack Part Number 131-0258-00). Attaching the ground of the test jack to the source and its tip to the drain bypasses all but the package inductance and gives a very good indication of the true V_{DS}.

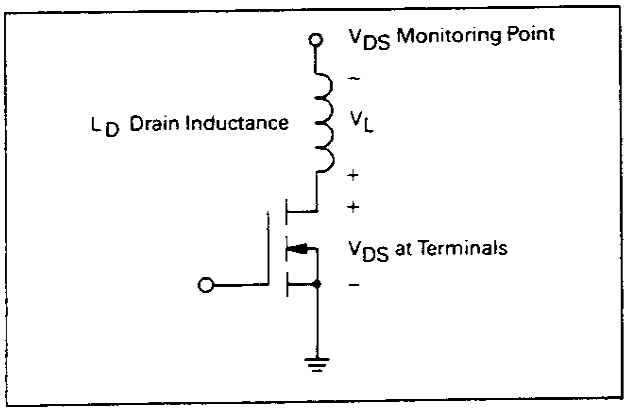

FIGURE 2 — At Turn-off, V_{DS} Appearing at the Terminals Is Equal to V_{DS} at the Monitoring Point Plus V_L

2. Excessive V_{GS}

The gate of the power MOSFET is isolated from the rest of the chip by a thin layer of SiO_2; exceeding the maximum V_{GS} rating (20 V for the MTP4N50) can rupture the gate oxide and destroy the device.

Voltage transients generated by the gate drive or coupled from the drain by the gate-to-drain capacitor can disturb circuit performance by triggering an unwanted turn-on due to momentarily high V_{GS}. In extreme cases, the transients from the gate drive cause device failure if the $V_{GS(MAX)}$ (20 V) rating is exceeded. If such transients are possible, a 20 V zener diode placed across the gate and source protects the MOSFET from rupture of its gate oxide.

3. Handling-Related Failures

Power MOSFETs, although less sensitive than CMOS devices, are susceptible to damage by electrostatic discharge (ESD). Consequently, the handling precautions recommended for CMOS IC's also are applicable to MOSFETs.

4. Excessive dv_{DS}/dt

Extremely rapid changes in the drain-to-source voltage may be of some concern to designers using power MOSFETs. Of the two modes that can cause problems, the first only disturbs circuit performance, while the second mode can cause device failure.

First mode. The first mode is referred to as "static dv/dt" since the MOSFET is not conducting when the dv/dt occurs. Figure 3, which shows the MOSFET and its parasitic NPN transistor, helps to define the problem. In some of the first MOSFETs, a large dv/dt (on the order of 30 volts/ns) could cause a displacement current through C_{ds} large enough to forward bias the base-to-emitter junction of the parasitic transistor. The associated turn-on of the

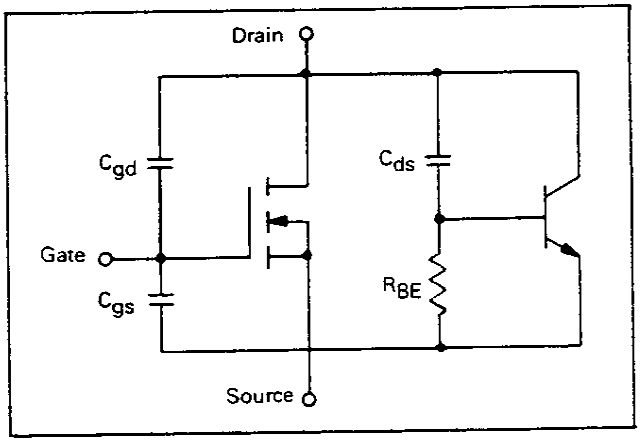

FIGURE 3 — The Power MOSFET With Its Parasitic Capacitances and Parasitic NPN Bipolar Transistor

bipolar transistor could cause a localized hot spot and device failure. In present devices, however, the magnitude of R_{BE} is so low that the dv/dt needed to effect problems is not practically obtainable.

Capacitor C_{gd} in Figure 3 also conducts during a rapid dv/dt. If the applied dv/dt and the gate-to-source impedance are high, then the displacement current through C_{gd} can cause V_{GS} to rise above the threshold voltage and cause the MOSFET to turn on. If the device begins to turn on, the drain-to-source voltage will fall, thereby reducing the applied dv/dt. Since the MOSFET is likely to be operating well within its forward biased SOA ratings and the spurious turn on lasts for a very short time, failures are

not typical in this mode of operation. The only result is a brief disturbance in circuit performance. Since a circuit problem (high gate-to-source impedance) and not a device problem causes the undesired turn-on, the solution to the problem is circuit oriented. A low gate drive impedance insures that the displacement current through C_{gd} does not develop a large enough potential across the gate-to-source terminals to turn the MOSFET on.[1]

Second mode. The second possible dv/dt mode is more critical since it can cause device failure. It occurs only when several conditions are present simultaneously. Figure 4a helps illustrate these conditions. In the totem pole

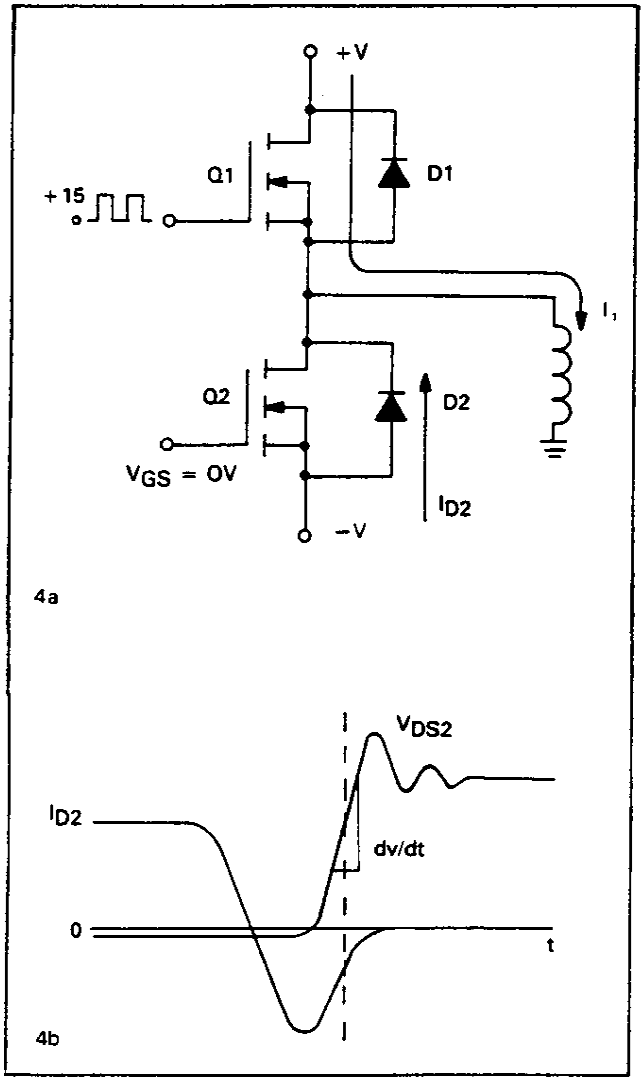

FIGURE 4 — In Bridge Configurations (a) dv/dt Precautions May Be Necessary. Several Conditions Must Exist Simultaneously, As In (b), Before Failures are Possible.

circuit, the diode of Q2 protects Q1 from excessive V_{DS} when Q1 turns off. It does so by providing a low impedance path for the inductive load current.

For instance, assume that Q1 is turned on, establishing load current I_1. When Q1 is switched off, the inductive load draws current, I_{D2}, through D_2. At this point in some circuits, Q2 is turned on, which represents no dv/dt concerns. But if Q1 is rapidly turned on while D_2 is still conducting, Q2 may fail due to excessive dv/dt or high feedthrough current. Figure 4b shows the instant at which failures can occur. Note that the diode must be conducting a reverse recovery current, a high dv/dt (> 0.3v/ns) must

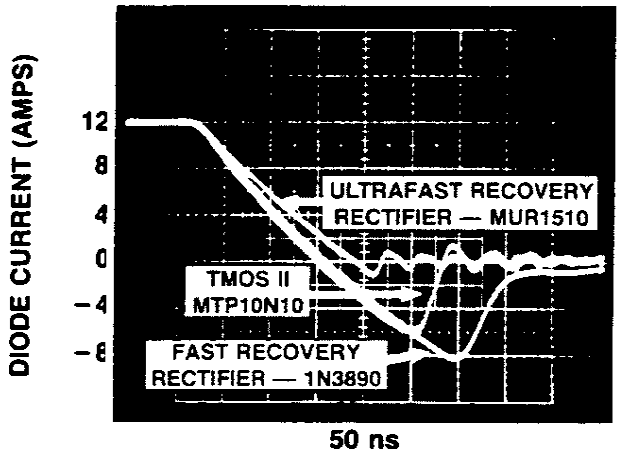

FIGURE 5 — Reverse Recovery Characteristics of: (a) 15 A, 100 V Ultrafast Recovery Rectifier; (b) 10 A, 100 V TMOS II; and (c), 12 A, 100 V Fast Recovery Rectifier.

be present and V_{DS} must be at least one-half of BV_{DSS} before failures occur.[2,3]

Several solutions to this second mode of dv/dt failures are available in the literature.[4,5,6] The optimum solution, however, is to make the MOSFET more immune to such dv/dt stress or to reduce both the reverse recovery time, t_{rr}, and reverse recovery charge, Q_{rr}, of the devices' intrinsic diode. The major manufacturers are in the process of doing both.

For example, the second generation of power MOSFETs from Motorola, dubbed "TMOS II™", show a marked improvement in t_{rr} and Q_{rr}. Previously the reverse recovery time of the drain-to-source diode was comparable to that of a fast recovery rectifier. However, as Figure 5 shows, some second generation devices have reverse recovery characteristics approaching those of ultrafast rectifiers.

These improvements have not required additional complicated processing steps that increase costs, nor have they compromised other important device parameters. In fact, just the opposite is true. For example, for a given die size, the improvement in $r_{DS(on)}$ of TMOS II over that of standard TMOS is about 30% for low voltage ($V_{BR(DS)} \leq 200$ V) devices. A designer often can replace a standard power MOSFET with a second generation device that has a smaller chip size, better performance, and a lower cost.

5. Excessive Junction Temperature, T_J

Next to excessive V_{DS}, V_{GS}, and dv/dt, the next great enemy to long term reliability is excessive junction temperature, T_J. Most designers understand that operating at junction temperatures in excess of the maximum rating seriously compromises reliability. They also know that even below $T_{J(max)}$, long term reliability is enhanced with lower operating junction temperatures. Consequently, with respect to thermal considerations, designers usually are fairly conservative. Since the pulsed and continuous current ratings reflect thermal limitations, systems typically are designed to operate well within both their current and thermal ratings.

With this guardbanding, thermally induced failures are rare under normal operating conditions. However, fault conditions, such as a shorted load, or other system failures can place an unanticipated thermal stress on the transistor and cause abrupt and catastrophic failures. In short, except in cases of serious neglect, thermal failures most often are system induced.

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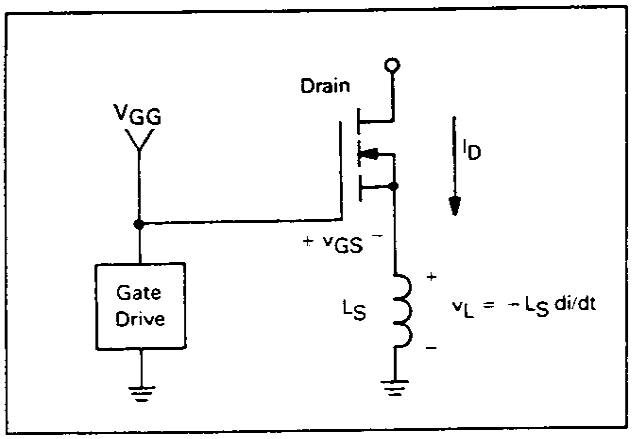

FIGURE 6 — Source Inductance Degrades the Turn-on and Turn-off Switching Transitions

6. Inductance-Related Degradation in Switching Speed

Any inductance in the source lead degrades switching speeds. The polarity of v_L in Figure 6 is such that the induced voltage always opposes the desired change in v_{GS}. For instance, during turn-on L_S opposes an increase in I_D and develops the polarity shown. Loop analysis shows that $v_{GS} = v_{GG} - v_L$. The opposite condition exists during turn-off, since the polarity of the voltage across L_S reverses and increases v_{GS}. Especially for high current MOSFETs, the maximum switching speed may be bounded by the source inductance. A simple way to minimize the bulk of the problem is to return the gate drive directly to the source pin, bypassing any L_S in the high current load path.

Summary

In summary of the failure modes discussed, the search for the causes of unexplained failures should begin with the meticulous observation of V_{DS}. Once satisfied that excessive V_{DS} is not the problem, the engineer should study the gate-to-source voltage waveform and insure that the current sourcing and sinking capability of the gate drive is adequate. Next, the device handling procedures should be checked to make certain that ESD is not damaging the gate oxide. The two dv/dt modes should then be examined, followed by a look at the junction temperature and failures that may be system induced. Finally, if switching speeds are slower than were expected, the possiblity of inductance-related switching speed degradation should be examined.

SUBTLE ADVANTAGES OF MOSFETs

Descriptions of performance advantages of MOSFETs are detailed in available literature. One advantage of MOSFETs not often discussed is the relative ease in which their SOA ratings can be interpreted. Figure 7 compares the RBSOA, or Reverse Biased SOA of the MJE13007 (a 400 V, 8 A bipolar) with the turn-off SOA of the MTP4N50 (a 500 V, 4 A power MOSFET). The comparison is between transistors of equal die area. Although the MOSFET and bipolar curves carry different titles, they both outline the SOA boundaries at turn-off.

If the designer, using a MOSFET device, insures that three specific conditions (pulsed current, V_{DS}, and T_J) are within their ratings, then he can be confident that the design is within the operating limits outlined by the MOSFET turn-off SOA curves. Interpretation of the bipolar RBSOA, however, is not as straightforward. Since the rating varies with T_J, I_{B1}, duty cycle, pulse width, and off bias, derating for the various combinations of influential parameters is as much an art as it is a science. The manufacturer's role is difficult because testing and guaranteeing RBSOA for the multitude of combinations of the independent variables is nearly impossible. The best the manufacturer can do is to rate the device at conditions that pertain to "typical" applications. If the designer is using the device at or near those conditions, the ratings provide

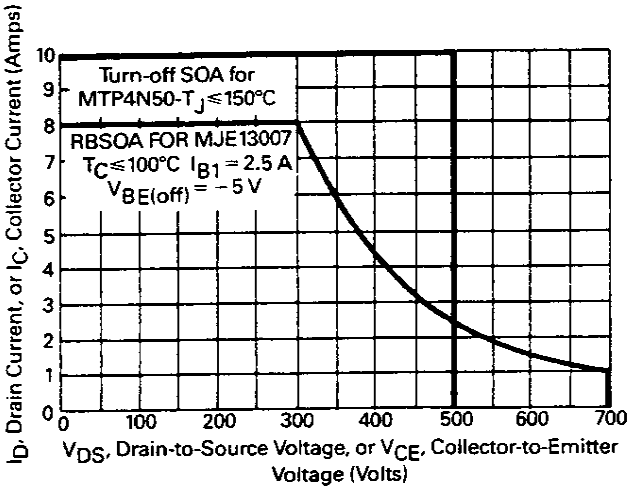

FIGURE 7 — Comparison of the MOSFET Turn-off SOA Rating and the RBSOA Rating of a Bipolar of Similar Die Area

the needed information. If not, the information he has is spotty and he may be forced to derate extensively to insure trouble free service.

Two other useful observations can be made from Figure 7. The first observation is that the power MOSFET curve encompasses more area than the bipolar curve. Even at the pulsed current rating, the MOSFET's turn-off SOA extends to its maximum V_{DS} rating. This is due to the MOSFET's positive temperature coefficient of on-resistance which tends to force current sharing across the entire die. With the MOSFET's reduction of the possibility of current crowding and hotspotting, a second breakdown derating is unnecessary.

The second observation, this one favoring the bipolar device, is that of the major differences in high voltage characteristics between the bipolar and MOSFET devices. Note that the MOSFET's rating abruptly terminates at the 500 V maximum V_{DS} rating, whereas the bipolar's rating extends well beyond its V_{CEO} rating of 400 V. This extended voltage rating is useful in applications in which the turn-off collector-to-emitter voltage is quite high. (I_C must still be constrained by the RBSOA rating.)

USING MOSFETs IN SWITCHED-MODE POWER SUPPLIES

The power MOSFETs' unique advantages are fueling the trend toward increased MOSFET usage in switched-mode power supplies. The three main advantages provided by MOSFETs are faster switching speeds, greater SOA, and simpler gate requirements. Any one of these advantages can cause the designer to choose a MOSFET for a specific application. For instance, at operating frequencies above 150 kHz, bipolar devices do not provide satisfactory performance; the high frequency characteristics of the

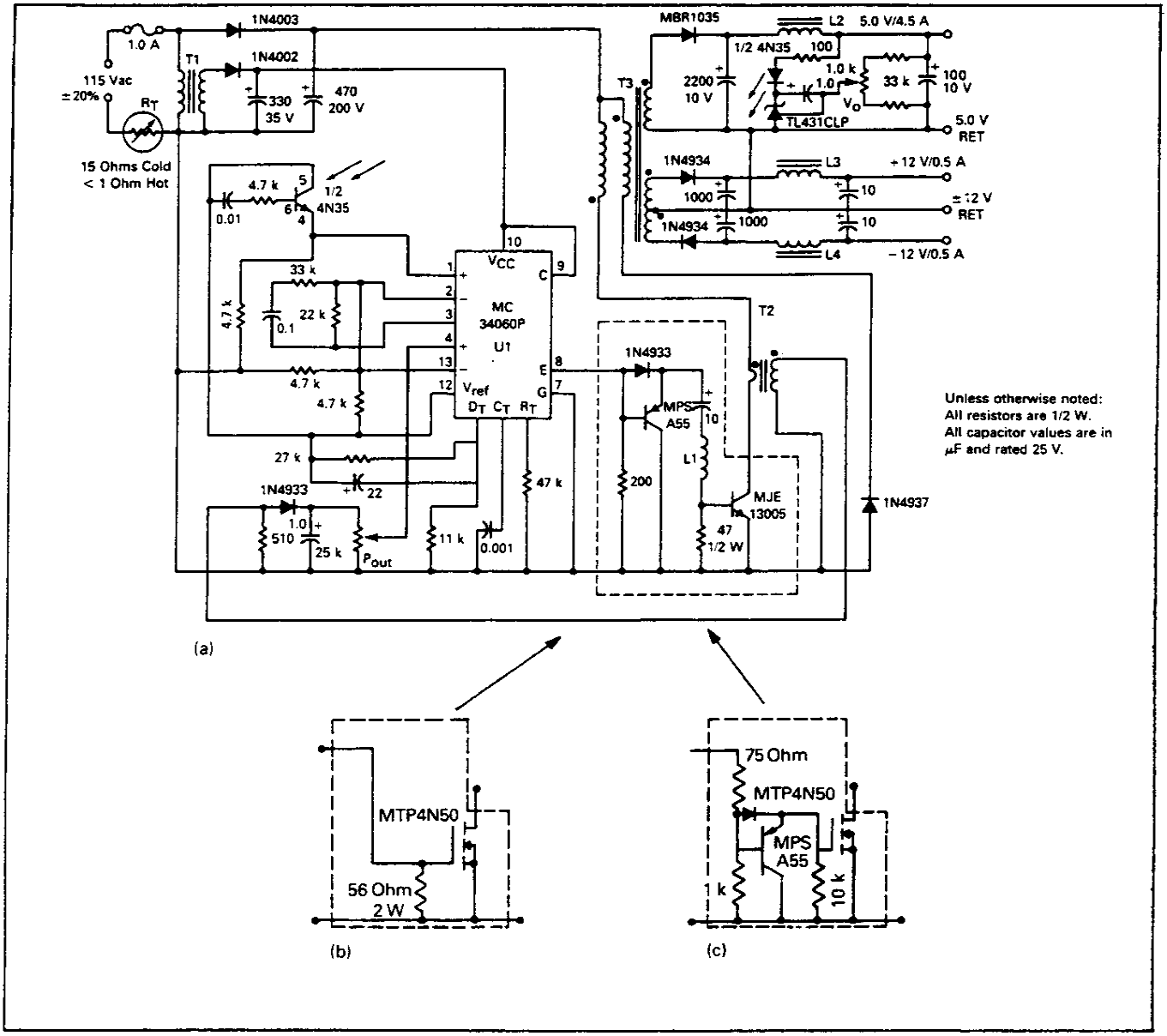

FIGURE 8 — A 20 kHz, 35 W Switched-mode Power Supply With: (a), A Bipolar Transistor; (b), A Power MOSFET With a Simple But Inefficient Gate Drive Network, and (c), A MOSFET With an Efficient, Fast and Inexpensive Alternative.

MOSFET make it the only viable choice. In other applications, the designer may select a MOSFET device because his design can benefit from all three of the MOSFET's most significant advantages.

Even at switching frequencies of 20 kHz, where good high frequency characteristics are not vital, the power MOSFET can be quite competitive. For example, consider the 20 kHz, 35 W power supply with a bipolar power transistor (an MJE13005) shown in Figure 8. In this circuit, the crossover time at turn-off is slightly under one microsecond and the case temperature of the MJE13005 is 71°C. (The case temperature rise above the 25°C ambient temperature serves as an indication of the transistor's relative inefficiency.)

If a MOSFET, an MTP4N50, is used in place of the bipolar, several components of the drive circuitry become superfluous (Figure 8b). In fact, five of the six elements that function with the MC34060 to form the drive circuit can be omitted. One might expect that performance would greatly suffer by such a drastic simplification of drive circuitry, but the opposite is true. With the MOSFET in the circuit the crossover time falls into the 50 ns range, and the case temperature rise is a mere 18°C—compared to 46°C for the bipolar. (This direct drive scheme also reduces design time to a minimum.)

The MOSFET drive circuit shown in Figure 8b still consumes as much power as the bipolar base drive circuit that it replaces. In this configuration, the MC34060 cannot discharge the MOFSET's input capacitance. Therefore, the size of R_{GS} dictates the gate-to-source impedance and the switching times during the turn-off transition. Since the magnitude of R_{GS} must be low to minimize turn-off time, drive losses in the on-state are high (≈2W) due to a V_{GS} of 10 to 12 V.

The addition (Figure 8c) of a few very inexpensive components increases gate drive efficiency without any degradation of switching speeds. Superficially, this option may not appear to offer much improvement over the orig-

inal bipolar circuit. There are, however, two important differences. First, the bipolar base drive carries a small cost premium due to the inductor, capacitor and larger diode. Second, and potentially more significant, the power supplied to the more efficient MOSFET gate drive circuit is much lower than that needed for the bipolar configuration. Unlike the drives in the two previous examples, the gate drive in 8c consumes most of its power during the very short switching transitions. Consequently, instead of using a transformer (T1) to generate the I.C.'s supply voltage, the designer may choose to obtain it by tying a voltage dropping resistor in series with a regulating zener diode across the rectified bus.

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