MEASUREMENT OF ZENER VOLTAGE TO THERMAL EQUILIBRIUM WITH PULSED TEST CURRENT

Prepared by
Herb Saladin
Discrete Power
Application Engineering

This paper discusses the zener voltage correlation problem which sometimes exists between the manufacturer and the customer's incoming inspection. A method is shown to aid in the correlation of zener voltage between thermal equilibrium and pulse testing. A unique double pulsed sample and hold test circuit is presented which improves the accuracy of correlation.[1]

Several zener voltages versus zener pulsed test current curves are shown for ten package styles. An appendix is attached for incoming inspection groups giving detailed information on tolerances involved in correlation.

INTRODUCTION

For many years the major difficulty with zener diode testing seemed to be correlation of tight tolerance voltage specifications where accuracy between different test set-ups was the main problem. The industry standard and the EIA Registration system adopted thermal equilibrium testing of zener diodes as the basic test condition unless otherwise specified. Thermal equilibrium was chosen because it was the most common condition in the final circuit design and it was the condition that the design engineers needed for their circuit design and device selection. Thermal equilibrium testing was also fairly simple to set-up for sample testing at incoming inspection of standard tolerance zeners.

In recent years with the advent of economical computerized test systems many incoming inspection areas have implemented computer testing of zener diodes which has been generating a new wave of correlation problems between customers and suppliers of zener diodes.

The computerized test system uses short duration pulse test techniques for testing zener diodes which does not directly match the industry standard thermal equilibrium test specifications.

This paper was prepared in an attempt to clarify the differences between thermal equilibrium and short duration pulse testing of zener diodes, to provide a test circuit that allows evaluation at various pulse widths and a suggested procedure for incoming inspection areas that will allow meaningful correlation between thermal equilibrium and pulse testing.

In the measurement of zener voltage (V_Z), the temperature coefficient effect combined with test current heating can present a problem if one is attempting to correlate V_Z measurements made by another party (Final Test, Quality Assurance or Incoming Inspection).[2] This paper is intended as an aid in determing V_Z at some test current (I_{ZT}) pulse width other than the pulse width used by the manufacturer.

Thermal equilibrium (TE) is reached when diode junction temperature has stabilized and no further change will occur in V_Z if the I_{ZT} time is increased.[2] This absolute value can vary depending on the mounting method and amount of heat sinking. Therefore, thermal equilibrium conditions have to be defined before meaningful correlation can exist.

Normalized V_Z curves are shown for ten package styles and for two to five voltage ratings per package. Pulse widths from 1.0 ms up to 100 seconds were used to arrive at or near thermal equilibrium for all packages with a given method of mounting.

©MOTOROLA INC., 1984

ClibPDF - www.fastio.com

Mounting

There are five conditions that can affect the correlation of V_Z measurements and are: 1) instrumentation, 2) T_A, 3) I_{ZT} time, 4) P_D and 5) mounting. The importance of the first four conditions is obvious but the last one, mounting, can make the difference between good and poor correlation. The mounting can have a very important part in V_Z correlation as it controls the amount of heat and rate of heat removal from the diode by the mass and material in contact with the diode package.

Three mounting methods used are:

1. Axial leaded package: Standard Grayhill clips (#2-8, Figure 14) and Motorola fixture #2-13600A, Figure 15).
2. TO-3 (Case 54): Finned heat sink WE1 model #3246 (0.83°C/W). Not shown.
3. Stud packages, DO-4 (Case 56). Case 58 and TO-220: aluminum block 2⅜" x 3⅝" x 4" (Figure 16).

Two glass axial lead packages (DO-35 and DO-41), curves (Figure 12 and 13) were measured with standard Grayhill clips and a modified version of the Grayhill clips to permit lead length adjustment. Also, these diodes were measured in a special mounting fixture used by Motorola final test on all axial lead diodes. This elaborate fixture is specially made and has more mass for heat sinking than the standard Grayhill clips. With modification of the Grayhill clips permitting lead length adjustment, V_Z measurements can be made to correlate with the special fixture, if so desired.

Test Circuit

The test circuit (Figure 17) consists of standard CMOS logic for pulse generation, inverting and delaying. The logic drives three bipolar transistors for generation of the power pulse for I_{ZT}. V_Z is fed into an unique sample and hold (S/H) circuit consisting of two high input impedance operational amplifiers and a field effect transistor switch.

For greater accuracy in V_Z measurements using a single pulse test current, the FET switch is double pulsed. Double pulsing the FET switch for charging the S/H capacitor increases accuracy of the charge on the capacitor as the second pulse permits charging the capacitor closer to the final value of V_Z.

The timing required for the two pulse system is shown in waveform G-3C whereby the initial sample pulse is delayed from time zero by a fixed 100 μs to allow settling time and the second pulse is variable in time to measure the analog input at that particular point. The power pulse (waveform G-2D) must also encompass the second sample pulse.

To generate these waveforms, four time delay monostable multivibrators (MV) are required. Also, an astable MV, is required for free-running operation; single pulsing is simply initiated by a push-button switch S1. All of the pulse generators are fashioned from two input, CMOS NOR gates; thus three quad gate packages (MC14001) are required. Gates 1A and 1B form a classical CMOS astable MV clock and the other gates (with the exception of Gate 2D) comprise the two input NOR gate configured monostable MV's. The Pulse Width variable delay output (Gate 1D) positions the second sample pulse and also triggers the 100 μs Delay MV and the 200 μs Extended Power Pulse MV. The respective positive going outputs from gates 3A and 2C are diode NOR'ed to trigger the Sample Gate MV whose output will consequently be the two sample pulses. These pulses then turn on the PNP transistor Q1 level translator and the following S/H N-channel FET series switch Q2. Op amps U4 and U5, configured as voltage followers, respectively provide the buffered low output impedance drive for the input and output of the S/H. Finally, the pulse extended Power Gate is derived by NORing (Gate 2D) the Pulse Width Output (Gate 1D) with the 200 μs MV output (Gate 2C). This negative going gate then drives the Power Amplifier, which, in turn, powers the D.U.T. The power amplifier configuration consists of cascaded transistors Q3–Q5, scaled for test currents up to 2.0 A.

Push button switch (S4) is used to discharge the S/H capacitor. To adjust the zero control potentiometer, ground the non-inverting input (Pin 3) of U4 and discharge the S/H capacitor.

Testing

The voltage V_{CC}, should be about 50 volts higher than the D.U.T. and with R_C selected to limit the I_{ZT} pulse to a value making $V_{ZT}\, I_{ZT} = \frac{1}{4} P_D$ (max), thus insuring a good current source. All testing was performed at a normal room temperature of 25°C. A single pulse (manual) was used and at a low enough rate that very little heat remained from the previous pulse.

The pulse width MV (1C and 1D) controls the width of the test pulse with a selector switch S3 (see Table 1 for capacitor values). Fixed widths in steps of 1, 3 and 5 from 1.0 ms to 10 seconds in either a repetitive mode or single pulse is available. For pulse widths greater than 10 seconds, a stop watch was used with push button switch (S1) and with the mode switch (S2) in the > 10 seconds position.

For all diodes with V_Z greater than about 6.0 volts a resistor voltage divider is used to maintain an input of about 6.0 V to the first op amp (U4) so as not to overload or saturate this device. The divider consists of R5 and R6 with R6 being 10 kΩ and R5 is selected for about a 6.0 V input to U4. Precision resistors or accurate known values are required for accurate voltage readout.

Using Curves

Normalized V_Z versus I_{ZT} pulse width curves are shown in Figure 1 through 13. The type of heat sink used is shown or specified for each device package type. Obviously, it is beyond the scope of this paper to show curves for every voltage rating available for each package type. The object was to have a representative showing of voltages including when available, one diode with a negative temperature coefficient (TC).

These curves are actually a plot of thermal response versus time at one quarter of the rated power dissipation. With a given heat sink mounting, V_Z can be calculated at some pulse width other than the pulse width used to specify V_Z.

For example, refer to Figure 12 which shows normalized V_Z curves for the axial lead DO-35 glass package. Three mounting methods are shown to show how the mounting effects device heating and thus V_Z. Curves

ClibPDF - www.fastio.com

are shown for a 3.9 V diode (1N5228) which has a negative TC and a 12 V diode (1N5242) having a positive TC.

In Figure 12, the two curves generated using the Grayhill mountings are normalized to V_Z at TE using the Motorola fixture. There is very little difference in V_Z at pulse widths up to about 10 seconds and only causing a very small error in V_Z. The maximum error occurs at TE between mounting and can be excessive if V_Z is specified at TE and a customer measures V_Z at some narrow pulse width and does not use a correction factor.

Using the curves of Figure 12, V_Z can be calculated at any pulse width based upon the value of V_Z at TE which is represented by 1.0 on the normalized V_Z scale. If the 1N5242 diode is specified at 12 V ± 1.0% at 90 seconds which is at TE, V_Z at 100 ms using either of the Grayhill clips curves would be 0.984 of the V_Z value at TE or 1.0 using the Motorola fixture curve. If the negative TC diode is specified at 3.9 V ± 1.0% at TE (90 seconds), V_Z at 100 ms would be 1.011 of V_Z at TE (using Motorola fixture curve) when using the Grayhill clips curves.

In using the curves of Figure 12 and 13, it should be kept in mind that V_Z can be different at TE for the three mountings because diode junction temperature can be different for each mounting at TE which is represented by 1.0 on the V_Z normalized scale. Therefore, when the correlation of V_Z between parties is attempted, they must use the same type of mounting or know what the delta V_Z is between the two mounting involved.

The Grayhill clips curves in Figure 13 are normalized to the Motorola fixture at TE as in Figure 12. Figures 1 through 11 are normalized to V_Z at TE for each diode and would be used as Figures 12 and 13.

Measurement accuracy can be affected by test equipment, power dissipation of the D.U.T., ambient temperature and accuracy of the voltage divider if used on the input of the first op-amp (U4). The curves of Figures 1 through 13 are for an ambient temperature of 25°C, at other ambients, θV_Z has to be considered and is shown on the data sheet for the 1N5221 series of diodes. θV_Z is expressed in mV/°C and for the 1N5228 diode is about −2.0 mV/°C and for the 1N5242, about 1.6 mV/°C. These values are multiplied by the difference in T_A from the 25°C value and either subtracted or added to the calculated V_Z depending upon whether the diode has a negative or positive TC.

TABLE 1.
S3 — Pulse Width

Switch Position	*C(μF)	t(ms)
1	0.001	1
2	0.004	3
3	0.006	5
4	0.01	10
5	0.04	30
6	0.06	50
7	0.1	100
8	0.4	300
9	0.6	500
10	1.0	1K
11	1.2	3K
12	6.0	5K
13	10	10K

*Approximate Values

General Discussion

The TC of zener diodes can be either negative or positive, depending upon die processing. Generally, devices with a breakdown voltage greater than about 5.0 V have a positive TC and diodes under about 5.0 V have a negative TC.

Die processing variations can vary greatly to achieve desired voltages, TC, impedance and capacitance.[2] For example, Figure 7 shows TO-220 10 W devices; other than the 3.0 V negative TC device, the positive TC diodes show very little difference in normalized V_Z for the different voltages. Figure 3, DO-41, plastic devices, show a similar condition for the voltage range between 12 V and 200 V. The user will have to interpolate between curves for other V_Z values or possibly generate their own curves.

Conclusion

Curves showing V_Z versus I_{ZT} pulse width can be used to calculate V_Z at a pulse width other than the one used to specify V_Z. A test circuit and method is presented to obtain V_Z with a single pulse of test current to generate V_Z curves of interest.

References

(1) Al Pshaenich, "Double Pulsing S/H Increases System Accuracy"; Electronics, June 16, 1983.
(2) Motorola Zener Diode Manual, Series A, 1980.

Motorola reserves the right to make changes without further notice to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Employment Opportunity/ Affirmative Action Employer.

ClibPDF - www.fastio.com

FIGURES 1 thru 17 — Conditions: Single Pulse, T_A = 25°C, V_Z @ I_{ZT} = ¼ P_D (Max) Each device normalized to V_Z at TE.

Axial Lead Packages: Mounting Standard Grayhill Clips

FIGURE 1 — DO-35 (GLASS) 500 mW DEVICE

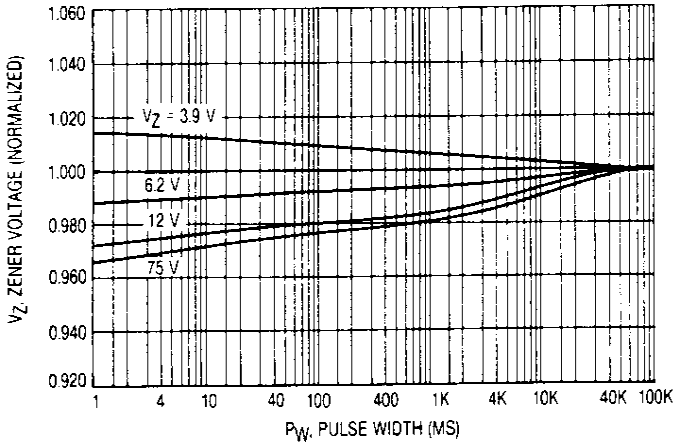


FIGURE 2 — DO-41 (GLASS) 1 WATT DEVICE

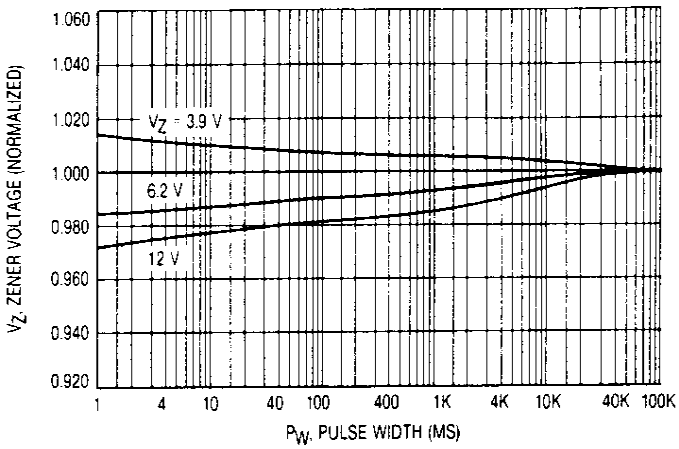


FIGURE 3 — DO-41 (PLASTIC) 1.5 WATT DEVICE

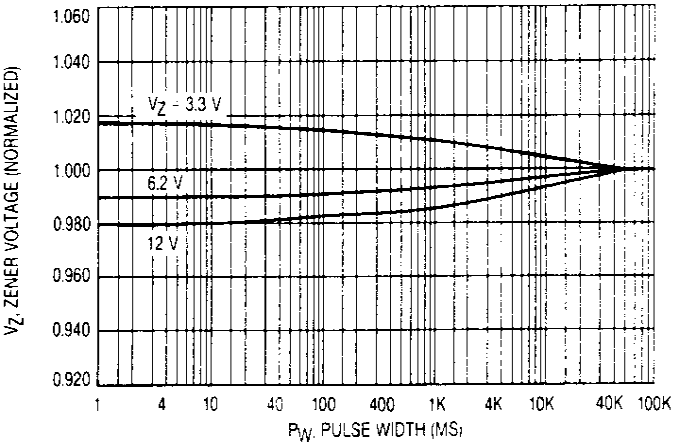


FIGURE 4 — DO-7 (GLASS) 400 mW DEVICE

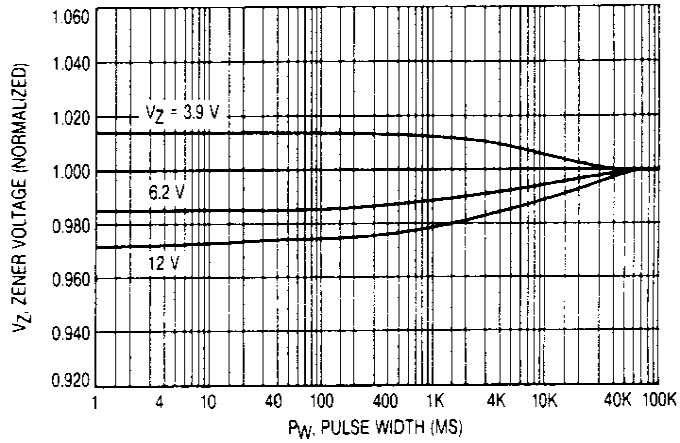


FIGURE 5 — DO-13 (METAL) 1 WATT DEVICE

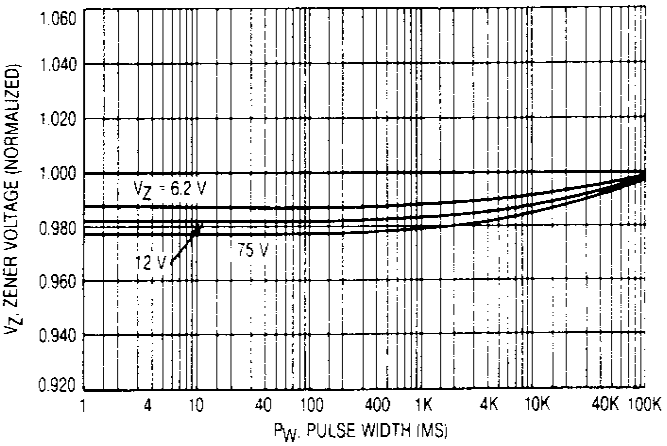
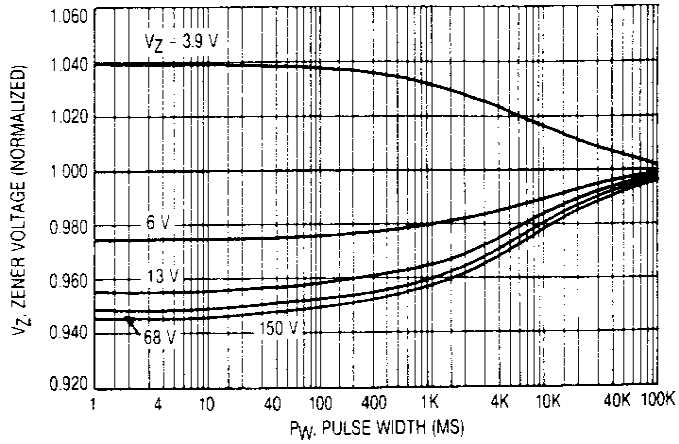


FIGURE 6 — CASE 17 (PLASTIC) 5 WATT DEVICE



ClibPDF - www.fastio.com

TO-220 Packages: Heat Sink, Aluminum Block 2⅜" x 3⅝" x 4"

FIGURE 7 — 10 WATT DEVICE

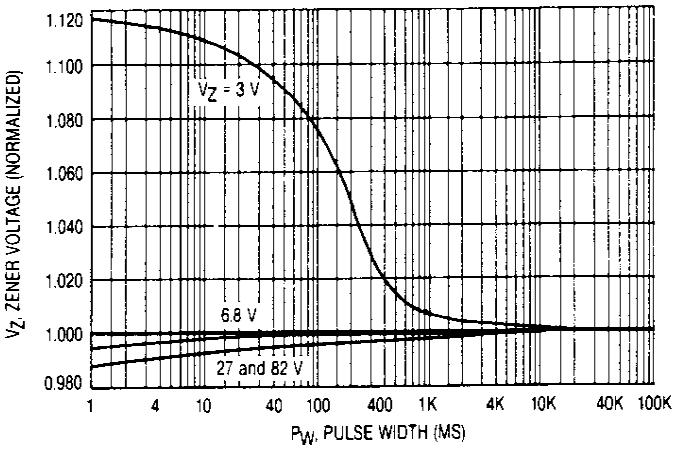
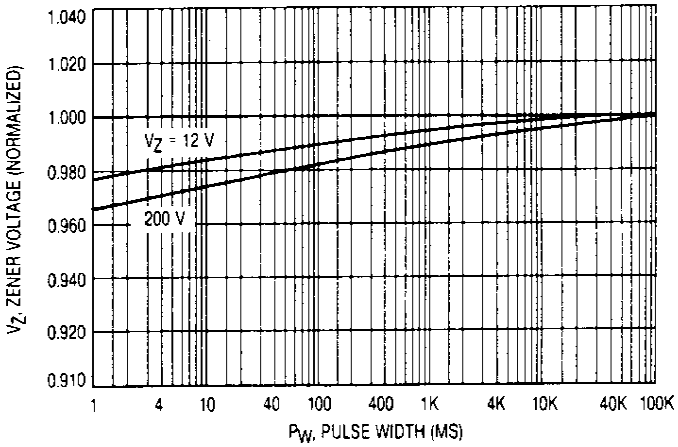


FIGURE 8 — 50 WATT DEVICE



Stud Packages: Heat Sink, Aluminum Block 2⅜" x 3⅝" x 4"

FIGURE 9 — DO-4, 10 WATT DEVICE

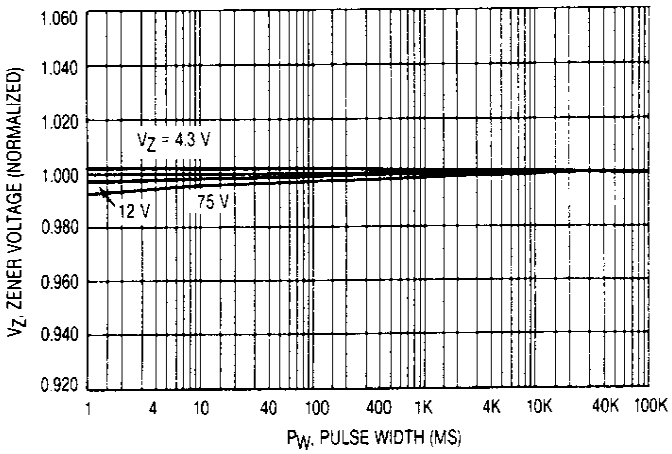


FIGURE 10 — CASE 58, 50 WATT DEVICE

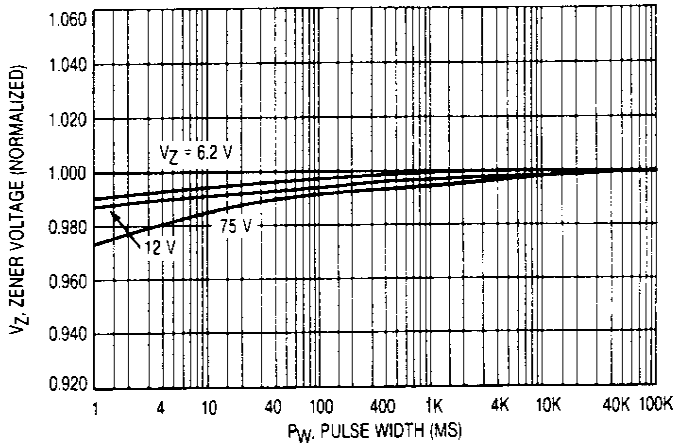
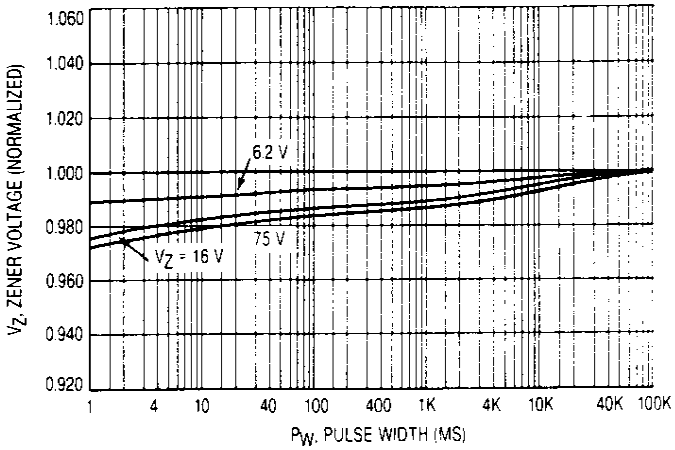


FIGURE 11 — TO-3, 50 WATT DEVICE
HEAT SINK: WEI #3246



ClibPDF - www.fastio.com

Three Mounting Methods: DO-35 and DO-41

FIGURE 12 — DO-35 (GLASS) 500 mW DEVICE

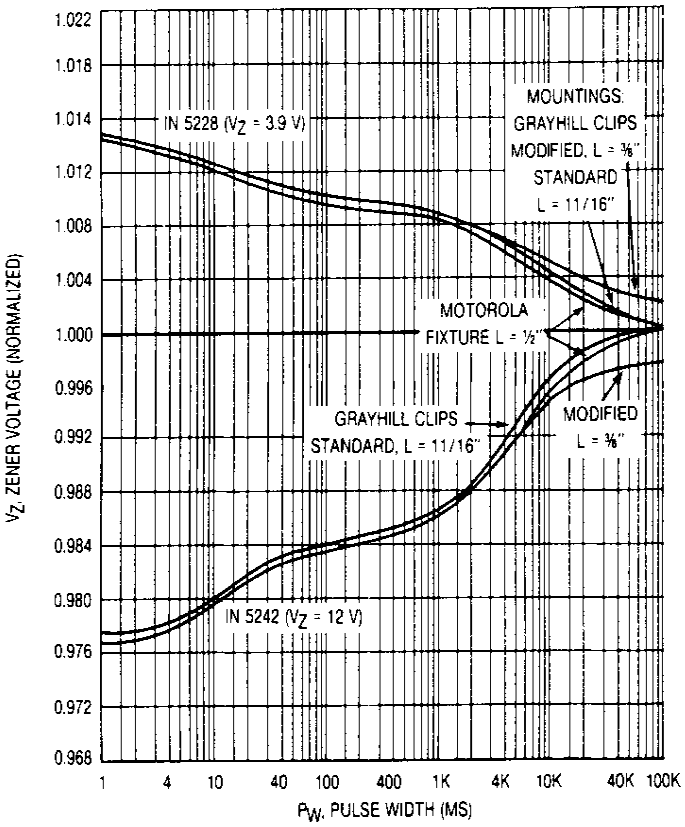
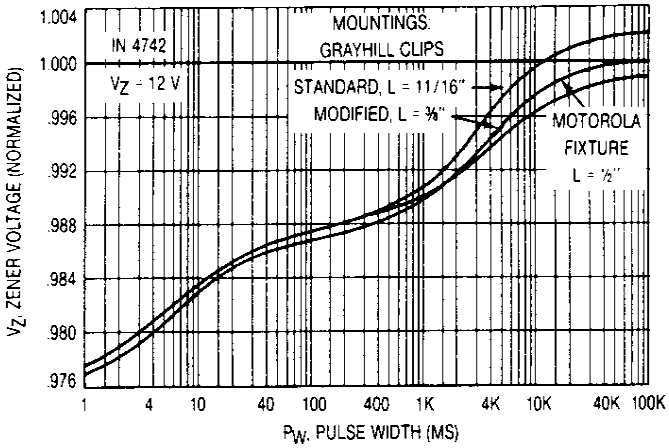


FIGURE 13 — DO-41 (GLASS) 1 WATT DEVICE



Mounting Fixtures

FIGURE 14 — STANDARD GRAYHILL CLIPS

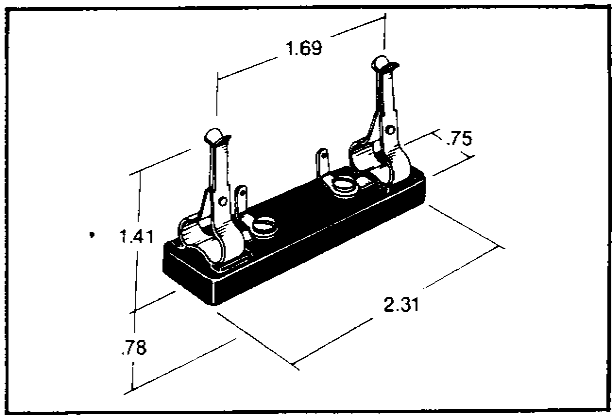


FIGURE 15 — FINAL TEST FIXTURE

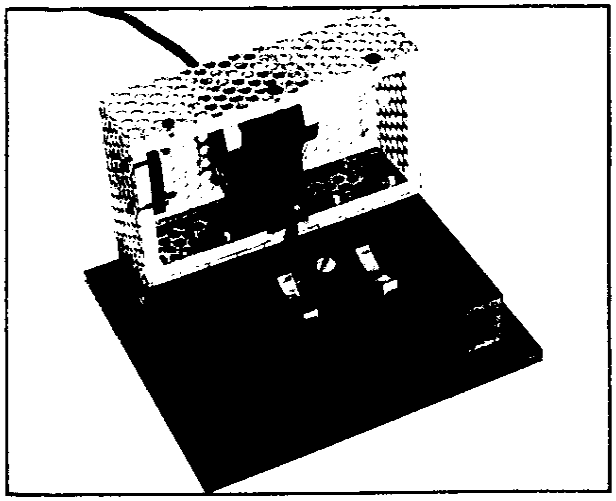
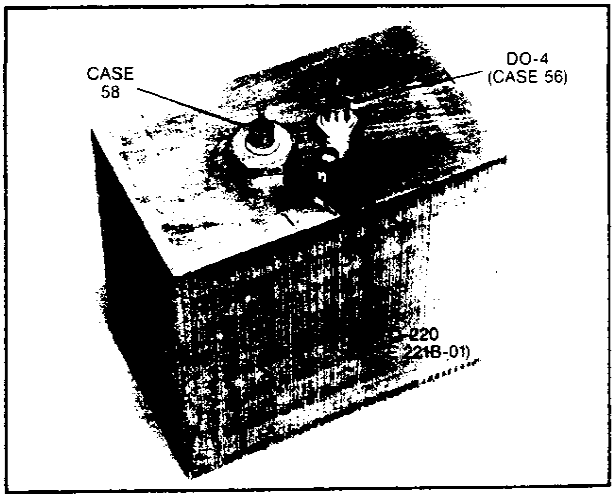


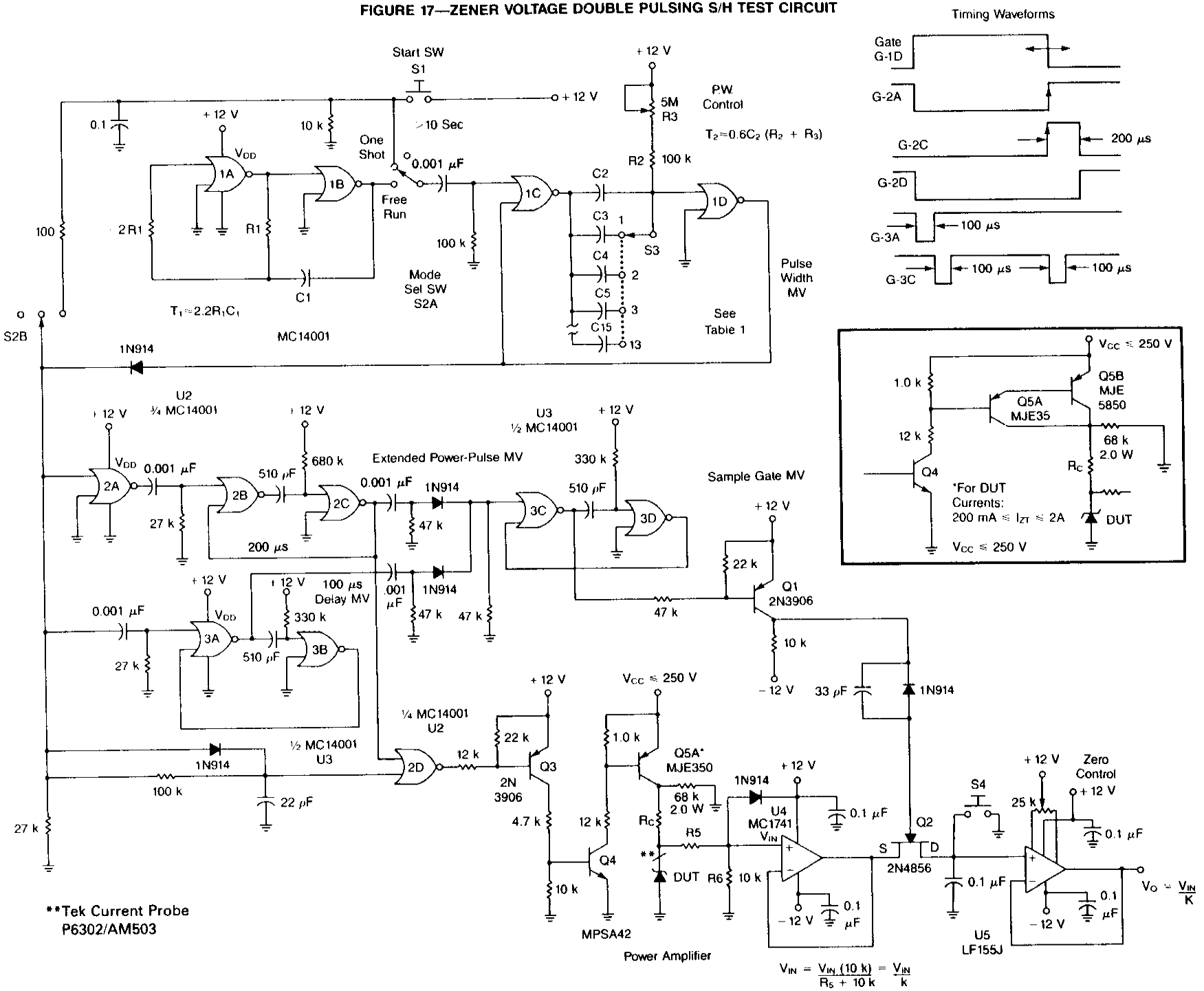
FIGURE 16 — ALUMINUM BLOCK
2⅜" x 3⅝" x 4"



ClibPDF - www.fastio.com

CMOS PDF - www.fastio.com

FIGURE 17—ZENER VOLTAGE DOUBLE PULSING S/H TEST CIRCUIT



APPENDIX A
Recommended Incoming Inspection Procedures
Zener Voltage Testing
Pulsed versus Thermal Equilibrium

This section is primarily for use of incoming inspection groups. The subject covered is the measurement of zener voltage (V_Z) and the inherent difficult of establishing correlation between supplier and buyer when using pulsed test techniques. This difficulty, in part, is due to the interpretation of the data taken from the variety of available testers and in some cases even from the same model types. It is therefore, our intent to define and re-establish a standardized method of measurement to achieve correlation no matter what test techniques are being used. This standardization will guarantee your acceptance of good product while maintaining reliable correlation.

DEFINITION OF TERMS

Temperature Coefficient (TC):

The temperature stability of zener voltages is sometimes expressed by means of the temperature coefficient (TC). This parameter is usually defined as the percent voltage change across the device per degree centigrade, or as a specific voltage change per degree centigrade. Temperature changes during test are due to the self heating effects caused by the dissipation of power in the zener junction. The V_Z will change due to this temperature change and will exhibit a positive or negative TC, depending on the zener voltage. Generally, devices with a zener voltage below five volts will have a negative TC and devices above five volts will exhibit a positive TC.

Thermal Equilibrium (TE)

Thermal equilibrium (TE) is reached when the diode junction temperature has stabilized and no further change will occur. In thermal equilibrium, the heat generated at the junction is removed as rapidly as it is created, hence, no further temperature changes.

MEASURING ZENER VOLTAGE

The zener voltage, being a temperature dependent parameter, needs to be controlled for valid V_Z correlation. Therefore, so that a common base of comparison can be established, a reliable measure of V_Z can only occur when all possible variables are held constant. This common base is achieved when the device under test has had sufficient time to reach thermal equilibrium (heat sinking is required to stabilize the lead or case temperature to a specified value for stable junction temperatures). The device should also be powered from a constant current source to limit changes of power dissipated and impedance.

All of the above leads us to an understanding of why various pulse testers will give differing V_Z readings; these differences are, in part, due to the time duration of test (pulse width), duty cycle when data logging, contact resistance, tolerance, temperature, etc. To resolve all of this, one only needs a reference standard to compare their pulsed results against and then adjust their limits to reflect those differences. It should be noted that in a large percentage of applications the zener diode is used in thermal equilibrium.

Motorola guarantees all of it's axial leaded zener products (unless otherwise specified) to be within specification ninety (90) seconds after the application of power while holding the lead temperatures at 30 ± 1°C, ⅜ of an inch from the device body, any fixture that will meet that criteria will correlate. 30°C was selected over the normally specified 25°C because of its ease of maintenance (no environmental chambers required) in a normal room ambient. A few degrees variation should have negligible effect in most cases. Hence, a moderate to large heat sink in most room ambients should suffice.

Also, it is advisable to limit extraneous air movements across the device under test as this could change thermal equilibrium enough to affect correlation.

SETTING PULSED TESTER LIMITS

Pulsed test techniques do not allow a sufficient time for zener junctions to reach TE. Hence, the limits need to be set at different values to reflect the V_Z at lower junction temperatures. Since there are many varieties of test systems and possible heat sinks, the way to establish these limits is to actually measure both TE and pulsed V_Z on a serialized sample for correlation.

The following examples show typical delta changes in pulsed versus TE readings. The actual values you use for pulsed conditions will depend on your tester. Note, that there are examples for both positive and negative temperature coefficients. When setting the computer limits for a positive TC device, the largest difference is subtracted from the upper limit and the smallest difference is subtracted for the lower limit. In the negative coefficient example the largest change is added to the lower limit and the smallest change is added to the upper limit.

Motorola Zeners

- Thermal equilibrium specifications:
  V_Z at 10 mA, 9.0 V minimum, 11.0 V maximum:
  (Positive TC)

TE	Pulsed	Difference
9.53 V	9.45 V	−0.08 V
9.35 V	9.38 V	−0.07 V
9.46 V	9.83 V	−0.08 V
9.56 V	9.49 V	−0.07 V
9.50 V	9.40 V	−0.10 V

Computer test limits:
Set V_Z max. limit at 11.0 V − 0.10 V = 10.9 V
Set V_Z min. limit at 9.0 V − 0.07 V = 8.93 V

- Thermal equilibrium specifications:
  V_Z at 10 mA, 2.7 V minimum, 3.3 V maximum:
  (Negative TC)

TE	Pulsed	Difference
2.78 V	2.83 V	−0.05 V
2.84 V	2.91 V	−0.07 V
2.78 V	2.84 V	+0.05 V
2.86 V	2.93 V	−0.07 V
2.82 V	2.87 V	+0.05 V

Computer test limits:
Set V_Z min. limit at 2.7 V + 0.07 V = 2.77 V
Set V_Z max. limit at 3.3 V + 0.05 V = 3.35 V

ClibPDF - www.fastio.com