MOTOROLA
Semiconductor Products Inc.

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Application Note

DESIGNING WITH TMOS POWER MOSFETs

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The advent of vertical current control in MOS Field Effect Transistors has brought their design advantages, well known to IC and Small Signal circuit designers, to the world of power control. The historical reasons for planar MOSFETs being impractical for power control, such as high on-resistances, long channel lengths, all terminals on the top of the die and huge die sizes with accompanying large capacitances, have all been alleviated.

Several processes with names such as VMOS, UMOS, DMOS, etc., have been developed to attain vertical current flow. The majority of suppliers, with trade names such as HEXFET, MOSPOWER, SIPMOS, etc., use the DMOS process for their product. Motorola has developed a process called TMOS for its power MOSFET line, which is a refinement of a double diffused process (vertical DMOS) that results in low "ON" resistance, has achieved excellent die utilization and has produced devices with breakdown voltages in excess of 1,000 volts.

The TMOS cell structure, illustrated in Figure 1, is duplicated thousands of times on a single chip to reduce on-resistance and increase current handling capability.

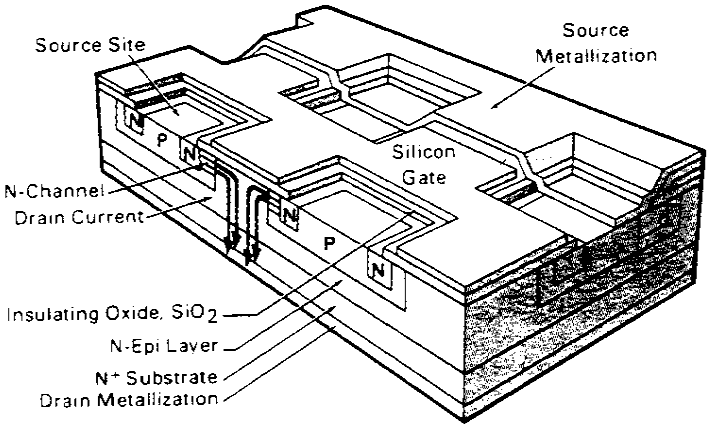

FIGURE 1 — Cross Section of TMOS Cell

Note that the current flow as shown by the vertical arrows is from the drain, then through a short distance horizontally to the source, thus the acronym "T"MOS has been adopted for the Motorola process.

A brief description of the TMOS process and structure will help circuit designers understand the electrical parameters of the device. An N-channel, enhancement mode TMOS process begins with an N epitaxial layer grown on an N^+ substrate. P^- regions are diffused into the N^- epi layer and then N^- regions are diffused inside the P^- regions. Next a layer of SiO_2 is grown to form the gate isolation and a layer of polycrystalline silicon doped with phosphorous is deposited to form the gate. Finally gate and source metallization is deposited to provide electrical contacts.

This application note is intended to be an introduction to the Motorola TMOS power MOSFET for both those that are and are not familiar with designing with bipolars. Those that are will have a greater appreciation of the trade-offs involved when comparing the two technologies and will be able to understand how to utilize TMOS FETs quite readily. For those that are fairly unfamiliar with bipolars, this article will show that power MOSFETs can provide excellent performance with relatively simple gate drive circuitry.

To facilitate the identification of the Motorola device numbers referred to herein, a brief explanation of Motorola's numbering system is in order. The MTM prefix indicates a metal TO-204 (formerly TO-3) package, MTP refers to a plastic TO-220AB package and MTH refers to the plastic TO-218 AC package. (Other packaging will soon be available.) The next number, whether it be one or two digits, denotes the current rating. Following the current rating, the N or P identifies the channel polarity. Finally, the last two, and sometimes three, digits give the voltage rating divided by ten. As an example, the MTM4N45 is a 4.0 A, 450 V, N-channel device in the metal TO-204 case.

COMPARING AND CONTRASTING BIPOLARS AND POWER MOSFETs

A quick look at Figures 2 and 3 indicates that the bipolar NPN and the N-channel TMOS FET have some very basic similarities; both perform roughly the same function. (Figures 2 and 3 will be discussed in greater

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detail later.) The most marked difference is that the gate of the MOSFET is voltage driven whereas the base of the bipolar is current driven. Otherwise the symbols denoting device voltages, currents, etc. are logically analogous as depicted in Table 1.

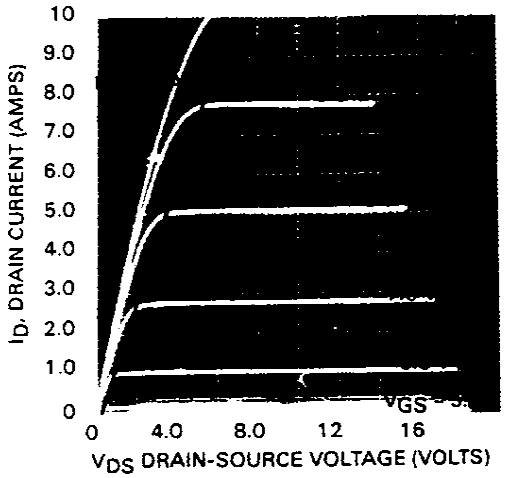


FIGURE 2 — I_D-V_{DS} Transfer Characteristics of MTP8N15
Region A is called the Ohmic, On, Constant Resistance or Linear Region
Region B is called the Active, Constant Current, or Saturation Region

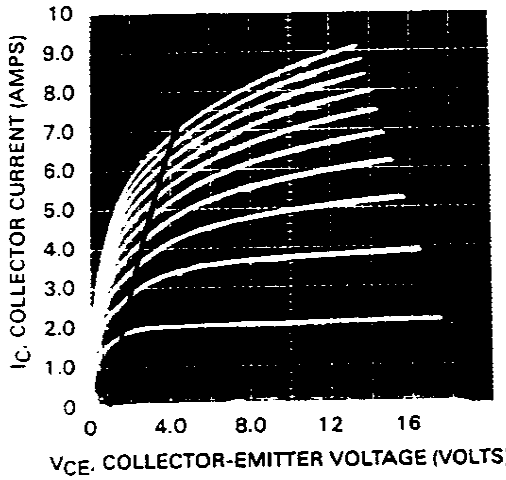
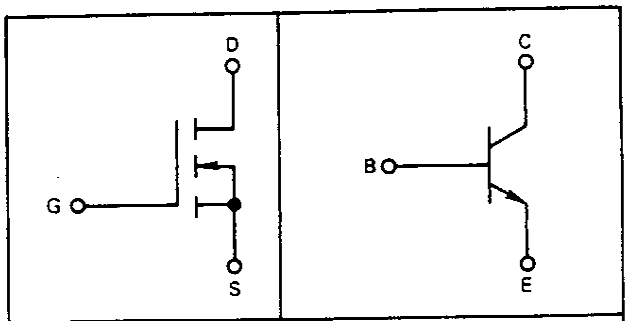


FIGURE 3 — I_C-V_{CE} Transfer Characteristics of MJE15030
(NPN, I_C Continuous = 8.0 A, V_{CEO} = 150 V)
Region A is the Saturation Region
Region B is the Linear or Active Region

When contrasting the two device technologies, it must be mentioned that the bipolar is a minority carrier device (holes in an NPN device) and the MOSFET is a majority carrier device (electrons in an N-channel FET). The type of carrier determines the amount of charge that needs to be transferred to the gate or base of the device to effect turn-on. This accounts for two major differences in the [illegible] characteristics.



TMOS FET	BIPOLAR TRANSISTOR
Drain	Collector
Source	Emitter
Gate	Base
$V_{BR(DSS)}$	$V_{BR(CES)}$
V_{DGO}	V_{CBO}
I_D	I_C
I_{DSS}	I_{CES}
I_{GSS}	I_{EBO}
$V_{GS(th)}$	$V_{BE(on)}$
$V_{DS(on)}$	$V_{CE(sat)}$
C_{iss}	C_{ib}
C_{oss}	C_{ob}
g_{fs}	h_{FE}
$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$	$r_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$

TABLE 1 — MOSFET and Bipolar Transistor Similarities

First, because less charge needs to be supplied to the gate to initiate turn-on, the MOSFET switching times, both on and off, are much faster. The relatively short delay, rise and fall times associated with the MOSFET are mainly due to charging or discharging the parasitic capacitances. The storage times associated with the minority carriers in the bipolar are absent in power MOSFETs. Second, the manner in which charge is supplied to the base of the bipolar transistor results in more current carriers and a lower collector to emitter voltage drop. Therefore, the saturation voltage of a bipolar is usually lower than the "ON" voltage of a power MOSFET of equivalent die size. However, low voltage, low on-resistance MOSFETs can be an exception to this rule. (On-resistance, or $r_{DS(on)}$, is the equivalent drain-source resistance when the MOSFET is fully turned on.)

When designing a power MOSFET, there are tradeoffs made between obtaining low on-resistance and high drain-source breakdown voltage. For the same die size, on-resistance increases roughly in proportion to the breakdown voltage squared. While this makes fabrication of low $r_{DS(on)}$ devices with breakdown voltages exceeding 1,000 volts difficult, it also makes practical low voltage devices with very low on-resistances. These low voltage, low $r_{DS(on)}$ devices, such as the MTM25N06 and the MTM35N06, have maximum $r_{DS(on)}$ ratings of 0.080 ohms and 0.055 ohms respectively. A 25 A drain current in the

MTM35N06 would produce a maximum $V_{DS(on)}$ of 1.375 volts, which is similar to the $V_{CE(sat)}$ of a comparably sized bipolar and lower than that of a Darlington.

Advantages of Power MOSFETs

Two of the most significant advantages that MOSFETs have over bipolars are simplified drive circuitry and faster switching. Power MOSFETs, therefore, are better suited for applications requiring efficient high frequency operation and/or simplified drive circuitry such as switched-mode power supplies, motor controls, audio amplifiers, battery chargers and automotive applications.

The gate drive circuitry of the voltage controlled MOSFET is generally less complex than the base drive circuit of the current controlled bipolar. The only current that needs to be supplied to the gate is that required to charge the input capacitances. Although rapid switching requires good current source and sink capabilities, the MOSFET needs very little gate current to allow it to remain in either the on, off or an intermediate state. Once the parasitic capacitances are charged, only leakage currents on the order of nanoamperes need to be supplied. Unlike the base drive of a bipolar, the MOSFET's gate drive is simpler because it is more independent of the drain current.

Often a CMOS or TTL chip can drive the MOSFET directly, especially if high switching speeds are not critical. TMOS Power FET Design Tips TDT102 and TDT103 describe specific gate drive circuits and highlight the gate drive considerations for switching power MOSFETs with excellent speed. These simpler drive circuits often translate into lower total piece-parts cost, greater reliability and reduced size and weight.

The main advantage of the MOSFET's fast switching capability is not necessarily that they can turn on a load rapidly. Often the advantage is that when they do turn on rapidly, less time is spent in the high power dissipation switching interval. Figure 4a compares the magnitudes of the switching and conduction losses and underscores the importance of maximizing switching speeds to increase efficiency. Since bipolars often switch an order of magnitude slower, their switching losses are significantly greater. At higher frequencies, the difference is often great enough to more than offset the higher "ON", or conduction, losses exhibited by power MOSFETs. So great is the improvement in switching efficiencies that new design capabilities have been created, as evidenced by switched-mode power supplies being operated above 150 kHz.

A third significant advantage is that MOSFETs have a greater Safe Operating Area (SOA) since they are not as susceptible as bipolars to hotspotting or current crowding. A brief description of the power MOSFET structure will clarify this point. A power MOSFET die actually contains many hundreds or even thousands of transistors in parallel. If one portion of the die has a slightly lower on-resistance, at turn-on that section will briefly carry more than its share of the current. The localized heating caused by the current imbalance will increase the temperature of that portion of the die. Due

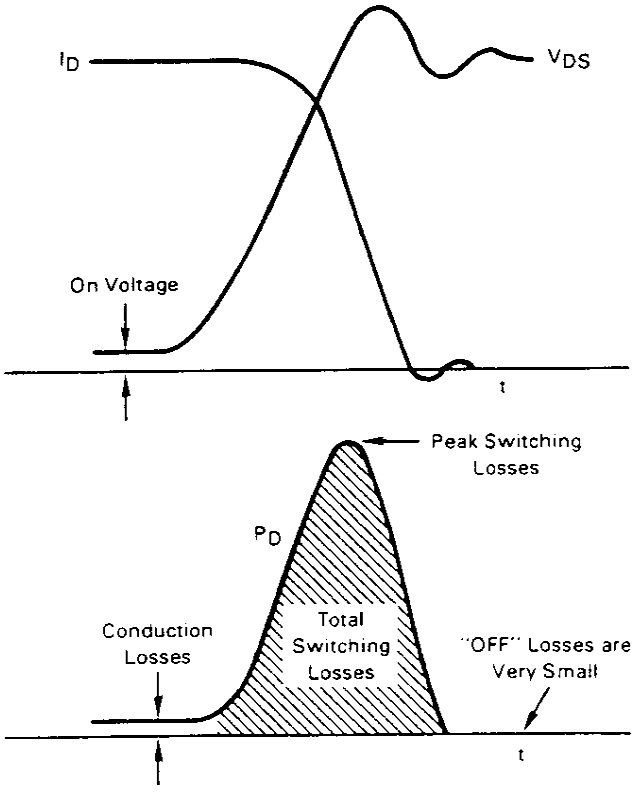


FIGURE 4a — Comparison of the Magnitudes of Conduction and Switching Losses

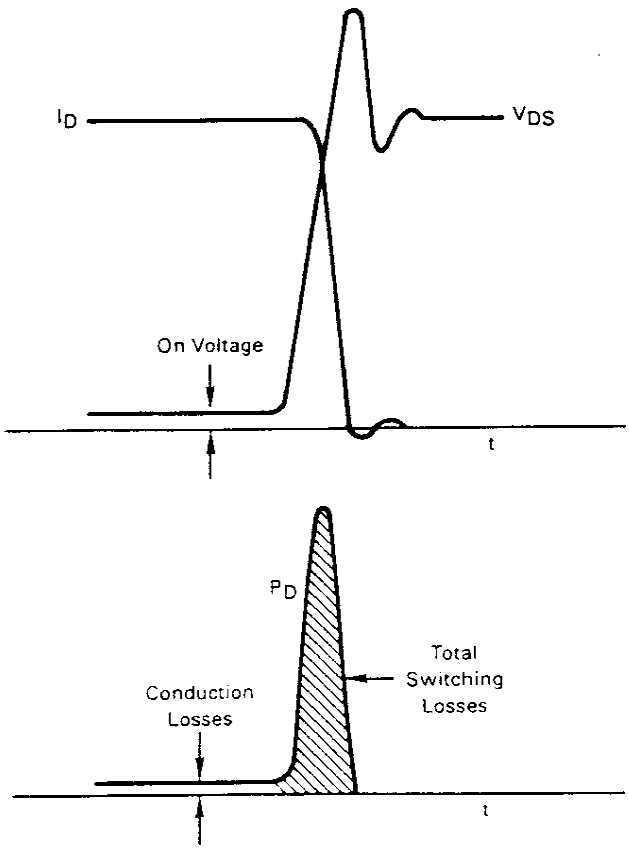


FIGURE 4b — Switching Losses Decrease with Faster Switching

to the positive temperature coefficient of r_{DS}, the localized resistance increases causing a decrease in the current in that region. In this manner power MOSFETs inherently share current as opposed to the current hogging or hot-spotting seen in bipolars. Since the entire chip shares the current, it is less likely that enough localized heat is generated to cause hotspotting.

The same argument supporting the concept of current sharing between regions on the same die can be extended to include the paralleling of multiple devices. If one device in a group of paralleled FETs has a lower on-resistance, that device will initially carry more than its share of current, heat up, see an increase in r_{DS}, and then carry a more equitable share of the total current. While these tendencies are definitely observable, the effect of the positive temperature coefficient of $r_{DS(on)}$ on the degree of current sharing is sometimes overestimated. Because the coefficient is small, the difference between junction temperatures in the low and high $r_{DS(on)}$ devices must be appreciable to force a high degree of current sharing.

Although the tendency of MOSFETs to current share is not overwhelming, its presence does promote stability in paralleled devices. The opposite is true of bipolars, which have a negative temperature coefficient of $V_{CE(sat)}$. Because the coefficient is negative, bipolars tend to current hog when operated in parallel. Often this tendency must be compensated for by employing emitter ballasting resistors or current sensing feedback loops that are usually unnecessary for power MOSFETs.

In contrast, the keys to successful paralleling of power MOSFETs are fairly easy to implement. Maintaining circuit symmetry and damping potential self oscillations with small resistances in series with each gate are two of the most important considerations.

The current sharing characteristic not only tends to keep the chip temperature uniform, gives the device rugged current capabilities and makes paralleling devices easier, but also improves the SOA characteristics of the devices. Surprisingly, the current sharing advantage of the power MOSFET shows up in the low current, high voltage portion of the SOA curves where the bipolar must be derated due to second breakdown (Figure 5). The reason for this is that bipolars are more likely to hotspot at higher voltages due to the higher electric fields reducing the effective chip area. Figure 5 indicates that except for the maximum voltage and current limits, the Forward Biased Safe Operating Area, or FBSOA, of the MOSFET is limited only by the package thermal limit and not by second breakdown due to current crowding as seen in bipolars.

TRANSFER CHARACTERISTICS

Comparison of Bipolar and TMOS

As indicated in Figures 2 and 3, the transfer characteristics of the power MOSFET and the bipolar can be divided similarly into two basic regions. The figures also show the numerous and often confusing terms assigned to those regions. To avoid possible confusion, this paper will refer to the MOSFET regions as the "on" (or "ohmic") and "active" regions and the bipolar regions as the "saturation" and "active" regions.

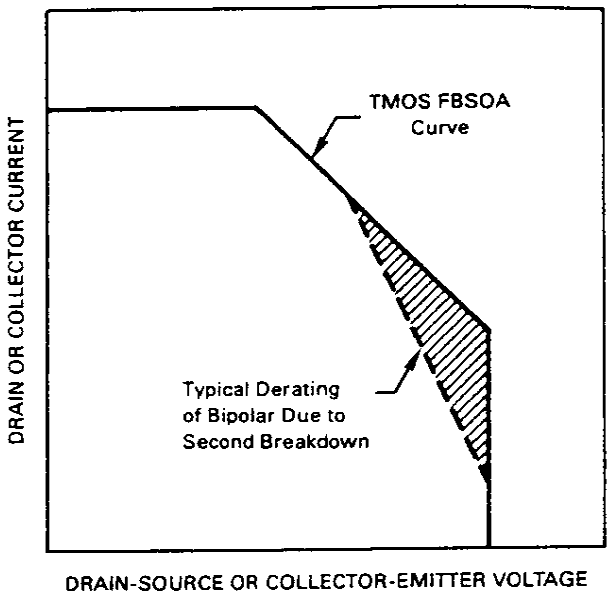


FIGURE 5 — Comparison of TMOS and Bipolar FBSOA Curves

One of the three obvious differences between Figures 2 and 3 is that the family of curves for the power MOSFET is generated by changes in gate voltage and not by base current variations. A second difference is that the slope of the curve in the bipolar saturation region is steeper than the slope in the ohmic region of the power MOSFET indicating that the on-resistance of the MOSFET is higher than the effective on-resistance of the bipolar.

The third major difference between the transfer characteristics is that in the active regions the slope of the bipolar curve is steeper than the slope of the TMOS curve, making the MOSFET a better constant current source. This phenomena occurs because as the drain-source voltage is increased and the device enters the active region, the channel carriers achieve their maximum drift velocity and the current no longer can increase appreciably.

On-Resistance

The on-resistance, or $r_{DS(on)}$, of a power MOSFET is an important figure of merit because it determines the amount of current the device can handle without excessive power dissipation. When switching the MOSFET from off to on, the drain-source resistance falls from a very high value to $r_{DS(on)}$, which is a relatively low value. To minimize $r_{DS(on)}$ the gate voltage should be large enough for a given drain current to maintain operation in the ohmic region. Data sheets show the transfer characteristics and give this information. As Figure 6 indicates, increasing the gate voltage above 15 volts has a diminishing effect on lowering on-resistance (especially in high voltage devices) and increases the possibility of spurious gate-source voltage spikes exceeding the maximum gate voltage rating of 20 volts. Somewhat like driving a bipolar deep into saturation, unnecessarily high gate voltages will increase turn-off time because of the

excess charge stored in the input capacitance. All Motorola TMOS FETs will conduct the rated continuous drain current with a gate voltage of 10 volts.

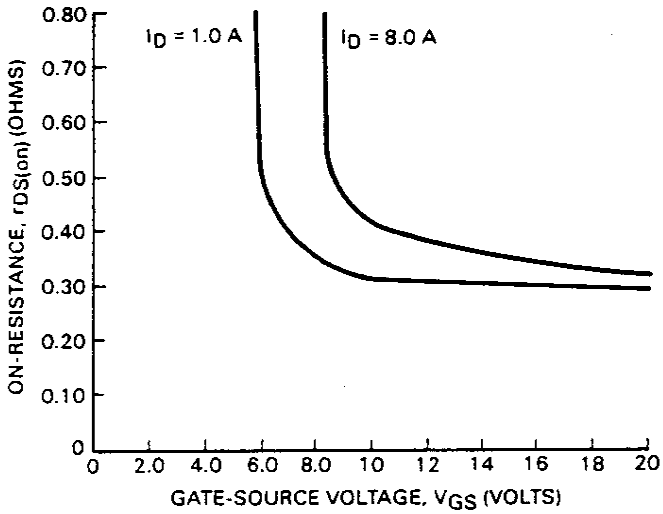


FIGURE 6 — Variation of $r_{DS(on)}$ with V_{GS} and I_D for MTP8N15

As the drain current rises, especially above the continuous rating, the on-resistance also increases. Another important relationship, which is addressed later with the other temperature dependent parameters, is the effect that temperature has on the on-resistance. The combination of the effects of various drain currents and temperatures is illustrated in the data sheets and shown in Figure 7.

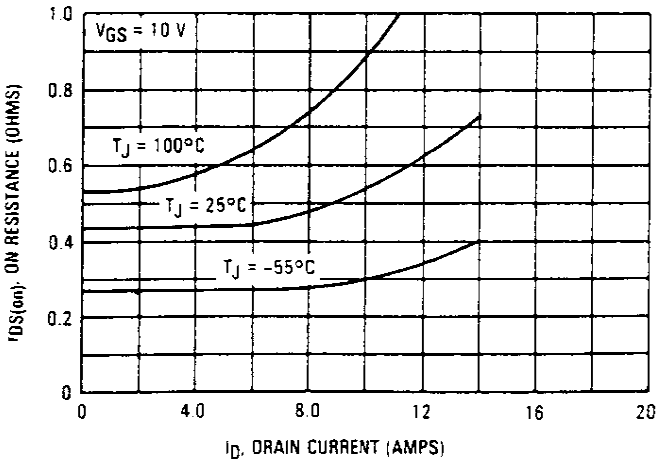


FIGURE 7 — Variation of $r_{DS(on)}$ with Drain Current and Temperature for MTM8N15

Transconductance

Since the transconductance, or g_{fs}, denotes the gain of the MOSFET, much like beta represents the gain of the bipolar, it is an important parameter when the device is operated in the active, or constant current, region. Defined as the ratio of the change in drain current corresponding to a change in gate voltage ($g_{fs} = dI_D/dV_{GS}$), the transconductance varies with operating conditions and temperature as seen in Figure 8. The value of g_{fs} specified in the Motorola Designer's Data Sheets is determined from the active portion of the V_{DS}–I_D transfer characteristics where a change in V_{DS} no longer significantly influences g_{fs}. Typically the transconductance rating is specified at half the rated continuous drain current and at a V_{DS} of 15 V.

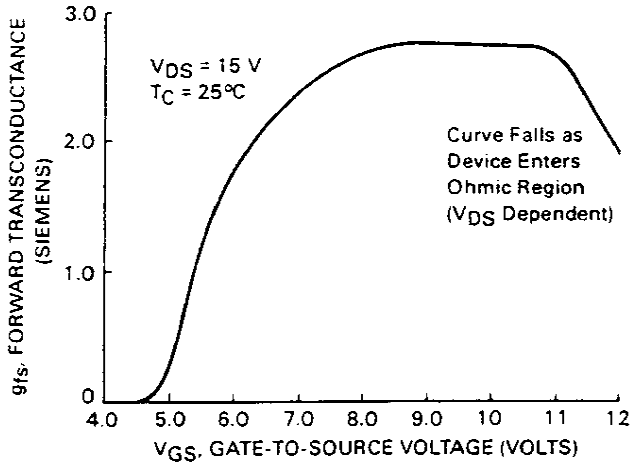


FIGURE 8 — Small Signal Transconductance versus V_{GS} of MTP8N10

For those designers only interested in switching the power MOSFET between the on and off states the transconductance is often an unused parameter. Obviously when the device is switched fully on, the transistor will be operating in its ohmic region where the gate voltage will be high. In that region, a change in an already high gate voltage will do little to increase the drain current; therefore, g_{fs} is almost zero.

Threshold Voltage

Threshold Voltage, $V_{GS(th)}$, is the lowest gate voltage at which a specified small amount of drain current begins to flow. Motorola normally specifies $V_{GS(th)}$ between 2.0 and 4.5 volts and at an I_D of one milliampere. Device designers can control the value of the threshold voltage and target $V_{GS(th)}$ to optimize device performance and practicality. A low threshold voltage is desired so the TMOS FET can be controlled by low voltage chips such as CMOS and TTL. A low value also speeds switching because less current needs to be transferred to charge the parasitic input capacitances. But the threshold voltage can be too low if noise can trigger the device or designers have difficulty dealing with leakage currents from previous stages. Also, a positive-going voltage transient on the drain can be coupled to the gate by the gate-to-drain parasitic capacitance and can cause spurious turn-on in a device with a low $V_{GS(th)}$.

SAFE OPERATING AREAS

To provide the designer with Safe Operating Area information for the various modes of operation the TMOS transistor may encounter, three different Safe Operating Areas are defined on the TMOS data sheets. To ensure long term reliability, power MOSFETs must be operated exclusively inside their published SOA curves. In addition to the Forward Biased Safe Operating Area, or FBSOA (often referred to as simply SOA), also shown are the Switching SOA, or SSOA, and the Reverse Bias SOA, or RBSOA. Beginning with the FBSOA curve, their intended uses will be discussed.

The FBSOA curve defines the maximum drain voltages and currents the device can safely handle when forward biased, or while it is on or being turned on. Of the three or perhaps four limits dictated by the boundaries of the FBSOA curve, the most unforgiving is the maximum drain-source rating which is indicated by boundary D in Figure 9. If this rating is exceeded, even momentarily, the device can be damaged permanently. Thus, precautions should be taken if there may be transients in the drain supply voltage.

The second limit, shown as Line C in Figure 9, is the package thermal limit and is dependent on the junction to case thermal resistance and the maximum allowable junction temperature. The purpose of this portion of the curve is to ensure that the junction temperature does not exceed the 150°C maximum rating. Since the transient thermal resistance decreases dramatically for shorter pulse durations, the power handling capability increases accordingly. For example, the MTM5N20, which is rated at 75 W, can dissipate 1300 W during a single 100 μs pulse at a case temperature of 25°C. Figure 10 shows that the normalized transient thermal resistance, r(t), at 100 μs is about 0.057, resulting in a worst-case transient thermal resistance of 0.095°C/W. From $\Delta T_{JC} = R_{\theta JC} P_D$, where $\Delta T_{JC} = T_{J(max)} - T_C = 150-25°C$; the developed power can be about 1300 W without exceeding the maximum rated junction temperature of 150°C.

Maximum allowable drain current is also time or pulse width dependent and defines the third boundary of the FBSOA curve, represented by Line B. The limit is determined by the bonding wire diameter, the size of the source bonding pad, device characteristics and, again, thermal resistance. Even though MOSFETs show rugged overcurrent capabilities, devices should not conduct more than their rated drain current for a given pulse duration. This includes transient currents such as the high in-rush current drawn by a cold incandescent lamp or the reverse recovery current required by a diode.

The fourth boundary, Line A, is fixed by the drain-to-source on-resistance and limits the current at low drain source voltages. Simply a manifestation of Ohm's Law, the limitation states that with a given on-resistance, current is limited by the applied voltage. The boundary does not describe a linear relationship, however, because the on-resistance increases gradually with increasing current.

An RBSOA curve defines the peak drain voltage and current limitations during clamped inductive turn-off. An inductive load is used because it causes the greatest turn-off stress, but it must be clamped so as not to avalanche the MOSFET with an uncontrolled drain-source "flyback voltage". Since power MOSFETs do not need to be derated for RBSOA, both turn-on and turn-off safe operating areas are bounded by the maximum pulsed drain current, I_{DM}, and the maximum drain-source voltage, V_{DSS}. On the TMOS Designer's

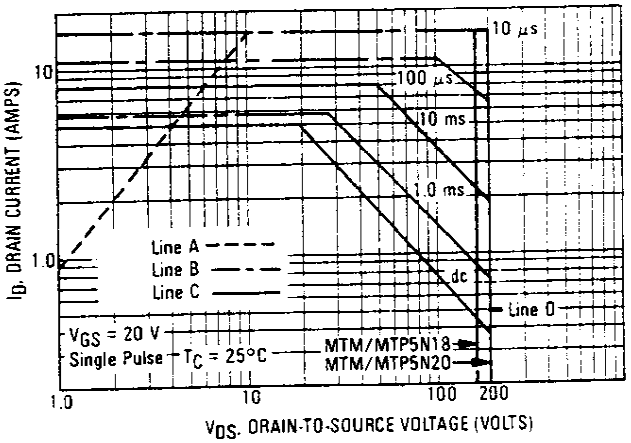


FIGURE 9 — FBSOA of MTM5N20

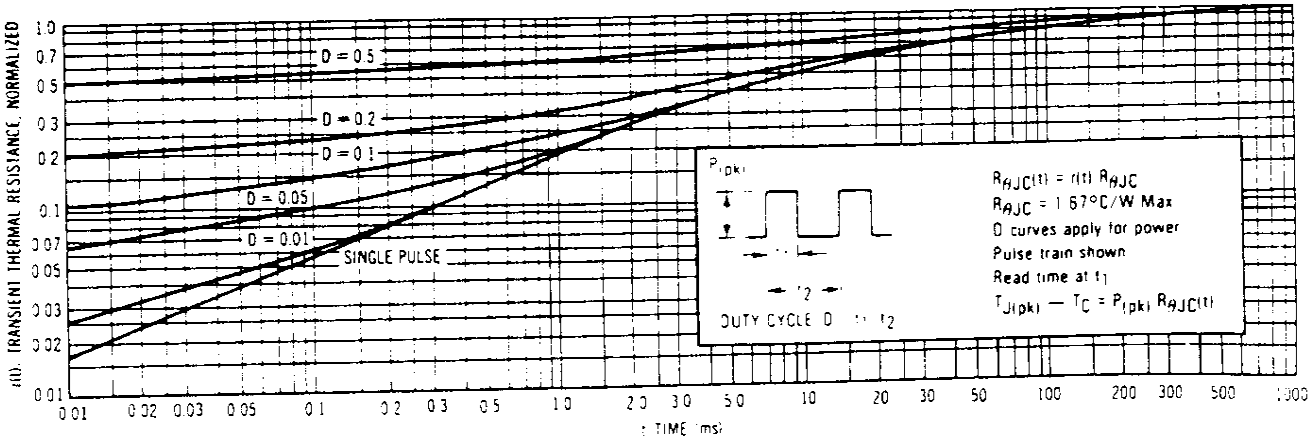


FIGURE 10 — Thermal Response Curve of MTM5N20

Data Sheets, these turn-on and turn-off peak voltage and current limitations are combined into one curve, the Switching Safe Operating Area, or SSOA. Figure 11, the SSOA of the MTM5N20, is applicable for both turn-on and turn-off of devices with rise and fall times of less than one microsecond.

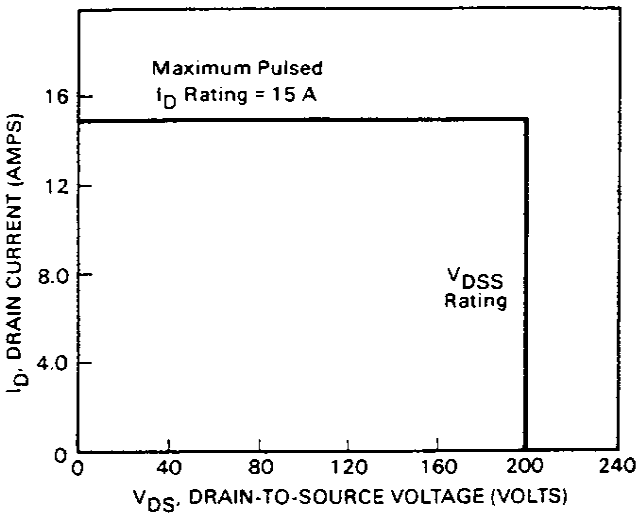


FIGURE 11 — Maximum Rated Switching Safe Operating Area of MTM5N20

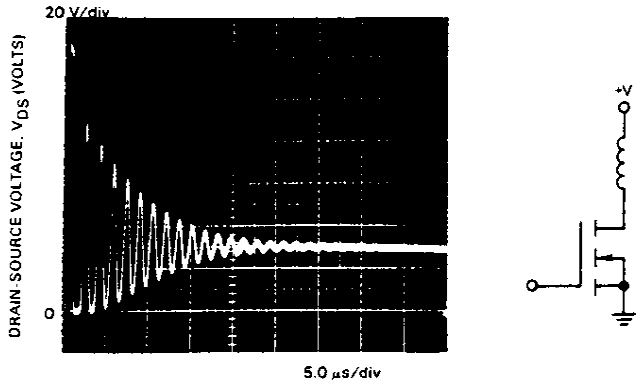


FIGURE 12 — V_{DS} Transient due to Unclamped Inductive Load

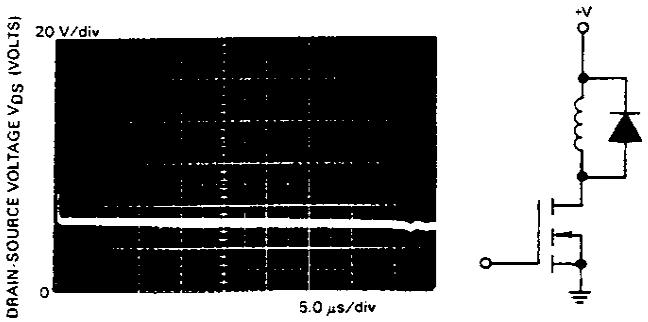


FIGURE 13 — V_{DS} Transient with Clamping Diode

PROTECTING THE POWER MOSFET

Protecting the Drain

The most common cause of failure in a power MOSFET is due to an excursion across an SOA boundary. A good portion of these failures are a result of exceeding the maximum rated drain source voltage, $V_{(BR)DSS}$. Drain voltage transients caused by switching high currents through load or stray inductances can force V_{DS} to exceed $V_{(BR)DSS}$ and may contain enough energy to destroy the device if it begins to avalanche. Therefore, allowing the device to go into avalanche is not recommended for TMOS power FETs. Transients on the drain supply voltage can also destroy the power MOSFET.

Fortunately, if there is any danger of these destructive transients, the solutions to the problem are numerous and fairly simple. Figure 12 illustrates a FET switching an inductive load in a circuit which provides no protection from excessive flyback voltages. The accompanying waveform depicts the turn-off voltage transient due to the load and the parasitic lead and wiring inductance. The MTM20N10 experiences the unrecommended avalanche condition for about 300 ns at its breakdown voltage of 122 volts. One of the simplest methods of protecting devices from flyback voltages is to place a clamping diode across the inductive load. Using this method, the diode will clamp most, but not all, of the voltage transient. V_{DS} will still overshoot V_{DD} by the sum of the effects of the forward recovery characteristic of the diode, the diode lead inductance and the parasitic series inductance as shown in Figure 13.

If the series resistance of the load is small compared to its inductance, a simple diode clamp may allow current to circulate through the load-diode loop for a significant amount of time after the MOSFET is turned off. When this lingering current is unacceptable, a resistor can be inserted in series with the diode at the expense of increasing the peak flyback voltage seen at the drain.

Protecting the drain-source from voltage transients with a zener diode, which is a wide band device, is another simple and effective solution. Except for the effects of the lead and wiring inductances and the very short forward recovery time, the zener will clip the voltage transient at its breakdown voltage. A transient with a slow $dv_{DS/dt}$ will be clipped completely while a transient with a rapid dv/dt might momentarily exceed the zener breakdown voltage. These effects are shown in Figure 14. Even though it is a very simple remedy, the zener diode is one of the most effective means of transient suppression. Obviously, the power rating of the zener should be scaled so that the clipped energy is safely dissipated.

Figure 15 shows an RC clamp network that suppresses flyback voltages greater than the potential across the capacitor. Sized to sustain a nearly constant voltage during the entire switching cycle, the capacitor absorbs energy only during transients and dumps that energy into the resistance during the remaining portion of the cycle. Component values may be computed by considering the power that the RC clamp network must absorb. From the power and the desired clamp voltage,

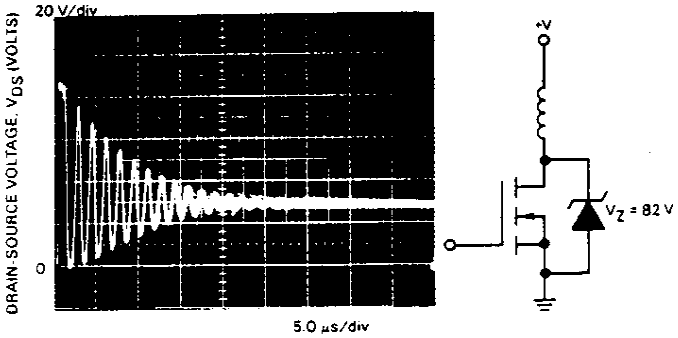


FIGURE 14 — V_{DS} Transient with Zener Clamp

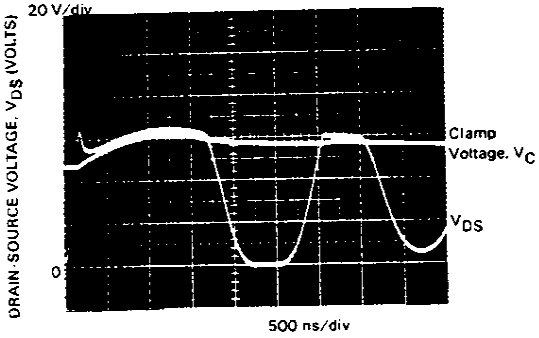
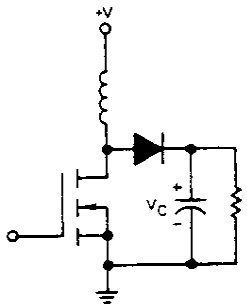


FIGURE 15a



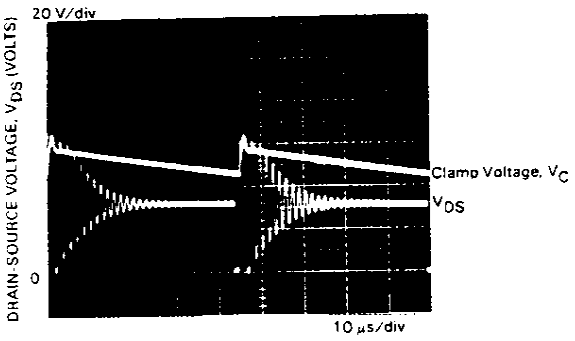


FIGURE 15b

FIGURE 15 — V_{DS} Transient and RC Clamp Voltage with RC Clamp Network

the resistance can be sized. Finally, the magnitude of the capacitance may be determined by relating the RC time constant to the period of the waveform.

As an example, a similar circuit has the following characteristics:

$L = 10\ \mu H$
$i = 3.0$ A (load current just before turn-off)
$f = 25$ kHz
$V_C = 60$ V (desired clamp voltage)

The power to be absorbed by the clamp network is:

$$P = 1/2\ L\ i^2 \times f = 1.125\ W$$

The component values can be determined:

$$\frac{V_C^2}{P} = R = 3.2K$$

$$\text{Let } \tau = RC = 5.0 \div f$$

$$C = 0.055\ \mu F$$

While this is a common and efficient circuit, the switching speeds of MOSFETs may produce transients that are too rapid to be attenuated by this method. If the flyback voltage reaches its peak during the first, say, 50 ns, the effectiveness of the circuit will be undermined due to the forward recovery characteristic of the clamp diode and any stray circuit inductance. It may be prudent in these cases to include a zener with a breakdown voltage slightly higher than the clamp voltage. When placed directly across the drain and source terminals, the lead lengths are short enough and the zener is fast enough to catch most transients. Since the zener's only purpose is to clip the initial flyback peak and not to absorb the entire energy stored in the inductor, the zener power rating can be smaller than that needed when one is used as the sole clamping element.

A fourth way to protect power MOSFETs from large drain-source voltage transients is to use an RC snubber network like that of Figure 16. Although it effectively reduces the peak drain voltage, the snubber network is not as efficient as a true clamping scheme. Whereas a clamping network only dissipates energy during the transient, the RC snubber also absorbs energy during portions of the switching cycle that are not overstressing the transistor. This configuration also slows turn-on due to the additional drain-source capacitance that must be discharged.

No matter which scheme is used, very rapid inductive turn-off can cause transients during the first tens of

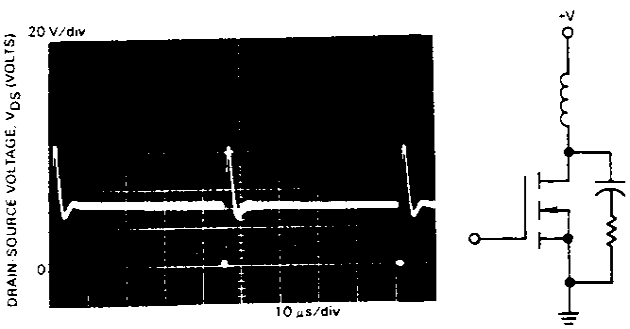


FIGURE 16 — V_{DS} Transient with RC Snubber

nanoseconds that may be overlooked unless a wide-band oscilloscope (B.W. ≥ 200 MHz) is used to observe the V_{DS} waveform.

Protecting the Gate

The gate of the MOSFET, which is electrically isolated from the rest of the die by a very thin layer of SiO_2, may be damaged if the power MOSFET is handled or installed improperly. Exceeding the 20 V maximum gate-to-source voltage rating, $V_{GS(max)}$, can rupture the gate insulation and destroy the FET. TMOS FETs aren't nearly as susceptible as CMOS devices to damage due to static discharge because the input capacitances of power MOSFETs are much larger and absorb more energy before being charged to the gate breakdown voltage. However, once breakdown begins, there is enough energy stored in the gate-source capacitance to ensure the complete perforation of the gate oxide. To avoid the possibility of device failure caused by static discharge, precautions similar to those taken with small-signal MOSFET and CMOS devices apply to power MOSFETs.

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

The gate of the power MOSFET could still be in danger after the device is placed in the intended circuit. If the gate may see voltage transients which exceed $V_{GS(max)}$, then the circuit designer should place a 20 V zener across the gate and source terminals to clamp any potentially destructive spikes. Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate threshold voltage and turn the device on.

POWER MOSFET GATE DRIVES

Driving a TMOS power transistor directly from a CMOS or open-collector TTL device is possible, but this circuit simplicity is obtained at the cost of slower switching speeds due to the charging current required by the parasitic input capacitance and the limited source and sink capabilities of these devices. From the output impedance of the gate drive circuit and the MOSFET input capacitance, or C_{iss}, an RC time constant can be obtained to roughly calculate the gate voltage rise or fall time (t_r or $t_f = 2.2\,RC_{iss}$). Since the MOSFET input capacitances vary significantly with the die area, a given gate drive will switch a smaller device such as the MTP5N06 more rapidly than the larger MTM15N40.

TTL Gate Drives

Driving the power MOSFET directly from a TTL device with a totem pole output and no additional circuitry is generally not an acceptable situation. In this case, the output voltage available is approximately 3.5 volts, which is insufficient to ensure the MOSFET will be driven into the ohmic region. A slightly more promising situation would be to use a pull-up resistor on the TTL output to utilize the entire 5.0 volt supply, but even the full 5.0 volts on the gate would not guarantee the MOSFET will conduct even half of its rated continuous drain current.

The open-collector TTL device, when used with a pull-up resistor tied to a separate 10 to 15 volt supply, can guarantee rapid gate turn-off and ensure sufficient gate voltage to turn the MOSFET fully on (Figure 17). Turn-on is not as rapid because the pull-up resistor must be sized to limit power dissipation in the lower TTL output transistor. However, when concerned about dynamic losses incurred while switching an inductive load, the gate fall time is more critical than the rise time due to the phase relationship between the drain current and drain-source voltage. Figure 18 shows a configuration providing faster turn-on, yet reducing power dissipation in the TTL device.

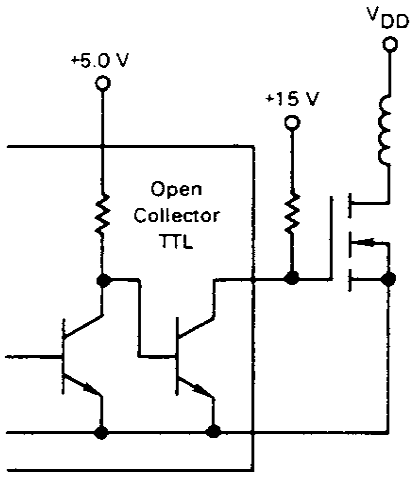


FIGURE 17 — Driving TMOS with Open Collector TTL

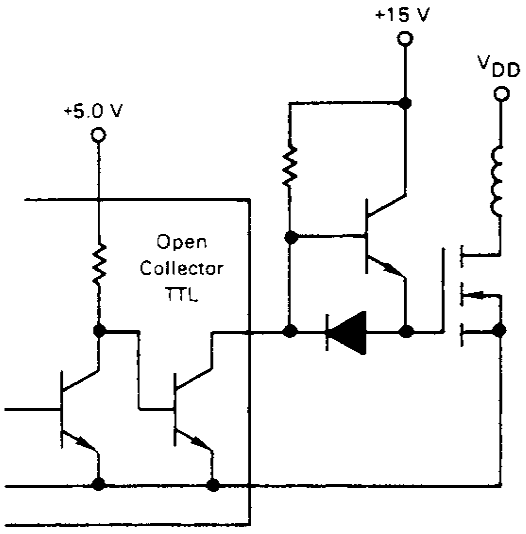


FIGURE 18 — Open Collector TTL-TMOS Interface for Faster Turn-on and Reduced Power Dissipation

When the lower transistor in the TTL output stage is turned on, shunting the MOSFET input capacitance to ground, modeling the bipolar as a saturated device may not be appropriate. The current sinking capabilities of TTL devices in the low output state is limited by the beta of the pull-down transistor and its available base current, which varies with product line and TTL family. Table II shows the current source and sink capabilities of various TTL families.

TABLE II — TTL Output Current Source and Sink Capabilities

	Output Drive	
Family	High (Source)	Low (Sink)
74LS00	0.4 mA	8.0 mA
7400	0.8 mA	16 mA
9000	0.8 mA	16 mA
74H00	1.0 mA	20 mA
74S00	1.0 mA	20 mA

Although the TTL peak current sinking capability might be twice the continuous rating, faster turn-off can be achieved by using an outboard transistor to clamp the gate to ground (Figure 19). In this configuration, the bipolars are operating as emitter followers. As such, they are never driven into saturation and their associated storage times do not significantly affect the switching frequency limit.

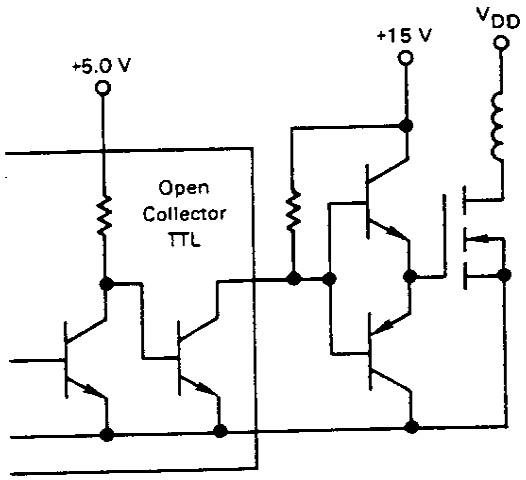


FIGURE 19 — Open Collector TTL Driving Complementary Emitter Follower

CMOS Gate Drives

Driving the power MOSFET directly from CMOS presents a different set of advantages and disadvantages. Perhaps most important, CMOS and power MOSFETs can be operated from the same 10 to 15 volt supply. A gate voltage of at least 10 volts will ensure the MOSFET is operating in its ohmic region when conducting its rated continuous current. This benefit allows the designer to directly interface CMOS and TMOS without any additional circuitry including external pull-up resistors. Again, however, circuit simplicity results in slower MOSFET switching due to the limited current source and sink capabilities of CMOS devices. Table III compares the output current capabilities of standard commercial CMOS gates to that of the CMOS buffers (MC14049, 14050). Note that while the current sinking capacity of the buffers is improved significantly over that of the standard CMOS gate, the current sourcing capacity is not. The figures in Tables II and III indicate the current at which the device can still maintain its output voltage within the proper logic level for a given logic state. As an illustration, with a V_{DS} of 15 V, a standard CMOS gate can typically source 8.8 mA in the HIGH state without its output falling below 13.5 volts.

If the switching speeds of CMOS buffers are not rapid enough, the discrete buffers suggested for use with TTL devices (Figures 18 and 19) can also be used to interface CMOS to TMOS. The only difference is the pull-up resistors are unnecessary for CMOS. Another difference in the two technologies that may affect the maximum switching frequency limit is that the TTL gates typically have faster switching times.

TABLE III — CMOS Current Source and Sink Capabilities

			B-Series Gates (MC14001CP)		CMOS Buffers (MC14049, 14050CP)	
		V_{DD}	Min (mA)	Typ (mA)	Min (mA)	Typ (mA)
Current Source Capability	V_{OH} = 2.5 V	5.0 V	-2.1	-4.2	-1.25	-2.5
	V_{OH} = 9.5 V	10 V	-1.1	-2.25	-1.25	-2.5
	V_{OH} = 13.5 V	15 V	-3.0	-8.8	-3.75	-10
Current Sink Capability	V_{OL} = 0.4 V	5.0V	0.44	0.88	3.2	6.0
	V_{OL} = 0.5 V	10 V	1.1	2.25	8.0	16
	V_{OL} = 1.5 V	15 V	3.0	8.8	24	40

Other Gate Drives

In certain situations pulse transformers are an effective means of driving the gate of a power MOSFET. They provide the isolation needed to drive bridge configurations or to control an N-Channel MOSFET driving a grounded load. One of the simplest examples of such a circuit is the first circuit in Table IV where the rise, fall, and delay times for this and the other circuits to be discussed are tabulated.

The diode in Circuit 1 is present simply to limit the flyback voltage appearing across the drive transistor Q1. A transformer turns ratio of one-to-one was chosen to provide an appropriate voltage at the secondary given the 15 volt primary supply voltage. A potential problem with this circuit is that the duty cycle influences the magnitude of V_{GS} because the volt-seconds product during the on and off intervals at the secondary must sum to zero. Figure 20 indicates that increasing the duty cycle decreases the maximum gate-source voltage. As the duty cycle increases above 33%, for the given primary voltage of 15 volts, the peak gate voltage falls below 10 volts and may eventually drop to a point where the device is no longer operating in the ohmic region. Increasing the primary voltage to 20 volts would increase the maximum allowable duty cycle.

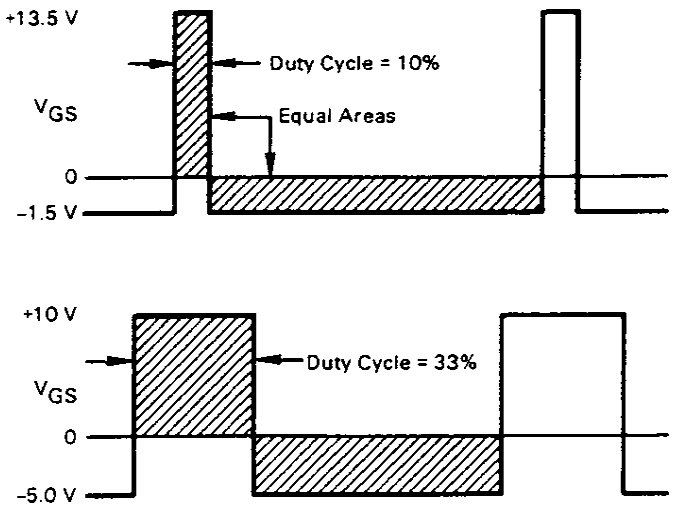


FIGURE 20 — Variation of V_{GS} with Duty Cycle in Pulse Transformer Gate Drive

The basic pulse transformer topology of Circuit 1 also has both maximum and minimum pulse width limitations in addition to those imposed by the volt-seconds requirements. The current in the primary winding may ramp-up to excessive levels due to magnetic saturation, especially in the smaller pulse transformers, if the pulse width is too wide. On the other hand, very short pulse widths may cause two different problems. First, transformer leakage inductance may limit current sourcing capability during a significant portion of the turn-on interval of a very small pulse width. Second, the pulse width must be wide enough to allow the magnetizing current (I_m) to ramp-up significantly, because the stored energy (defined by the current in the magnetizing inductance) provides turn-off drive to the MOSFET gate. To eliminate the problem of I_m varying with pulse width and to improve turn-off drive, the circuit shown in Figure 21 may be used.

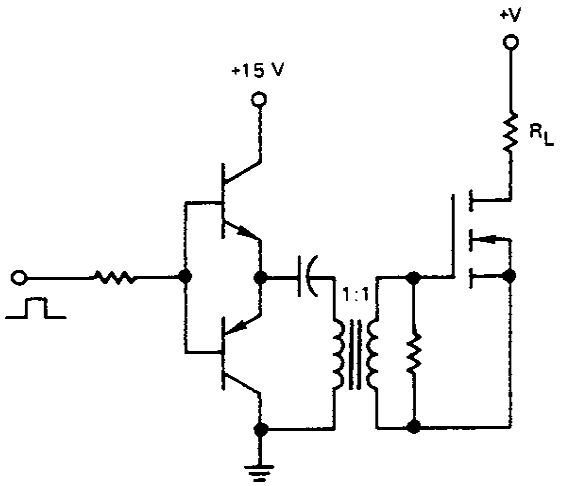


FIGURE 21 — Circuit to Eliminate the Varying of I_m with Pulse Width

A modification to the basic transformer gate drive circuit described above is the addition of a zener diode in series with the clamping diode (Circuit 2). The zener allows additional flyback voltage to appear across the primary terminal when Q1 is turned off. When this additional potential is induced across the secondary, it initially provides greater reset voltage levels and, thus, more rapid gate turn-off. Naturally, inherent in this circuit are the same duty cycle, pulse width and frequency limitations that accompanied Circuit 1.

Circuit 3 is very similar to Circuit 1 except the gate resistances are scaled upward and one is shunted by a diode. The purpose of this configuration is to speed up the MOSFET turn-on while leaving the turn-off slow in comparison. While the MOSFET input capacitance can charge rapidly through the diode, it must discharge through the two relatively high impedance gate resistances. This might be done to minimize inductive flyback voltage or any other undesired phenomena occurring during very rapid turn-off.

A variation of the push-pull converter is used to drive the gate of the MOSFET in Circuit 4. When Q1 is turned on, the 10 volts across the lower of the two primary windings induces the same potential in N_2. The voltage seen at the secondary, due to the 2:1 step-down ratio ($N_1 + N_2/N_3$), equals the primary supply voltage. At turn-off, the potential across N_2 reverses and is clamped to the 10 V supply by D1. Now N_2 induces its voltage in N_1 and the potential appearing at the secondary reverses in polarity but the magnitude is still 10 volts. If the pulse width is long enough to generate sufficient magnetizing current, this circuit yields good current sinking capabilities.

TABLE IV — Switching Speeds of Various TMOS Gate Drives

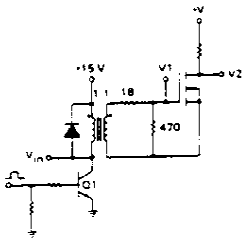
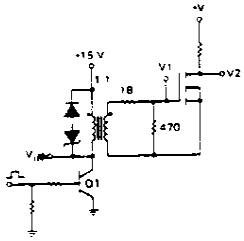
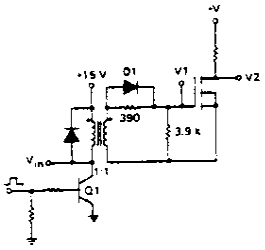
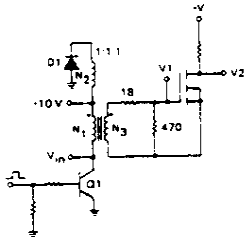
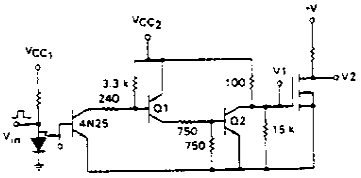
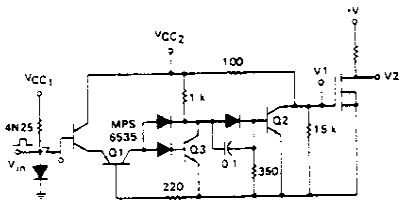
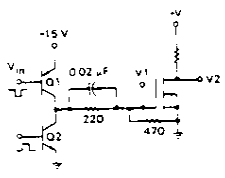
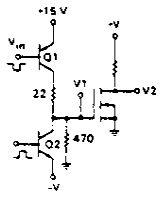
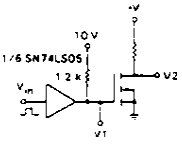
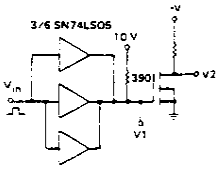
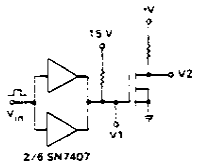
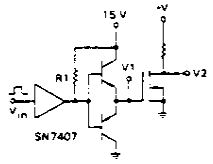
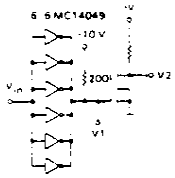
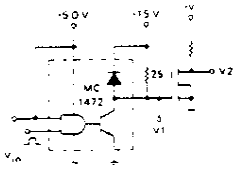
			Gate Switching Times (ns)				Drain Switching Times (ns)			
			Turn-on Delay (V_{in} vs V_1)	Turn-on Rise Time	Turn-off Delay (V_{in} vs V_1)	Turn-off Fall Time	Turn-on Delay (V_{in} vs V_2)	Turn-on Fall Time	Turn-off Delay (V_{in} vs V_2)	Turn-off Rise Time
Circuit 1 Simple Pulse Transformer			15	85	35	230	25	25	185	20
Circuit 2 Pulse Transformer w/Flyback Zener*			15	90	25	190	30	25	125	35
Circuit 3 Pulse Transformer w/Speed-up Diode		With Diode D1	30	95	220	1250	60	35	640	230
		Without Diode D1	50	1500	280	1100	220	340	660	230
Circuit 4 Quasi Push-Pull Transformer Drive			15	85	40	230	30	25	160	35
Circuit 5 Standard Opto-Coupling Circuit			3900	460	1600	140	4000	80	1750	20
Circuit 6 High B.W. Opto-Coupling Circuit			3700	420	450	120	3800	75	520	20
Circuit 7 High Performance Push-Pull Circuit			20	60	25	30	30	20	45	15

TABLE IV — Switching Speeds of Various TMOS Gate Drives (continued)

			Gate Switching Times (ns)				Drain Switching Times (ns)			
			Turn-on Delay (V_{in} vs V_1)	Turn-on Rise Time	Turn-off Delay (V_{in} vs V_1)	Turn-off Fall Time	Turn-on Delay (V_{in} vs V_2)	Turn-on Fall Time	Turn-off Delay (V_{in} vs V_2)	Turn-off Rise Time
Circuit 8 High Performance Push-Pull Circuit			20	60	45	70	40	25	85	15
Circuit 9 Low Power Schottky TTL			110	5000	60	600	480	1000	375	150
Circuit 10 Paralleled Low Power Schottky TTL			45	1800	30	210	180	310	140	50
Circuit 11 Paralleled SN7407 Buffers with Pull-Up Resistance			25	710	30	140	60	60	130	30
Circuit 12 SN7407 Buffer Driving a Complementary Emitter-Follower		R1 = 2.0 k	30	140	20	20	50	20	40	10
		R1 = 5.1 k	60	430	20	20	110	40	40	10
Circuit 13 Six Paralleled CMOS Inverters (MC14049UB)			30	920	20	130	100	160	90	30
Circuit 14 Dual Peripheral Driver (MC1472)			370	100	170	80	280	50	230	15
	*Transformer Specs Ferroxcube 3019P3CB $N_1 = N_2 = N_3 = 10$ Turns #19 Trifilar Wound $L_P \approx 0.6$ mH									

Two opto-coupled drive circuits are shown in Circuits 5 and 6. Circuit 5 is one of the most straight forward ways of developing a low impedance gate drive from the output of the opto-coupler. This circuit, however, is plagued by long switching delays that limit the useful operating frequency. These delays are inherent in the opto-coupler and their magnitudes are affected by the phototransistor's output load impedance. If this impedance is lowered, as accomplished with Circuit 6, the gate drive turn-off delay is significantly lower. Besides the complexity of these circuits, especially Circuit 6, the gate drive's bipolar output transistor, Q2, must remain on the entire time that the MOSFET is off. The energy dissipated in these two drivers during low duty cycle operation may be critical if efficiency is a major concern.

Circuits 7 and 8 are similar versions of a circuit that can be used as a high performance gate drive. The base currents for the bipolar drives must by push-pulled as shown in Figure 22. MOSFET turn-on is initiated during a positive transition of the input pulse. Q1 is turned on, supplying the required base current for Q3, which is Baker clamped to minimize its turn-off storage time. Both circuits have excellent turn-on times because of the low impedance path provided between the supply and the gate of the MOSFET.

Turn-off occurs when the falling edge of the input pulse is differentiated by the series combination of R1 and C1, thus turning on Q2. Base current is then free to flow into Q4, clamping the gate to ground or a negative potential. The duration of the clamping interval may be adjusted by varying the RC network. Before the occurrence of another input pulse, the MOSFET will remain off due to the 470 ohms gate-source resistance.

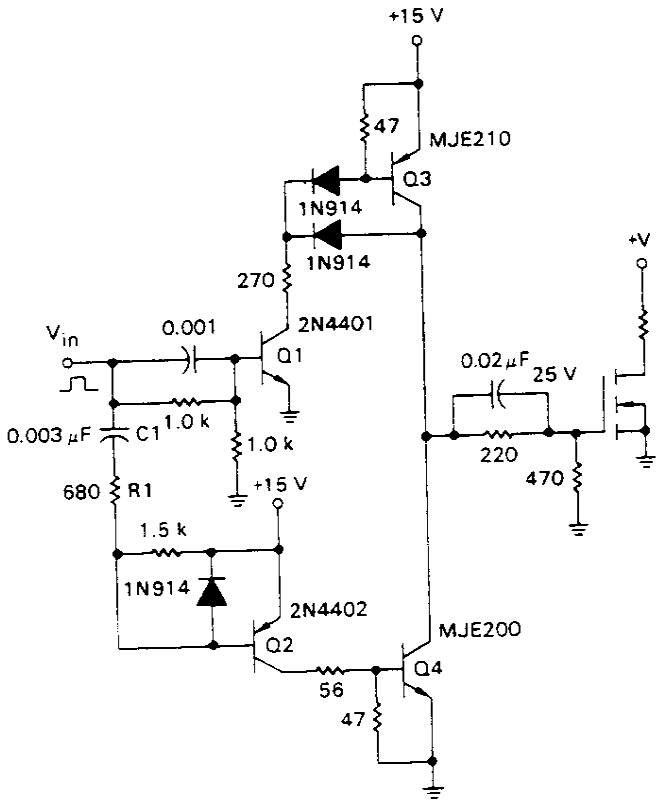


FIGURE 22 — Push-Pull Base Drive for Circuits 7 and 8

Circuits 9 though 12 are examples of how TTL devices may interface with the TMOS power MOSFET. The first of the circuits, number 9, has a very simple interface between the open collector, Low Power Schottky SN74LS05 hex inverter and the MTP12N10. Turn-off speed is fair, considering the circuit simplicity, but turn-on speed is poor because of the large value of R1 needed to protect the inverter from excessive power dissipation when the TTL output is low. Putting three such buffers in parallel, Circuit 10, reduces all the associated switching times by a factor of nearly two-thirds.

Another TTL device with an open collector output is utilized in Circuit 11. Two of the six buffers in the SN7407 operate in parallel with only a pull-up resistor and the gate of the MOSFET connected to the collector of the high voltage (30 volts) output transistors. The associated switching times are quite respectable given the simplicity of the drive circuit.

Another application of the SN7407, as mentioned earlier, is to use it to drive a discrete complementary emitter-follower buffer (Circuit 12). Lowering the pull-up resistor, R1, increases the turn-on speed at the expense of increasing gate turn-off power dissipation.

All six inverters of an MC14049UB are paralleled in Circuit 13. While the pull-up resistor is not a necessity (as it is with open-collector TTL devices), it does balance the current source and sink capabilities of the CMOS buffer. Without that resistor, one could expect slower turn-on but the drive circuit would be more efficient because the CMOS device no longer must sink the current drawn through R1 when the CMOS outputs are low. Of course, fewer than the six paralleled inverters could be used at the cost of slower switching.

Several ICs that were originally intended for other applications have been adopted by some circuit designers looking for fast, yet simple and efficient MOSFET gate drive schemes. One such device is the MC1472, a dual peripheral driver, designed to interface MOS logic to high current loads such as relays, lamps and printer hammers. Because each of the two output transistors can sink 300 mA, MOSFET turn-off times are short when this device is used in a gate drive network. Turn-on times are also short in Circuit 14 because the value of R1 is so low that it only minimally impedes the current during the charging of the MOSFET input capacitances. The advantage of this large current sourcing capability is once again offset by the significant currents that will flow whenever the MC1472 output is low to turn the MOSFET off. In fact, for the 25 ohm pull-up resistor and a V_{CC1} of 15 volts, that current approaches the combined sinking capabilities of the two output transistors in that package. Other examples of ICs that are used to drive the gate of a power MOSFET are the MMH0026 dual MOS clock driver, the MC1555 timer, the TL494 pulse width modulation control circuit and the MC75451 peripheral driver. As power MOSFETs gain in popularity, more drivers specifically designed for MOSFETs will appear.

TEMPERATURE DEPENDENT CHARACTERISTICS

$r_{DS(on)}$

Junction temperature variations and their effect on the on-resistance, $r_{DS(on)}$, should be considered when designing with power MOSFETs. Since the on-resistance varies approximately linearly with temperature, power MOSFETs can be assigned temperature coefficients that describe this relationship. For example, the MTM8N15 data sheet includes Figure 7 which illustrates the relationship between temperature, $r_{DS(on)}$ and I_D. At I_D = 8.0 A, the temperature coefficient is:

$$\frac{\Delta r_{DS(on)}}{\Delta T_J} = \frac{0.74\text{-}0.48\ \Omega}{100\text{-}25°C} = 0.0035\ \Omega/°C$$

Using 0.0035 Ω/°C, an $r_{DS(on)}$ of 0.83 Ω is easily computed for an I_D of 8.0 A and a T_J of 125°C. The temperature coefficient will vary between product lines but the on-resistance approximately doubles between a T_J of 25°C and 125°C. Since the static losses in a bipolar do not increase appreciably with temperature, as temperature increases, bipolars accentuate one of their greatest advantages over MOSFETs—lower on voltages.

Switching Speeds are Constant with Temperature

High junction temperatures emphasizes one of the most desirable characteristics of the MOSFET, that of low dynamic or switching losses. In the bipolar, temperature increases will increase switching times causing greater dynamic losses. On the other hand, thermal variations have little effect on the switching speeds of the power MOSFET. These speeds depend on how rapidly the parasitic input capacitances can be charged and discharged. Since the magnitudes of these capacitances are essentially temperature invariant, so are the switching speeds. Therefore, as temperature increases, the dynamic losses in a MOSFET are low and remain constant, while in the bipolar the switching losses are higher and increase with junction temperature.

Threshold Voltage

The gate voltage at which the MOSFET begins to conduct, the gate threshold voltage, is also temperature dependent. The variation with T_J is linear as shown on all data sheets. Having a negative temperature coefficient, the threshold voltage falls about 10% for each 45°C rise in the junction temperature.

Importance of $T_{J(max)}$ and Heat Sinking

Two of the packages that commonly house the TMOS die are the TO-220AB and the TO-204/formerly TO-3. The power ratings of these packages range from 40 to 250 watts depending on the die size and the type of material used as the heat spreader. These ratings are nearly meaningless, however, unless some heat sinking is provided. Without heat sinking the TO-204 and the TO-220 can dissipate only about 4.0 and 2.0 watts respectively, regardless of the die size.

Because long term reliability decreases with increasing junction temperature, T_J should not exceed the maximum rating of 150°C. Steady state operation above 150°C also invites abrupt and catastrophic failure if the transistor experiences additional transient thermal stresses. Excluding the possibility of thermal transients, operating below the rated junction temperature can enhance reliability. A $T_{J(max)}$ of 150°C is normally chosen as a safe compromise between long term reliability and maximum power dissipation. Motorola is presently conducting reliability tests at T_J = 200°C to determine if that temperature is an acceptable $T_{J(max)}$ specification for the TO-204 package.

In addition to increasing reliability, proper heat sinking can reduce static losses in the power MOSFET by decreasing the on-resistance. $r_{DS(on)}$, with its positive temperature coefficient, can vary significantly with the quality of the heat sink. Good heat sinking will decrease the junction temperature, which further decreases $r_{DS(on)}$ and the static losses. Regarding poor heat sinking, the converse is also true.

DRAIN-SOURCE DIODE

Inherent in most power MOSFETs, and all TMOS transistors, is a "parasitic" drain-source diode. Figure 1, the illustration of cross-section of the TMOS die, shows the P-N junction formed by the P-well and the N-Epi layer. Because of its extensive junction area, the current ratings of the diode are the same as the MOSFET's continuous and pulsed current ratings. For the N-Channel TMOS FET shown in Figure 23, this diode is forward biased when the source is at a positive potential with respect to the drain. Since the diode may be an important circuit element, Motorola Designer's Data Sheets specify typical values of the forward on-voltage, forward turn-on and reverse recovery time. The forward characteristics of the drain-source diodes of several TMOS power MOSFETs are shown in Figure 24.

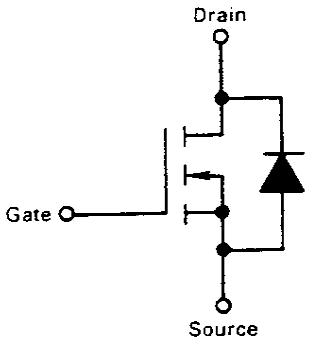


FIGURE 23 — Complete N-Channel Power MOSFET Symbol Including Drain-Source Diode

Most rectifiers, a notable exception being the Schottky diode, exhibit a "reverse recovery" characteristic as depicted in Figure 25. When forward current flows in a standard diode, a carrier gradient is formed in the high resistivity side of the junction resulting in an apparent storage of charge. Upon sudden application of a reverse bias, the stored charge temporarily produces a negative current flow during the reverse recovery time, or t_{rr}, until the charge is depleted. The circuit conditions that

influence t_{rr} and the stored charge are the forward current magnitude and the rate of change of current from the forward current magnitude to the reverse current peak. When tested under the same circuit conditions, the parasitic drain-source diode of a TMOS transistor has a t_{rr} similar to that of a fast recovery rectifier.

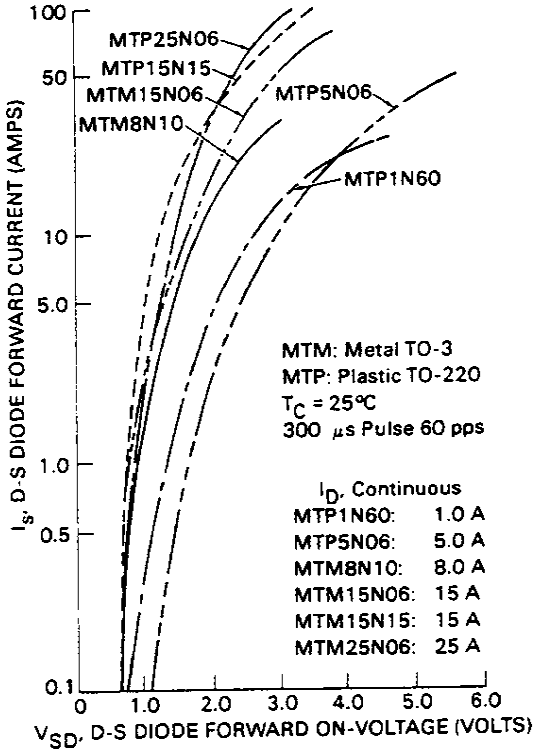


FIGURE 24 — Forward Characteristics of Power MOSFETs D-S Diodes

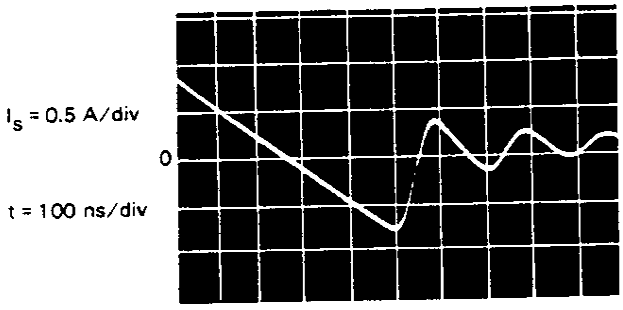


FIGURE 25 — Reverse Recovery Characteristics of MTM15N15 Drain-Source Diode

In many applications, the drain-source diode is never forward biased and does not influence circuit operation. However, in multi-transistor configurations, such as the totem pole network of Figure 26, the parasitic diodes play an important and useful role. Each transistor is protected from excessive flyback voltages, not by its own drain-source diode, but by the diode of its complementary transistor. As an illustration, assume that Q2 of Figure 26 is turned on, Q1 is off and current is flowing up from ground, through the load and into Q2. When Q2 turns off, current is diverted into the drain-source diode of Q1 which clamps the load's inductive kick to V^+. By similar reasoning, one can see that D2 protects Q1 during its turn-off.

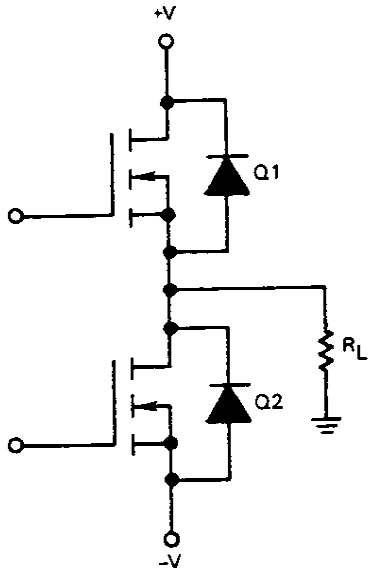


FIGURE 26 — TMOS Totem Pole Network with Integral Drain-Source Diodes

As a note of caution, it should be realized that the drain-source diode of a power MOSFET, like all diodes except the Schottky, have forward recovery times, meaning they do not instantaneously conduct when forward biased. Therefore, in a totem pole configuration, the TMOS drain-source diode may be too slow to protect the complementary transistor from excessive flyback voltage. Because of this possibility, rapid switching of such configurations may require other clamping schemes.

P-CHANNEL POWER MOSFETs

To complement some of the N-channel devices, Motorola also produces P-channel power MOSFETs. Because current carriers in the P-channel devices are holes, which have lower mobility than the electron carriers of the N-channel devices, the $r_{DS(on)}$ of P-channel MOSFETs is always greater for a given die size and drain-source breakdown voltage. This impedes the development of truly complementary devices. For instance, if equal on-resistances are desired, the unequal die dimensions will mandate differences in all die area dependent parameters such as capacitances, pulsed current ratings, thermal resistance and safe operating areas.

The application will determine which of the device parameters—whether it be the on-resistance, drain-source breakdown voltage, transconductance, etc.—need be matched closely. Table V compares the pertinent electrical parameters of the MTP8P10 with those of N-channel devices that may be considered as device complements. Besides showing the MTP8N10 is not always the best choice for a complement to the MTP8P10,

the table also indicates the die area of a P-channel device must be approximately doubled to achieve the on-resistance of an N-channel device with the same $V_{(BR)DSS}$ rating.

P-channel power MOSFETs can simplify certain circuit configurations much in the same way that PNP bipolars can. The circuit simplicity obtained when using P-channel devices to switch a grounded load, for instance, may more than offset the price differential between the N- and P-channel devices.

In Figure 27 the source is connected to the positive rail and the drain is attached to the load. As such, the MOSFET is off when $V_{GS} = 0$ V and begins to turn on as V_{GS} (a negative quantity) rises in absolute magnitude above the device threshold voltage. Current would then be free to flow from the source to drain and into the load. Still, a logic signal, which is normally referenced to ground, must be used to control the gate. A level shifter, followed by a discrete emitter-follower-buffer can supply the proper logic levels while at the same time provide rapid MOSFET switching.

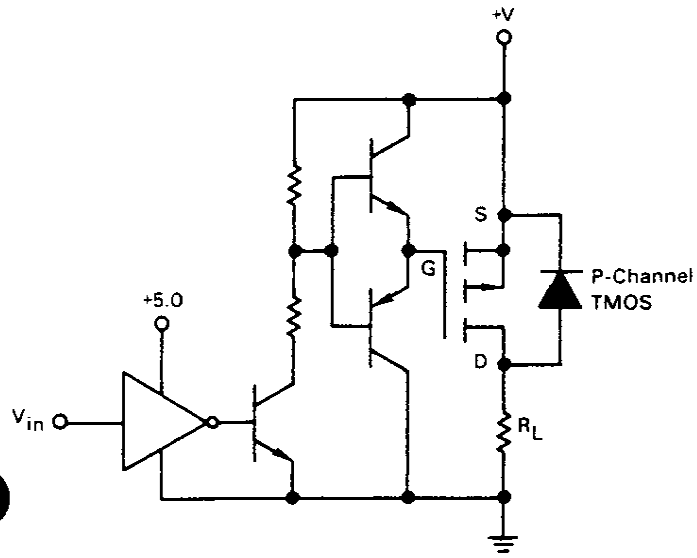


FIGURE 27 — Level Shifter for P-Channel MOSFET Driving a Grounded Load

The main difficulty in driving an N-channel device as an emitter-follower is that the gate-to-source voltage must be carefully controlled as the source-to-ground potential is swinging from ground up to near the positive rail. All driving schemes somehow must provide a gate signal that is referenced to the source of the power MOSFET. There are basically three ways to drive a grounded load with an N-channel device. They are:

1. By bootstrapping.
2. By using pulse transformers.
3. By using opto-couplers.

The simplicity of bootstrapping makes that method the one of choice if its limitations are inconsequential in the specific application or they can somehow be circumvented. The bootstrapping circuit in Figure 28 generates the required gate-to-source signal. One of the main problems with this topology is that the load cannot remain in the on state for an unlimited period of time because the finite charge stored in C1 is eventually bled off. A second problem is that this circuit cannot switch high voltages since C1 will be charged to the system supply voltage and then this potential will be impressed across the gate to source. Fortunately, in applications that require grounded loads, such as those in the automotive industry, the supply voltages are often compatible with this method of bootstrapping.

By using a pulse transformer one can also achieve the desired gate-to-source signal. This method is described in the section entitled "Power MOSFET Gate Drives".

TABLE V — Complements of MTP8P10

		P-Channel	N-Channel			Units
		MTP8P10	MTP8N10	MTP10N10	MTP12N10	
Drain-Source Voltage (Max)		100	100	100	100	Vdc
I_D	Continuous	8.0	8.0	10	12	Adc
	Pulsed	25	20	25	30	Adc
Max Power Dissipation		75	75	75	75	Watts
Threshold Voltage		2.0 to 4.5	2.0 to 4.5	2.0 to 4.5	2.0 to 4.5	Vdc
On-Resistance @ $I_D/2$ (Max)		0.4	0.5	0.33	0.18	ohms
Transconductance (Min)		2.0	1.5	2.5	3.0	mhos
Input Capacitance (Max)		1200	400	600	1200	pF
Output Capacitance (Max)		600	350	400	500	pF
Reverse Transfer Capacitance (Max)		180	100	80	250	pF
Fall Time (Max)		150	120	150	150	ns
Rise Time (Max)		150	60	50	100	ns
Normalized Die Area		1.0	0.45	0.66	1.0	—

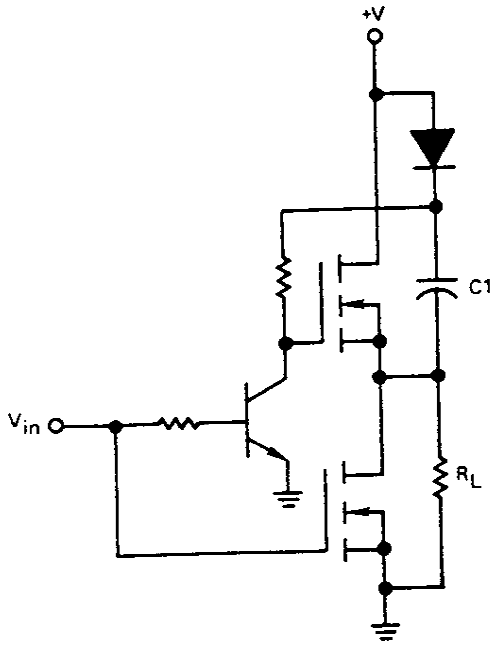


FIGURE 28 - Bootstrapping Circuit to Drive a Grounded Load with N-Channel TMOS

An opto-coupler certainly may be used in this situation but a second supply, referenced to the source of the MOSFET, is needed to power the output of the opto-coupler. The upper rail of this supply must be free to rise above the drain supply voltage when the MOSFET is turned on, requiring either a supply be completely isolated from the drain supply or one that is generated from it by a bootstrapping method.

Conclusion

Clearly, the advantages and disadvantages of the power MOSFET give that technology its specific realm of usefulness. That niche is in systems that utilize simple drive circuitry and/or require efficient high frequency switching. Some designers also favor the power MOSFET because of its extended FBSOA or its other more subtle advantages. This application note has outlined and explained the most common considerations that the designer should be aware of when designing with TMOS power MOSFETs. Following these suggestions will yield excellent reliability and performance.

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