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Application Note

UNDERSTANDING POWER TRANSISTOR DYNAMIC BEHAVIOR — dv/dt EFFECTS ON SWITCHING AND RBSOA —

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Power transistor dynamic behavior can be affected to a large extent by dv/dt limitations. A look at the internal workings of the transistor readily shows how these limitations arise. A simple circuit model is developed which reproduces the behavior of power transistors in dv/dt limited modes of operation. Experience with the model gives some guidelines for minimizing dv/dt limitations in practical circuits.

INTRODUCTION

Power transistor dynamic behavior is affected, to a first order extent by rates of dv/dt which are found in today's power conditioning circuits. These effects show up in terms of switching speed, shape of crossover time waveforms, and reverse bias safe operating area. In particular, complex aberrations in crossover time waveforms are easily explained by using a dv/dt model.

OBSERVED BEHAVIOR

The effects of dv/dt limitations show up most readily in turn-off waveforms. Aberrations similar to those in the voltage rise and current fall waveforms of Figure 1 are a commonly observed result.

The types of possible aberrations are by no means limited to those shown in the examples here. In general, dv/dt limitations are indicated by additional inflections in the voltage rise and current fall waveforms. The additional inflections can be either single or multiple. They can affect either the current fall or voltage rise waveforms singly, or they can be present in both waveforms. dv/dt limitations can also cause what is generally called a "porch" or tailing in the collector current waveform. Additional examples are shown in Figure 2.

In addition to affecting the shape, dv/dt limitations can show up as a lengthening of the crossover time. It is possible for a dv/dt limited transistor to have normal looking waveforms which are merely slower than they otherwise would have been.

Generally speaking, the type of waveform observed is dependent upon the timing of a dv/dt generated current pulse. Further discussion of this topic is presented in the next two sections.

The effects of dv/dt also show up in the shape of the RBSOA curve. Internal current flow generated by dv/dt is, in part, responsible for the portion of Figure 3 that falls below BV_{CBO}.

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These observed behaviors are fairly easily explained by looking at what happens in the transistor structure when a rapidly rising voltage is present at the collector; in other words, by looking at a little bit of transistor physics.

TRANSISTOR PHYSICS

There are two primary aspects of transistor design that are responsible for sensitivity to dv/dt. These are the inevitable capacitance that comes along with the collector-base junction, and the emitter geometry.

A look at Figure 4 will lend some insight as to how these structural characteristics are involved in dv/dt limitations.

The arrows represent current flow across the collector-base junction. This current is produced when a positive value of dv/dt is impressed across the junction capacitance. Note that the current flow is uniform across the collector base junction.

The largest portion of the injected current causes no substantial effect on performance. It is merely swept out the base lead, under the influence of reverse bias. However, if conditions are right, some of the current injected near the center of the emitter finger is allowed to flow vertically through the structure. This current that flows vertically is forward bias base current. The transistor cannot distinguish the difference between it and turn-on base current which is intentionally supplied from outside. If any of this dv/dt induced current is not swept out the base lead, and is allowed to flow vertically, it will get gain multiplied.

Gain multiplication of C_{ob} injected base current is the essence of dv/dt limited power transistor behavior. The operation of transistor gain on the injected current results in a pulse of collector current, which would otherwise not exist, superimposed upon the normal collector current fall waveforms.

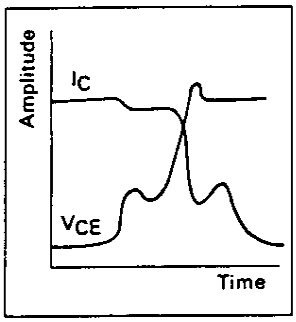

FIGURE 1 — dv/dt Limited Waveforms

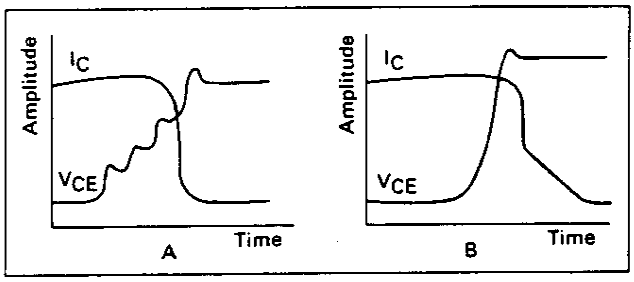

FIGURE 2 — Additional dv/dt Limited Waveforms

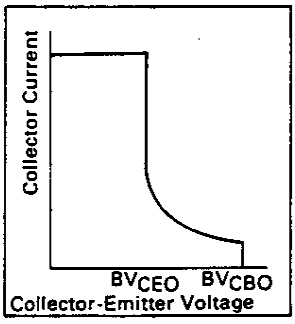

FIGURE 3 — Typical RBSOA Curve

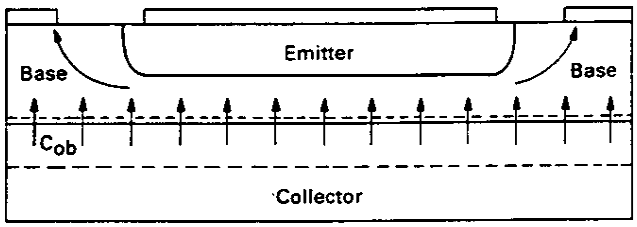

FIGURE 4 — Emitter Finger Crossectional View

The dynamic differences in dv/dt limited waveforms are dependent upon the timing of this pulse. If it occurs very early in the turn-off response, a distorted voltage rise waveform such as that in Figure 2-A is likely. If, on the other hand, the pulse occurs late in the crossover time waveform, some form of tailing in the current fall waveform is more likely. All combinations in-between are also possible. This includes the possibility that both voltage rise and collector current fall waveforms are smooth, but crossover time is considerably lengthened with respect to what it would be without the dv/dt limitation.

Reverse bias safe operating area is also affected, although the results are not as easy to observe as they are in the switching waveforms. However, the effects are very much present, and can be explained as follows.

Given the absence of vertical base current flow, the fundamental RBSOA limitation of a bipolar transistor is its collector-base breakdown voltage. The limiting constraint, as long as the base-emitter junction remains reverse biased, is the collector-base voltage. At low currents, this constraint is satisfied, and RBSOA extends to BV_{CBO} (Figure 3). However, if any dv/dt injected base current is permitted to flow vertically, a portion of the base-emitter junction becomes forward biased. In the forward biased mode, maximum operating voltage is reduced to $BV_{CEO(sus)}$. This represents a substantial reduction in RBSOA capability, and helps to explain why power transistors appear to be more fragile when they are operated at high speeds. High rates of dv/dt will generally have an adverse effect on the transistor's ability to withstand turn-off stress.

MODELS

The model shown in Figure 5 was derived in a straightforward manner from the emitter finger cross section in Figure 6. The subscripts E and C refer to those portions of the emitter finger which are relatively at the edge and relatively toward the center respectively. Base spreading resistance is shown as r_b.

From this model, it is very easy to see how dv/dt affects transistor performance very little, unless C_{ob} injected current gets trapped by the base spreading resistance. Any current generated by Q_E's C_{ob} capacitance is shunted into the turn-off bias ($V_{BE(off)}$). Consequently, dv/dt has little effect on performance. However, the situation changes quite a bit with respect to Q_C. Due to the presence of r_b, current flowing through its C_{ob} capacitance has the option of flowing either into the off bias supply, or through the base-emitter junction. If conditions are right, and base current flows into Q_C, then the high rate of dv/dt caused by the rapid turn-off of Q_E causes a current pulse to flow through Q_C. In the model, this current pulse can be easily measured and correlated to waveform aberrations.

This simple model produces most observable waveform aberrations quite well. However, it has some trouble in generating Q_C current pulses early enough to produce the voltage rise aberrations depicted in Figure 2-A.

It was suspected that non-linearity in r_b is required to fully duplicate this waveform. The model shown in Figure 7 represents the worst case of non-linearity; here, the diode allows virtually no C_{ob} injected base current to be excavated by the off bias. This model faithfully reproduces all of the waveform aberrations that are shown in Figures 1 and 2.

CIRCUIT DESIGN IMPLICATIONS

Power transistor dv/dt limitations can be described in one word, undesirable. Therefore, it is of some interest to take a look at circuit techniques which can minimize or eliminate dv/dt limitations.

There are three variables with which the circuit designer can control dv/dt. They are on-drive, off-drive, and snubbing. Each one is considered individually, beginning with on-drive.

On-Drive

At first glance, on-drive might appear to be an unlikely candidate for influencing dv/dt limited behavior. However, on-drive has a first order affect on the nonlinearity in base spreading impedance. The harder the transistor is driven in the on state, the more difficult it is for off bias to remove charge under the emitter fingers. Therefore, dv/dt limited behavior can be affected dramatically by the amount of turn-on drive.

From a circuit point of view, the message is clear. Minimum turn-on base drive will yield maximum freedom from dv/dt limitations. From a practical point of view, the Baker Clamp is an excellent vehicle for maximizing transistor performance in this regard.

Off-Drive

The effects of off-drive on dv/dt limited behavior are rather complex, and somewhat unpredictable. The reason is that a change in off bias simultaneously affects both the magnitude of dv/dt, and the efficiency with which dv/dt induced currents are removed. For example, as off-bias is increased, collector current fall time is reduced. The reduction in fall time will, in most inductive circuits, cause a higher value of dv/dt to appear at the collector. This higher value of dv/dt will cause more current to be generated in the transistor's collector-base junction capacitance, tending to increase dv/dt limitations. On the other hand, the increased off bias excavates base charge more efficiently, tending to decrease dv/dt limitations. Which effect will win out depends upon a host of variables, including transistor processing, on-drive, collector current, temperature, and load line shaping, to name a few.

Perhaps the most practical approach in dealing with this variable is to observe its effects under actual operating conditions. A relatively small change in off-bias can, at times, clean up some rather messy looking waveforms.

Snubbing

Snubbing is a very effective technique for dealing with dv/dt limited behavior. Since a critical value of dv/dt is required to generate undesirable behavior, snubbing can be used as a complete cure. With the addition of enough snubbing, dv/dt is reduced below the critical value that is needed to cause limitations. In these circumstances, dv/dt no longer has a first order effect on performance.

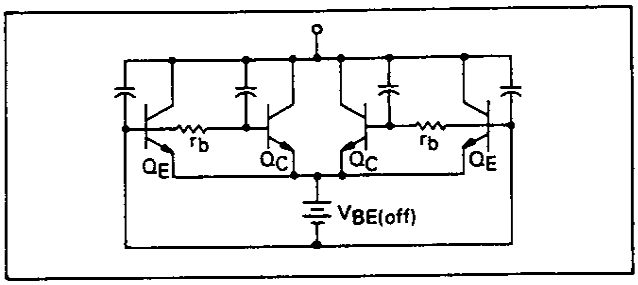

FIGURE 5 — dv/dt Model

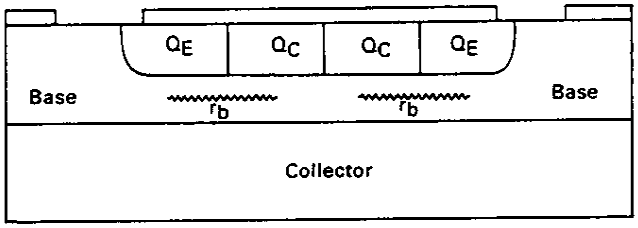

FIGURE 6 — Emitter Finger Crossection

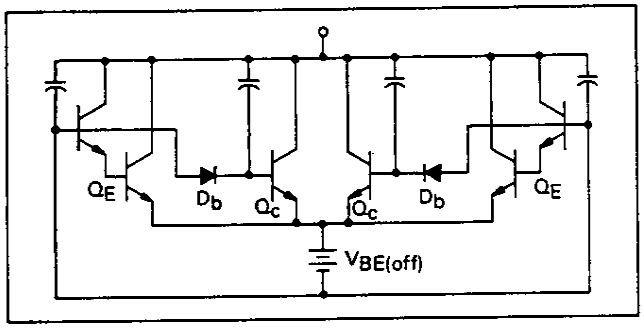

FIGURE 7 — Refined dv/dt Model

CONCLUSION

Concepts relating to dv/dt play a significant role in understanding some of the more subtle aspects of power transistor dynamic behavior. dv/dt has an effect on switching times, switching waveform shapes, and reverse safe operating area. Understanding the basic phenomena leads to techniques for minimizing dv/dt limitations in high speed power conditioning circuits.

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