AN-701

UNDERSTANDING MECL 10,000 DC AND AC DATA SHEET SPECIFICATIONS

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The dc and ac specifications for emitter-coupled logic are somewhat different than those for saturated logic. This application note describes the specifications found on a MECL 10,000 data sheet and provides information for understanding these specifications for persons unfamiliar with emitter-coupled logic.

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INTRODUCTION

The increasing need for high speed digital systems has led to the growth and popularity of emitter coupled logic, in particular, MECL 10,000. Application areas that traditionally have been TTL designs are being designed with ECL, in addition to the areas normally designed with ECL, due to the marketplace demand for high performance. When using a different logic family, an engineer must become familiar with the operating characteristics and specifications of the family. Because of dissimilar design and operating concepts, the specifications for ECL are somewhat different than those for TTL. A good approach to understanding ECL specifications is an investigation of the basic gate design and then a description of the dc and ac parameters of the logic family.

BASIC GATE CIRCUIT DESCRIPTION

The basic MECL 10,000 gate circuit consists of a differential amplifier, a reference voltage bias network, and emitter-follower buffering transistors (Figure 1). The

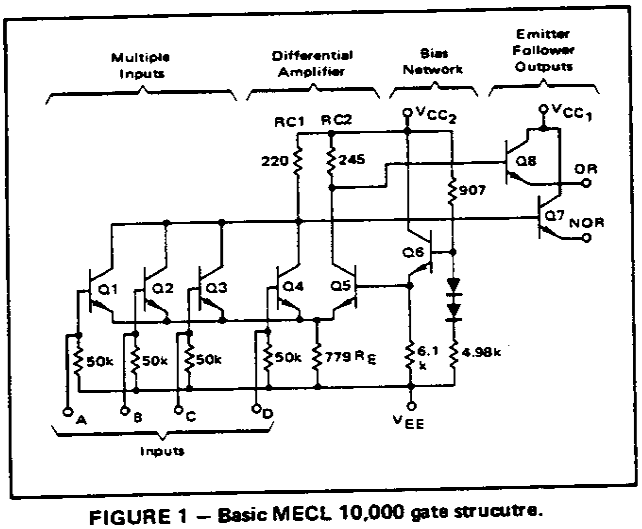

FIGURE 1 – Basic MECL 10,000 gate strucutre.

power supply voltages are V_{CC} = GND and V_{EE} = -5.2 V. To explain operation of the gate circuit, operation of each individual section of the circuit will be described.

The differential amplifier is an emitter-coupled current switch consisting of transistors Q1 thru Q5. The multiple gate inputs provide an OR'ing function (Q1 thru Q4) which is amplified by the current switch.

To examine current switch operation begin with all gate inputs low (nominally -1.75 V) and the base of Q5 referenced to V_{BB} (nominally -1.29 V). Transistor Q5 will be conducting current and the common emitter point of the transistors will be about -2.09 V = $V_{BB} - V_{BE}$ (Q5). Transistors Q1 thru Q4 will not be conducting current because the input base-emitters of these devices will not be sufficiently forward biased.

The current through Q5 will be about 4 mA with a voltage of -2.09 V at the emitter node of the transistors and an emitter resistor of 779 ohms. The voltage drop at the Q5 collector node established by the 4 mA current and resistor R_{C2} is about -0.98 V. The voltage drop at Q1 – Q4 collector node is about -0.05 V because only the current to the base of the emitter-follower passes through the resistor (transistors Q1 thru Q4 are not conducting).

The emitter-followers serve to buffer the current switch from loading and to restore output voltages to proper MECL levels. The OR output is obtained through Q8 giving a low level $V_{OL} = V_{RC2} + V_{BEQ8}$ = -1.75 V. Similarly the NOR output is obtained through Q7 with a V_{OH} = -0.924 V.

If one or more of the gate inputs is switched to a high logic level, the current in the differential amplifier will flow through the input transistor cluster and resistor R_{C1}. A high logic level on the base of any of the input transistors will forward bias the corresponding transistor (Q5 ceases to conduct) and allow a current flow of approximately 4.49 mA in the switch.

The voltage drop at collector resistor R_{C1} will now be about -0.98 V as established by the current through the resistor. V_{RC2} will be about -0.05 V. After translating through the emitter-followers, the NOR output will be nominally a V_{OL} = -1.75 V and the OR output will be nominally V_{OH} = -0.924 V.

The bias network provides a reference voltage V_{BB} = -1.29 V typical at 25°C. The characteristics of the bias driver compensate for variations in power supply voltage and temperature change to insure that the threshold point remains in the center of the transfer characteristic.

Although the above discussion describes operation of the basic gate function, more complex circuits operate with a similar current switching action. The emitter resistor R_E will be replaced by a current source as the current switch (or "tree") becomes more complex with such features as multilevel gating. In any case, an analysis could be done on these devices and they would have similar input and output levels.

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.
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TRANSFER CURVE AND DC LEVELS

To show the transfer characteristics of a MECL gate, a curve may be obtained showing output levels versus input levels for both the OR and NOR outputs. Referring to Figure 2, the transfer curve for a MECL 10,000 gate is presented with the dc specification points at 25°C. A discussion of the specification points will help in understanding the transfer curve and logic operation of the gate.

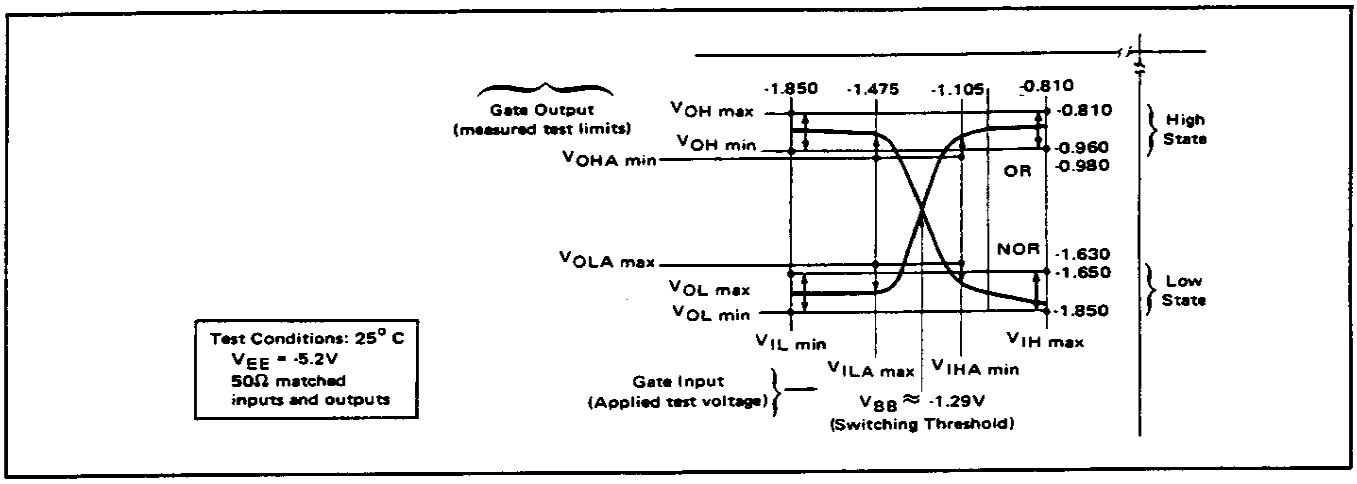

FIGURE 2 – MECL 10,000 transfer curve and specification points.

As an input moves from a logic low voltage to a logic high voltage, the OR output goes from a low voltage to a high voltage and the NOR output goes from a high to a low voltage (providing all other inputs stay low). In normal operation, any MECL 10,000 output will be within specified minimum and maximum limits when in either the high or low state.

The specified limits for output voltages are shown in Figure 2. The high output level will fall between V_{OHmax} = –0.810 V and V_{OHmin} = -0.960 V, and the low output level will be between V_{OLmax} = -1.650 V and V_{OLmin} = -1.850 V. These are the normal operating levels for MECL 10,000 (25°C) and output voltages remain within the preceding limits as long as the inputs stay within normal logic levels.

As the input voltage approaches the transition region, additional specification points become important. These points are V_{IHA}, V_{ILA}, V_{OLA}, and V_{OHA} which serve two purposes. The first purpose is to define the transition region of the transfer characteristics, i.e., the actual switching region of the gate. The "X" of the transfer curve must fall within the limits established by the threshold voltages. The second purpose of the threshold voltage is to define the guaranteed noise margins for MECL 10,000.

The guaranteed noise margins are defined as follows:

$$N.M._{high\ level} = V_{OHAmin} - V_{IHAmin}$$

$$N.M._{low\ level} = V_{ILAmax} - V_{OLAmax}$$

This may be seen more clearly in Figure 3. Noise margin is the "band" of voltage to protect against erroneous operation due to undershoot, noise, etc. The guaranteed noise margins are worst case numbers as defined by the threshold voltages, 125 mV for the high state and 155 mV for the low state. Typical noise margins, as would be seen from Figure 3, are greater than 200 mV.

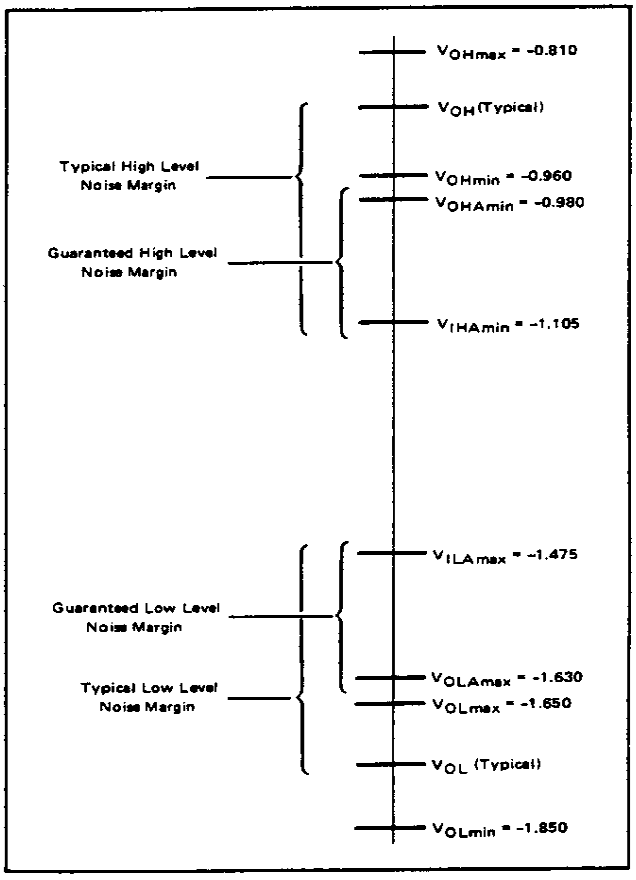

FIGURE 3 – MECL 10,000 output levels and noise margins at 25°C.

THE MECL 10,000 DATA SHEET

The data sheet for a MECL 10,000 device consists of several elements including a device description, logic diagram, dc and ac specifications, and switching time test

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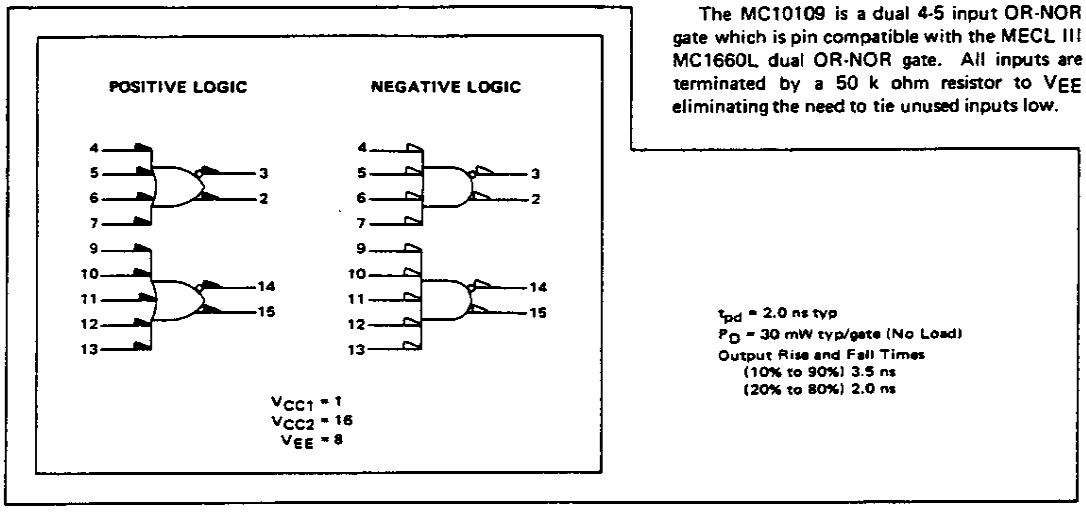

The MC10109 is a dual 4-5 input OR-NOR gate which is pin compatible with the MECL III MC1660L dual OR-NOR gate. All inputs are terminated by a 50 k ohm resistor to V_{EE} eliminating the need to tie unused inputs low.

t_{pd} = 2.0 ns typ
P_D = 30 mW typ/gate (No Load)
Output Rise and Fall Times
(10% to 90%) 3.5 ns
(20% to 80%) 2.0 ns

CIRCUIT SCHEMATIC

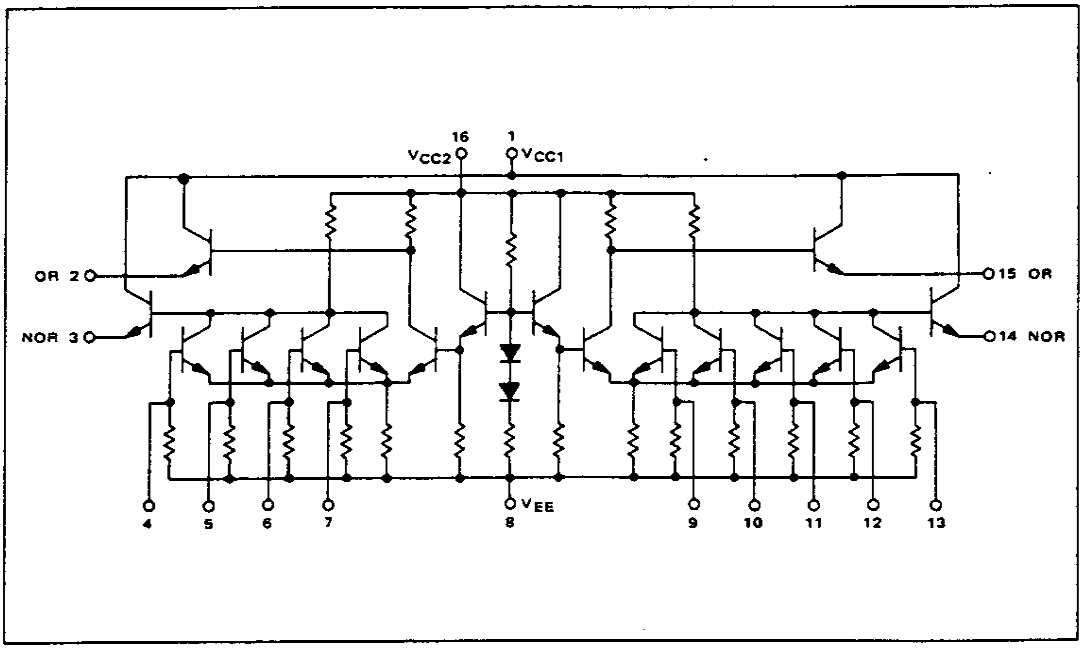

FIGURE 4 – Front page of MC10109 data sheet.

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circuits. Also, some devices will have additional information such as truth tables, circuit schematic diagrams, and applications information.

The device description provides a synopsis of the outstanding characteristics of the logic element. This information in conjunction with the logic diagram provides basic operational information for the device. On many data sheets, both the positive and negative logic diagrams are shown for the convenience of the designer (Figure 4). Also, in the example shown of the MC10109, the circuit schematic is also provided.

On more complex parts, truth tables are shown to describe operation of the circuit. The type of truth table may range from a simple dc configuration to a complex sequential ac configuration such as for the MC10136 (Figure 5). The truth table shows the output logic states

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H

ϕ = Don't care.
* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

FIGURE 5 – Sequential AC truth table for MC10136 universal counter.

as the inputs vary in sequence as shown from top to bottom of the table. Also, outputs change on a low to high transition of the clock. The intent of the truth table is to show clocked sequential operation of the counter under varying input conditions. Other counters and shift registers have similar tables.

The dc and ac specifications will be described in much greater detail for these are the parameters with which the designer must be very familiar. Additional information on the data sheet such as applications ideas is provided for the benefit of the designer and need not be described in more than a general sense.

DATA SHEET DC LEVEL SPECIFICATIONS

The data sheet for a device gives the specific limits, levels, and switching times a manufacturer guarantees. For MECL 10,000 the pertinent dc specifications and switching times are contained in a table of electrical characteristics (Figure 6). The table is accompanied by a statement of the conditions under which the table limits will be met. The devices are specified at 500 LFPM air flow to reflect normal system usage and 50 ohms to -2.0 volt loading (which is the worst case limit for output loading). Slight variations in airflow from 500 LFPM and loading of 50 ohms will not result in any appreciable change in operation of MECL 10,000. If large variations, such as greater than 20% change in airflow and/or 50 ohm loading, the "MECL Integrated Circuit Data Book" and the "MECL System Design Handbook" should be consulted for changes in specific parameters.

The table is composed of four major sections: the dc voltage and current levels, the ac switching limits, the input forcing functions, and input pin test conditions. The input pin test conditions show how the forcing functions are applied to obtain the dc and ac limits given.

The individual dc characteristics are discussed below:

1. **Power Supply Drain Current** – The value, I_E, specified by this test is the current leaving the V_{EE} pin of the device at -5.2 volts. I_E is essentially independent of output loading, and a maximum value for worst case design is given for 25°C. This current may be used to calculate package power, not including output load power.

2. **Input Current** – Two values, I_{inH} and I_{inL}, are given for this parameter. I_{inH} is a maximum value of current required by the input. It is tested with V_{IHmax} applied to the input under test.

I_{inL} is the minimum value of current an input will draw when V_{ILmin} is applied to the input. This value is tested to insure that the input pulldown resistor (nominally 50 kohms) is sufficiently low in magnitude. The high impedance input pulldown resistor forces the input to a low state if the input is not externally connected. If the resistor is too large in magnitude, it may not sink sufficient collector-base leakage current from the input transistor to insure a low logic input state.

3. **High Output Voltage** – The minimum and maximum V_{OH} limits are given at 25°C and the commercial range temperature extremes, -30°C and 85°C. MECL 10,000 levels track with temperature, therefore, different limits are listed for the various temperatures. The V_{OH} level at 25°C falls in the band of voltage between V_{OHmax} and V_{OHmin} as shown in the transfer curve (Figure 2).

When testing V_{OH} at an output, corresponding inputs are placed at either V_{IHmax} or left open. V_{IHmax} is the maximum allowable high input voltage, and an open input will exhibit an extreme minimum low level.

4. **Low Output Voltage** – This parameter is similar to high output voltage in that minimum and maximum values are given at 25°C, -30°C and 85°C. Also, inputs are left open or placed at V_{IHmax} when testing V_{OL}.

V_{OL} falls in the lower band of voltage between V_{OLmax} and V_{OLmin} at 25°C as shown in Figure 2.

5. **High Threshold Voltage** – V_{OHA} is the high output level sustained with the inputs of a device at input threshold voltages. A minimum value is given for V_{OHA} at the specification temperatures. V_{OHAmin} is used to define high level noise margin.

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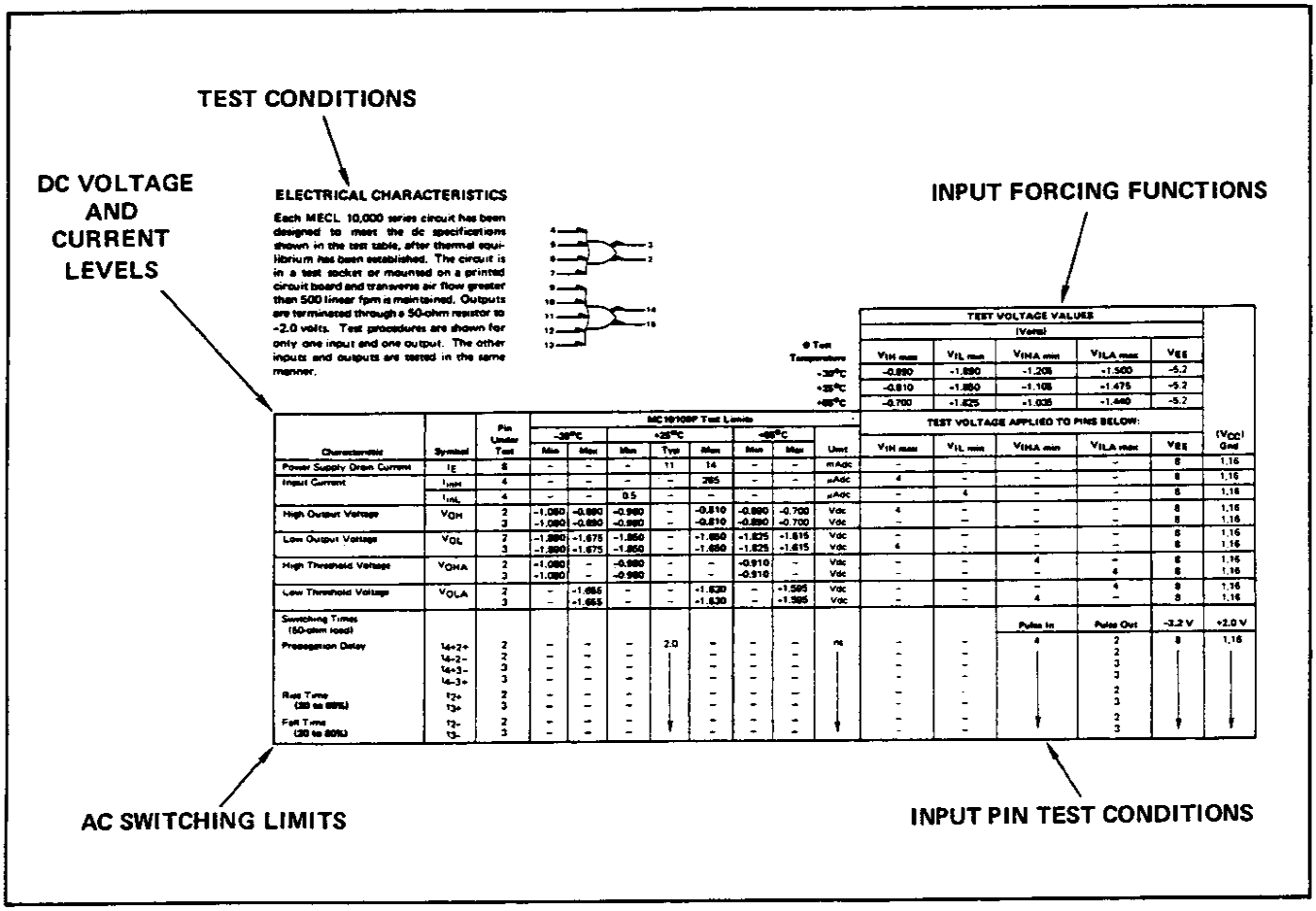

FIGURE 6 – Table of electrical characteristics for a MECL 10,000 gate package.

One or more inputs will be placed at V_{IHAmin} and/or V_{ILAmax} when testing V_{OHAmin}. These input levels determine the limits of the threshold region of the transfer curve. The logic configuration of the device will determine which inputs need to be placed at threshold voltages to test a given output.

6. **Low Threshold Voltage** – With the inputs of a device at input threshold voltages, V_{OLA} is the low output level of the device. A maximum value of V_{OLA} is specified at the given temperature. V_{OLAmax} is used to define low level noise margin. Similar to V_{OHAmin}, the logic configuration will determine which input pins are placed at input threshold voltages when testing V_{OLA}.

AC SWITCHING LIMITS

MECL 10,000 is a high speed logic family with gate delays (50% – 50%) and rise and fall times (20% – 80%) of approximately 2 ns. The edge speeds and short propagation delays require a special approach to testing and specifying limits.

Figure 7 shows a MECL 10,000 test fixture schematic for a gate device. Notice several features of the test circuit:

1. The outputs of the device are loaded directly to the input of an oscilloscope. The high speed of MECL 10,000 requires the use of a sampling oscilloscope for accurate measurement. The scope inputs have a 50 ohm input im-

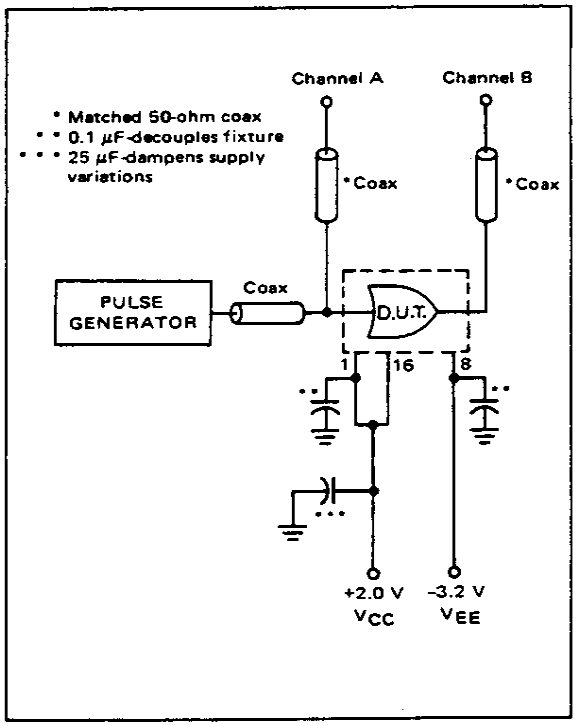

FIGURE 7 – MECL 10,000 test fixture schematic for a gate device.

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pedance which provide the proper loading termination.

2. The supply voltages are offset by +2 Vdc from the normal voltages (as used for dc specifications). Although MECL 10,000 outputs are specified driving 50 ohm loads to -2 V, the scope inputs have a 50 ohm impedance to ground. Therefore, the supply voltages are offset by +2 Vdc to load the outputs directly into the oscilloscope 50 ohm inputs. V_{CC} becomes +2 V and V_{EE} becomes -3.2 V.

3. The input and output cables to the oscilloscope are equal lengths of 50 ohm coaxial cable. The input signal from the pulse generator is stubbed-off to the input of the device; then the signal runs to the oscilloscope where it is terminated. The length of coaxial cable from the device input to the scope should be equal in length to the cable from the device output to the scope to maintain the original time relationship.

The data sheet of each MECL 10,000 device has a figure of the switching time test circuit and waveforms similar to Figure 8. The ac switching times (Figure 6) through a given logic path in a device. Times are measured from the 50% amplitude point of the input signal to the 50% amplitude point of the output signal. The waveforms of Figure 6 show the various delays t_{+-}, t_{++}, t_{-+}, t_{--} with the symbology denoting the transition direction of the input and output signals respectively.

2. **Rise and Fall Times (t_{X+}, t_{X-})**: The output signal is specified from the 20% and 80% points for rise and fall times. Rise time is measured from 20% to 80% of full output amplitude, and fall time vice versa. Other MECL families have these times specified 10% to 90%. MECL 10,000 with the designed-in "rounding" of the waveshape is difficult to measure accurately with the full 10% to 90% points, therefore, the 20% to 80% points are used.

Rise and fall times are also shown in Figure 8. The t_+ denotes a rising signal and t_- denotes a falling waveshape.

3. **Toggle Frequency (f_{tog})**: This is a measure of the maximum frequency at which a master-slave flip-flop will toggle. A minimum and/or typical number will be specified. The device will toggle from dc to at least the minimum frequency specified at the given temperature. A typical number is the frequency at which most devices will cease to toggle or output levels no longer remain in specified limits.

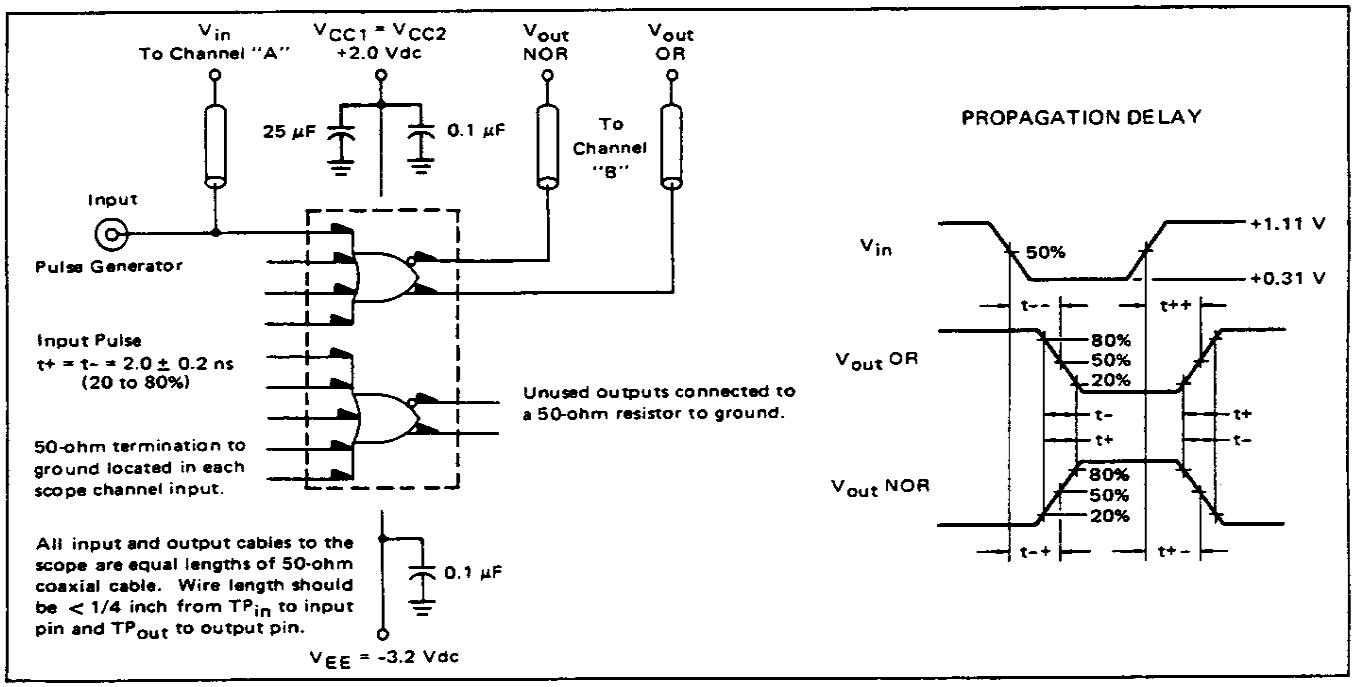

FIGURE 8 – Switching time test circuit and waveforms at 25°C.

of a device may be tested using its illustrated test circuit.

Notice that the input waveforms are offset by +2.0 Vdc due to the similar offset in power supply voltage. The high level becomes +1.11 V and the low level becomes +0.31 V.

The table of ac switching limits gives minimum, maximum and typical values for various parameters. Also, special conditions for each test are shown under input pin test conditions including input voltages, pulse in, and pulse out.

Various switching parameters are discussed below:

1. **Propagation Delay ($t_{X\pm\ y\pm}$)**: This parameter is a measure of the time needed for a signal to propagate

When testing toggle frequency, a test circuit similar to Figure 9 is employed. A type D flip-flop requires that the $\overline{Q}$ output be fed back to the D input. The $\overline{J}$ and $\overline{K}$ inputs of the MC10135 J-K flip-flop may be left open or put at a low logic state. More complex devices such as counters may require control inputs to be at proper levels to perform the count function.

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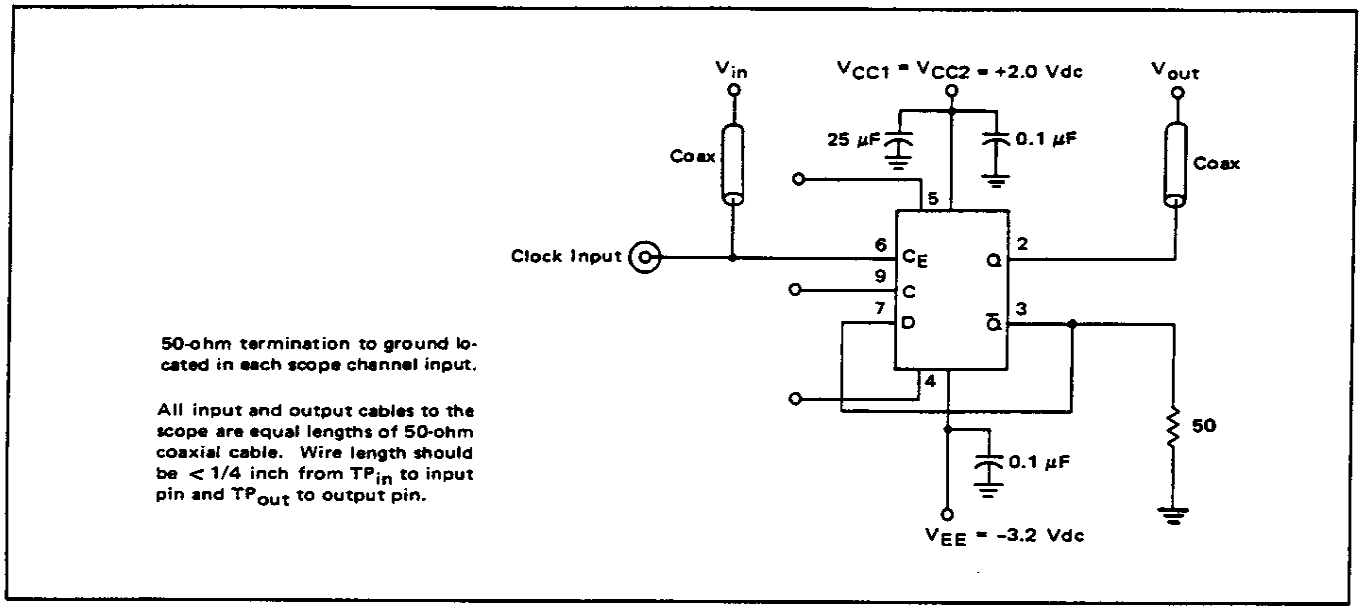

FIGURE 9 — Toggle frequency test circuit.

4. **Setup and Hold Times (t_{setup}, t_{hold})**: Any latch or flip-flop having a gated or clocked input has required setup and hold times. MECL 10,000 devices have two basic types of circuits which have setup and hold times specified.

The first device type is a latch circuit into which data is gated. The latch will allow information to ripple through as long as the gate (clock) input is at the required logic level. If the gate input goes to the opposite logic level, information will be stored in the latch and new data at the data input will be ignored.

The second type of device is an edge-triggered master-slave circuit (D type flip-flops, J-K flip-flops, counters, shift registers). Data cannot ripple through this device in a manner similar to the latch type circuit. Information is entered into the device on an edge transition of the clock.

Figure 10 shows setup and hold time definitions. Setup time is the minimum time before the transition of the clock pulse that information must be present at the data input (the figure shows a positive clock signal). Hold time is the minimum time after transition of the clock pulse that information must remain unchanged at the data input.

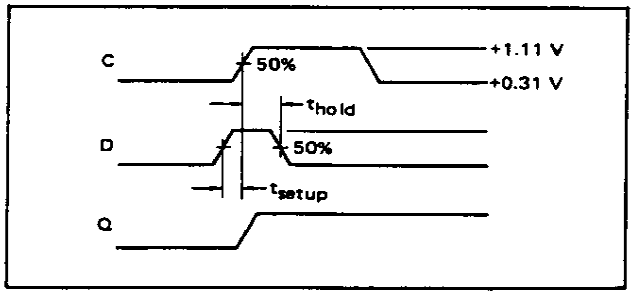

FIGURE 10 — Setup and hold time waveforms.

Information on a data input should not change for the sum of the setup and hold times. If the information changes during this total time, the operation of the device is in an indeterminate region. Therefore, proper data may or may not enter the device.

CONCLUSION

This application note has restricted discussion to information found on the basic data sheet. More information concerning maximum ratings, parameter symbols and definitions, and technical data may be found in the General Information Section of the "MECL Integrated Circuits Data Book" and the "MECL System Design Handbook." Also, circuit testing techniques for MECL 10,000 are discussed in Application Note AN-579.

The levels and noise margins discussed in the application note pertain to the commercial temperature range MECL 10,000 (-35°C to +85°C) but the same basic arguments apply to the full temperature range (-55°C to +125°C) devices.

REFERENCES

1. "MECL Integrated Circuits Data Book," Motorola Inc., November, 1972.
2. "MECL System Design Handbook", Motorola Inc. 2nd Edition, December, 1972.
3. AN-579, "Testing MECL 10,000 Integrated Logic Circuits," Motorola, Inc., 1972.

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