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Application Note

INTERCONNECTION TECHNIQUES FOR MOTOROLA'S MECL 10,000 SERIES EMITTER COUPLED LOGIC

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This application note describes some of the characteristics of high speed digital signal lines and gives wiring rules for MECL 10,000 emitter coupled logic. The note includes discussions of printed circuit board interconnects, board-to-board interconnects, and wirewrapping techniques.

MOTOROLA *Semiconductor Products Inc.*

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INTRODUCTION

As the digital integrated circuit market has become more mature, the need for very high speed logic elements has grown. Future machine designs demand a logic family with high clock rate capability, short propagation delays, and a minimum of layout constraints. From this need, the MECL 10,000 family of emitter-coupled logic has evolved – designed to be the most usable very high speed logic family available.

The 2.0 nanosecond gate propagation delay of MECL 10,000 gives the family a speed range between the older 4.0 nanosecond MECL II and 1.0 nanosecond MECL III families. Additional characteristics, such as low power dissipation (25 mW per gate function), and slow rise and fall times have eased the difficulties encountered in trying to balance system speed versus ease of design.

A MECL 10,000 system has the capability for clock rates in excess of 100 MHz. To permit such high speed operation, gate propagation delays must necessarily be short. However, to simplify wiring techniques and to minimize the use of transmission lines, rise and fall times have been kept to slower values.

MECL III still remains the industry standard as the highest speed logic family available. However the 1 nanosecond rise time of MECL III demands a transmission line environment. On the other hand, MECL 10,000 has been designed to approach the higher speed rates of MECL III, but with simpler wiring requirements.

The operational behavior of a MECL III gate with a rise time of 1 nanosecond (10%-90%) is shown in figure 1 for comparison. Figure 1a shows the difference in rise times when either gate is driving only a pulldown resistor. Figure 1b shows the same outputs driving an 8 inch signal line to a gate input. The MECL III gate shows severe ringing. This necessitates the use of a transmission line. The effect of the slower rise time of the MECL 10,000 gate is obvious in that ringing is not as severe. Herein, lies an advantage for the system designer using MECL 10,000 – that is, he may realize a very high speed system using only a minimum of transmission lines.

When driving long lines or large fanouts at maximum frequency, transmission lines are needed. MECL 10,000 has the capability to drive such lines. Also, the family is specified to be completely compatible with MECL III in the 16-pin dual-in-line packages. As a result, MECL 10,000 can be used to obtain maximum versatility with low power and ease of layout design.

The following discussion is intended to give the system designer insight into these problem areas: The use of non-transmission line interconnections; the characteristics of transmission lines which affect MECL interconnections; and the techniques used for transmission lines. Other considerations to be made for system interconnections are also discussed, such as noise margins, clock driving, wire wrapping, and party line techniques.

SIGNAL LINE CONSIDERATIONS

The purpose of an interconnection line in any digital system is to transmit information from one point of the system to another. When information on a signal line changes, a finite amount of time is necessary for the information to travel from the sending end to the receiving end of the line. As the circuit speed becomes faster and clock rates increase, the dynamic behavior of the interconnection line becomes increasingly important. The rise and fall times of the logic elements, loading effects, delay times of the signal paths, and the various other transient characteristics, all affect reliable operation of the system. The effects of these factors and the advantages of the dynamic characteristics of MECL 10,000 are perhaps best shown by briefly investigating the transmission line qualities of a signal path.

In figure 2a is shown a simple interconnection circuit. A MECL 10,000 gate is shown driving a line of length ℓ, to another gate with a pulldown resistor, R_L. If the loading effect of the receiving gate is disregarded for the moment (input impedance is very large with respect to R_L), the same line could be modeled as shown in figure 2b.

The driving gate is modeled as a voltage source with output impedance, R_o. The signal line will exhibit an impedance to a transient signal which is called its characteristic impedance, Z_o. If the line is not a regular transmission line, Z_o will vary somewhat. However, for this example let us assume Z_o is constant.

When the output of the driving gate changes state, the voltage at point A is a function of the internal voltage swing, V_{INT}, output impedance, and line impedance:

$$V_{A(t)} = V_{INT(t)}\left(\frac{Z_o}{R_o + Z_o}\right).$$

For MECL 10,000, R_o is small with respect to the line impedance, so the output swing is nearly the same as the input transition – typically 800 mV. The signal will prop-

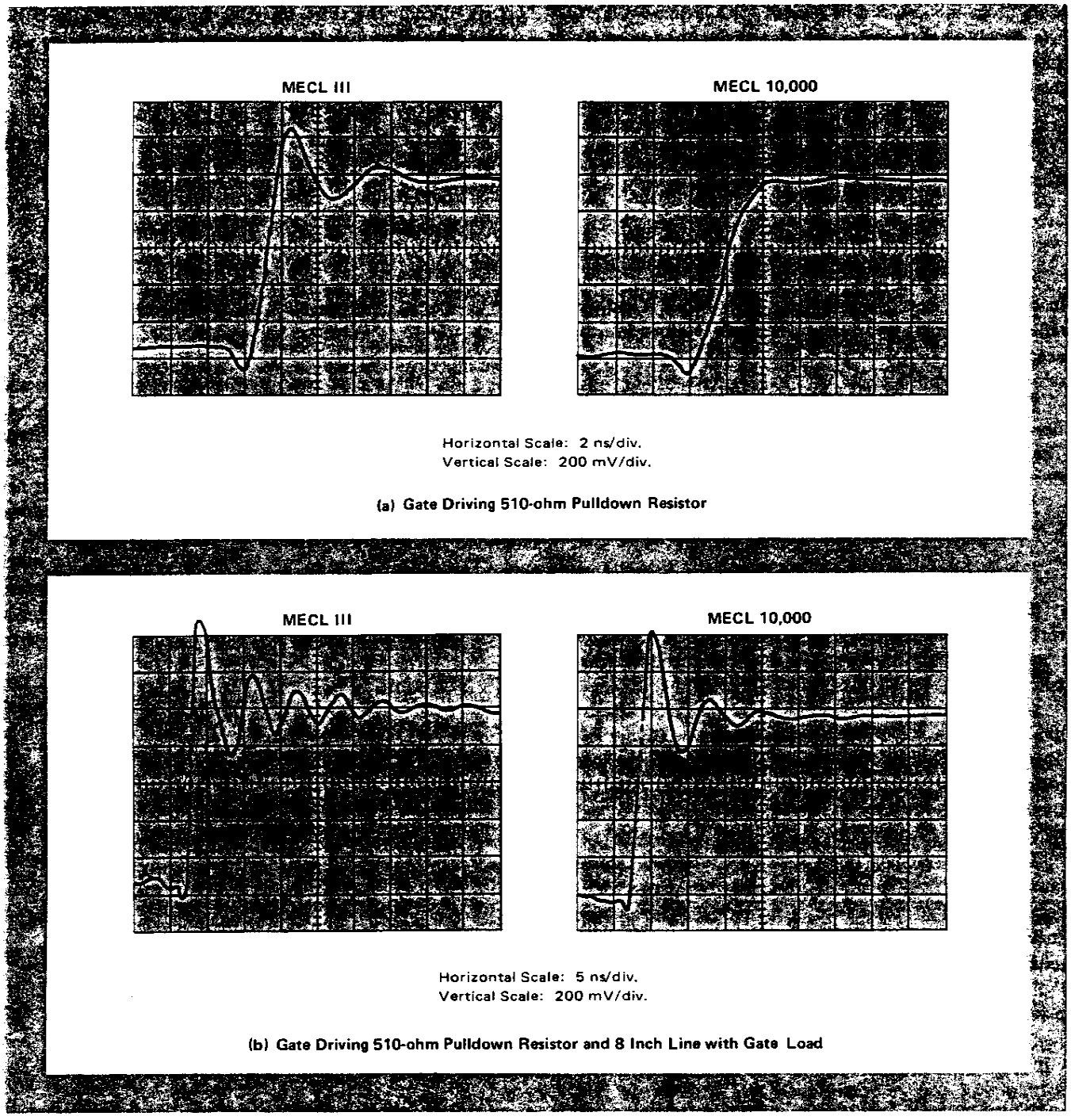


FIGURE 1 – Comparison of MECL III and MECL 10,000 Waveforms

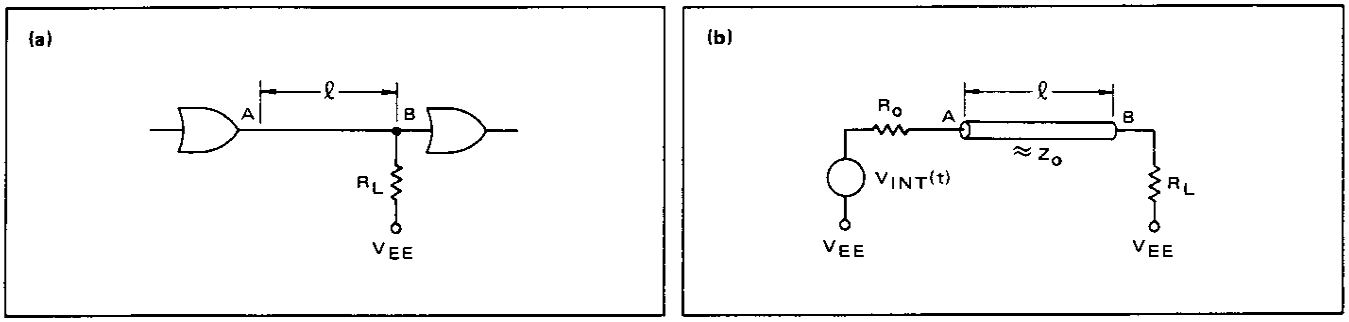


FIGURE 2 – MECL 10,000 Interconnection Circuit

agate down the line and be seen at point B time T_D later. The signal, when reaching the end of the line (point B), may be reflected and returned toward the sending end of the line. The reflected voltage is:

$$V_A' = \rho_L V_A,$$

where ρ_L is the reflection coefficient,

$$\rho_L = \frac{R_L - Z_o}{R_L + Z_o}.$$

In the special case where $R_L = Z_o$, then $\rho_L = 0$ and the reflected voltage is zero. In this situation the load resistor exactly matches the characteristic impedance of the line, so no reflection occurs.

When reflection does occur, it returns to point A at time 2 T_D, where T_D is the one-way line propagation delay. The sending end will again reflect this voltage with a reflection coefficient, ρ_S, given by:

$$\rho_S = \frac{R_o - Z_o}{R_o + Z_o}.$$

The reflected signal will continue to bounce back and forth between the ends of the signal line, gradually diminished in amplitude by reflection coefficients and the resistance in the line.

Now consider a second line in which the load resistor has been moved to the sending end of the line (figure 3a). This model is altered from the first only in that the load resistor is seen at the driver output. When the output of the driving gate changes state, the output swing, V_A, will be typically 800 mV.

The signal reaching point B will be reflected (as discussed). The coefficient, ρ_L, becomes worst case (≈ 1) because the input impedance of the receiving gate is high. In such a case the reflection will be large. As the reflection returns to point A at time 2 T_D, the reflection coefficient, ρ_S, comes into play. Its value will be very close to the previous case:

$$\rho_S = \frac{\frac{R_o R_L}{R_o + R_L} - Z_o}{\frac{R_o R_L}{R_o + R_L} + Z_o} \approx \frac{R_o - Z_o}{R_o + Z_o},$$

since R_o is small compared to R_L.

The reflections, as before, continue to bounce back and forth on the line getting successively smaller in amplitude. The result is that ringing appears on the signal line (figure 3c).

Rise time effects may be understood by considering the delay time of the line. If the line length ℓ is sufficiently short, the first reflections are seen at the sending end of the line while the driver is still changing state. The reflections are hidden by the rising edge of the pulse, and ringing is reduced. Therefore, the slow rise time of MECL 10,000 permits longer line lengths to be used before trouble with ringing is encountered.

This second signal line example is called an open line or an unterminated line. To limit undershoot to about 12 percent of the logic swing, the maximum open line length permitted would be:

$$L_{max} = \frac{t_r}{2t_{pd}},$$

where: t_r = Rise time of driving gate (ns) (20% - 80%)
t_{pd} = Propagation delay per unit line length (ns/in).

The above expression may also be used to show the effect of loading on an interconnection. t_{pd} is dependent on the rate of signal propagation on the line; the rate is controlled by the type of line and the loading on the line. MECL inputs are high impedance and capacitive in net reactance (3 to 5 pF per input). Increased loading slows the rate of propagation of the line and decreases allowable open line length. That is, as fan-out increases, the maximum open line length decreases for acceptable undershoot.

To understand how ringing and undershoot affect system operation, it is helpful to define guaranteed noise mar-

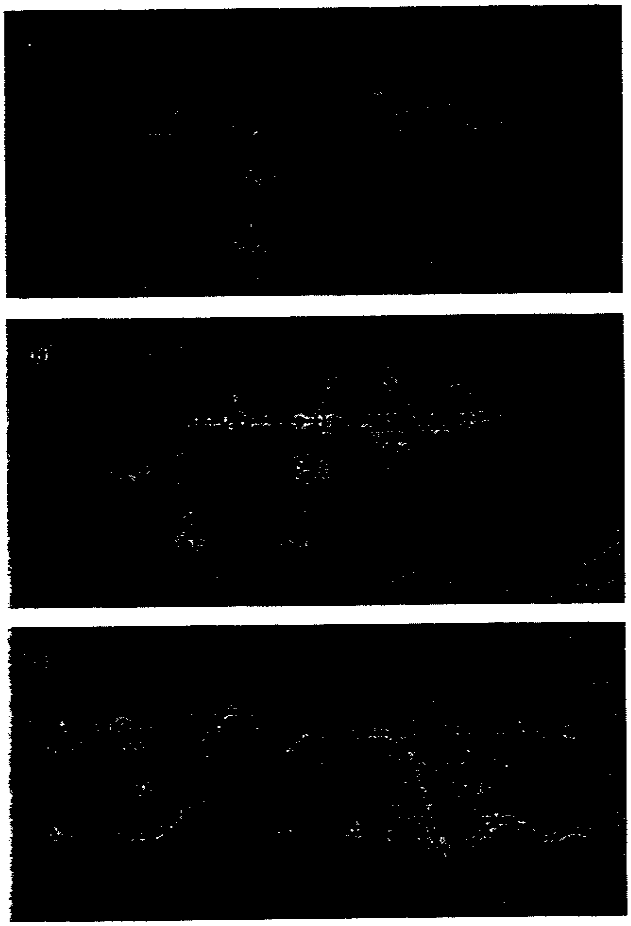


FIGURE 3 – MECL 10,000 Interconnection with Load Resistor at Sending End of Line

gins. Noise margin is defined as the difference between a worst case input logic level (V_{OHAmin} or V_{OLAmax}) and the worst case threshold (V_{IHAmin} or V_{ILAmax}) for the corresponding logic level. Guaranteed noise margins (N.M.) for MECL 10,000 at 25°C are:

$$\text{Logic 1 N.M.} = V_{OHAmin} - V_{IHAmin} = -0.980 - (-1.105) = 125 \text{ mV};$$

$$\text{Logic } \emptyset \text{ N.M.} = V_{ILAmax} - V_{OLAmax} = -1.475 - (-1.630) = 155 \text{ mV}.$$

However, using typical logic levels of -0.900 volts and -1.700 volts, the nominal voltage margins are greater than 200 mV for both logic levels.

For system design, worst case conditions should be considered. If so, a 125 mV noise margin becomes the design limit. This voltage margin protects against signal undershoot, power supply variations, and system noise. Good circuit interconnections should limit maximum undershoot to less than 100 to 110 mV to provide a design safety margin.

Other factors – such as line impedance and placement of loads on the line – also affect ringing of signals. A long and elaborate discussion would be necessary to describe all of the varying effects, and the description here is only intended to give a brief idea of the many factors involved. When line lengths and fanout go beyond limits (which will be defined), techniques such as twisted pair lines and terminated lines may be used.

PRINTED CIRCUIT BOARD INTERCONNECTS

Layout rules needed for designing with MECL 10,000 depend mainly on the design goals of the system user. MECL 10,000 may be used in layouts ranging from single layer printed circuit (PC) board with wired interconnects, to the most elaborate multilayer board with a complete transmission line environment. Optimization of system layout will include considerations of the system size, desired performance, and cost.

Use of a ground plane is a suggested procedure whenever possible. A ground plane is beneficial for maintaining a noise free voltage plane for the V_{CC} supply, and for maintaining constant characteristic impedance whenever transmission lines become necessary. A ground plane may be established by using single sided board with wired interconnects, or by using double or multilayer PC board.

WITHOUT GROUND PLANE

In small systems where the number of interconnects and the package density are high, it is difficult to reserve a large ground plane area without the use of multilayer board, a costly approach. However, MECL 10,000 may still be used with good system performance if certain guidelines are followed:

(1) V_{CC} should be bussed to the V_{CC} pins of each package. Bus lines should be as wide as possible with a width of 0.1 inch minimum per row of packages. If an edge connector is used, V_{CC} should be pinned out to several connector pins.

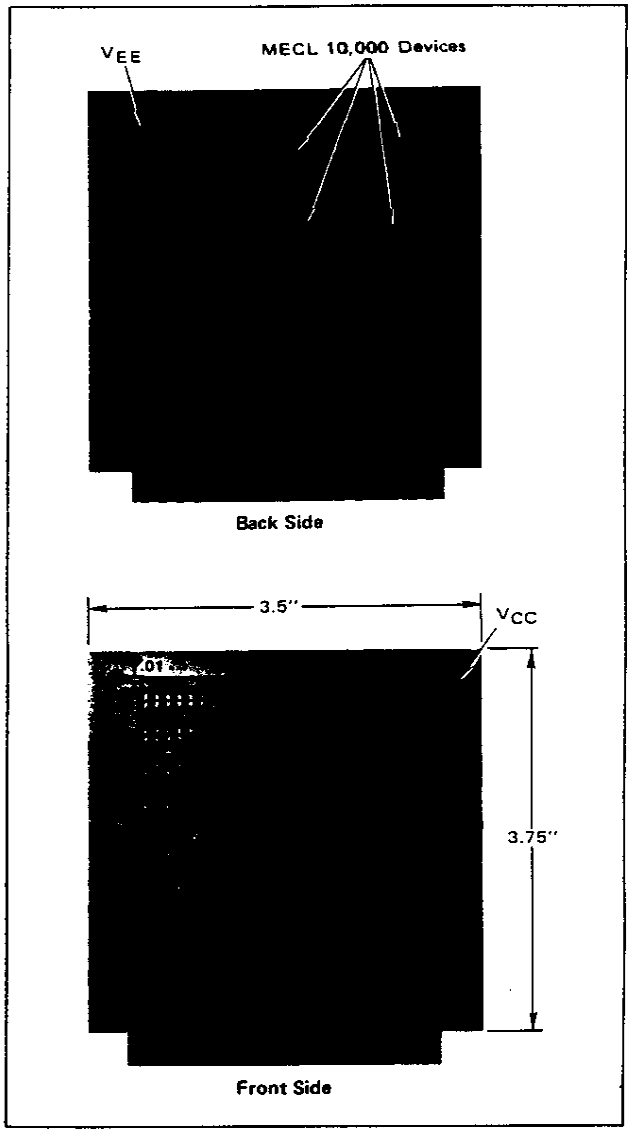


FIGURE 4 – Printed Circuit Board for MECL 10,000 System Without Ground Plane

(2) V_{EE} should also be bussed, if possible, to pin 8 of each package (pin 12 of the 24 pin package). When V_{EE} is brought onto the board via an edge connector, the V_{EE} line should be in close proximity to a V_{CC} pin for easy bypassing.

(3) Each device should be bypassed between the V_{CC} and the V_{EE} pins with a low inductance 0.01 μF capacitor.

(4) Logic interconnecting lines should be kept to minimum length. A maximum line length of 6 inches is suggested; ringing will begin to get too severe with longer line lengths. For line lengths greater than 6 inches, signal lines with series damping resistors are necessary (similar to those shown in figure 13).

(5) For high fanout (8 or greater) and high speed clock distribution, twisted pair lines or coaxial cable should be used. Both of these techniques are described in detail later.

Figure 4 shows a double-sided PC board in which the above rules are illustrated. Several MECL 10,000 devices are

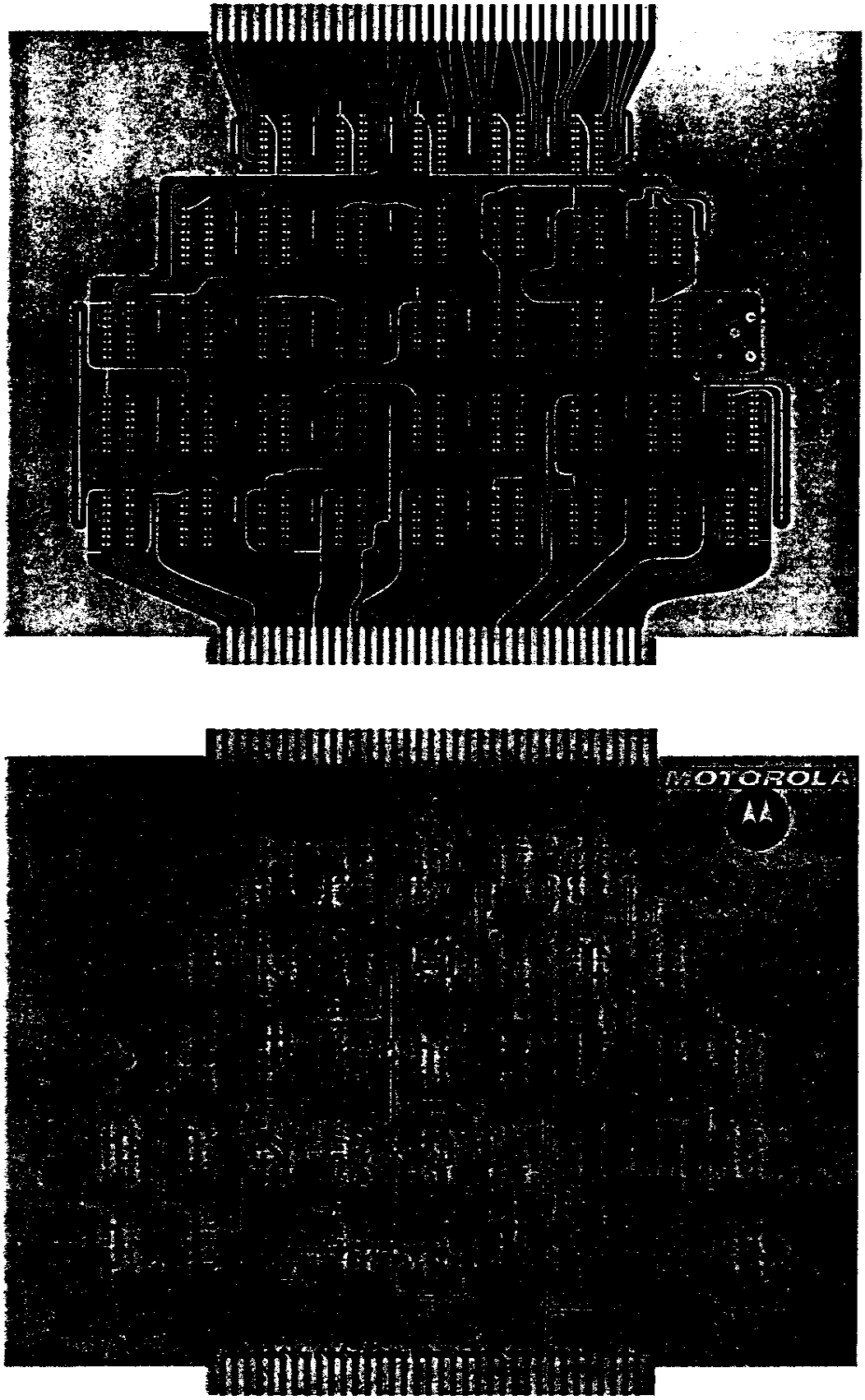


FIGURE 5 – MECL 10,000 PC Board With Ground Plane

used with MTTL in a high speed counter, in which the MECL and MTTL are operated by a common voltage supply. Notice that V_{EE} and V_{CC} are both bussed to the package and that bus lines are as wide as conveniently possible. Two 0.1 μF capacitors are used for low frequency bypassing on the board. Each MECL 10,000 device is bypassed with a 0.01 μF capacitor, and additional bypassing is scattered through the MTTL circuitry. Note that signal lines are short and no transmission lines are used.

WITH GROUND PLANE

A ground plane allows best performance for a MECL 10,000 system. The ground plane serves two purposes. First, it provides a constant characteristic impedance (Z_o) to signal interconnections; secondly, it provides a low inductance path for ground currents on the V_{CC} supply. As with systems which have no ground plane, certain design guidelines are recommended as follows:

(1) The ground plane (V_{CC}) need not cover 100% of the board surface. Approximately 30 to 40% of the ground area may be removed for signal interconnections, as illustrated in figure 5. When using edge connectors, the ground plane should be pinned out to about every seventh connector pin.

(2) The V_{EE} supply should be bussed if possible, to pin 8 of each package. Bus line width at any point should be a minimum of 0.1 inch. Where possible, the V_{EE} supply should be extended to a plane under the signal lines etched on the ground plane side of a two-sided circuit board. If V_{EE} is a plane under these lines, they will exhibit a constant characteristic impedance. This technique is also shown in figure 5.

(3) Bypassing need not be as extensive as on a board without a ground plane. Provide a low inductance 0.01 μF capacitor every two to six packages, depending upon how extensive the ground plane is. As a rule if the ground plane covers less than 50% of the board area, then bypass every two packages. On two-sided systems or multilayer systems where 100% ground plane is present, only one capacitor for every four to six packages is needed.

(4) In practice, the majority of board interconnects are shorter than six inches, with fanouts four or less. As discussed, the rise and fall times of MECL 10,000 allow these lines to be treated as unterminated transmission lines requiring only a pull-down resistor. Normally, a 510-ohm resistor to V_{EE} is used. (Detailed limits for interconnections are provided as a function of line impedance and fanout in the following section).

(5) For high fanout and high speed clock distribution, terminated transmission lines or twisted pair lines should be used. These techniques are discussed in the following sections.

TRANSMISSION LINE GEOMETRIES

With a ground plane present, three types of transmission line geometries are feasible: wire over ground; microstrip line; and strip line. The following sections summarize the characteristics of each type of line.

(1) Wire over ground – The cross section of a wire over a ground is shown in figure 6a. The characteristic impedance of the wire is:

$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4h}{d}\right),$$

where e_r is the effective dielectric constant surrounding the wire. The wire over ground plane is useful for breadboard layouts (as with single-sided board) and for backplane wiring. The characteristic impedance of a wire over ground plane will be about 120 ohms with variance depending on the wire size, type of insulation, and distance from the ground plane.

(2) Microstrip lines – A microstrip line (figure 6b) is a strip conductor separated from a ground plane by a dielectric medium. Two-sided and most multilayer boards use this type of transmission line. If the thickness, width, and height of the line above the ground plane are controlled, the line will exhibit a characteristic impedance of:

$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8\,w + t}\right).$$

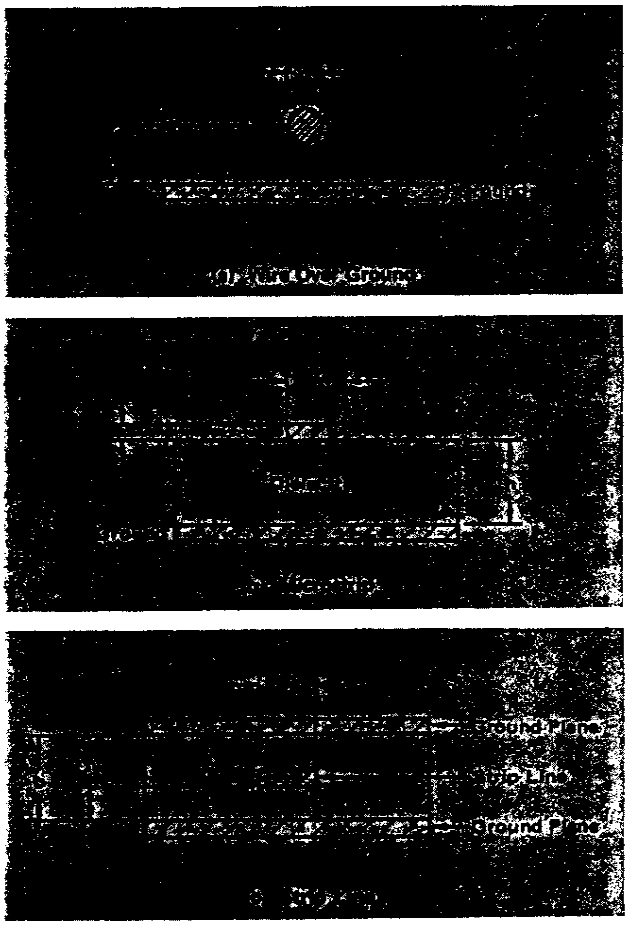


FIGURE 6 – Transmission Line Geometries

Here e_r is the dielectric constant of the board. For standard G-10 fiberglass epoxy boards the dielectric constant is about 5.0.

The signal line is obtained by etching unwanted copper from the board using photo resist techniques. A characteristic impedance can easily be controlled to within 10 percent.

As mentioned above, board thickness and dielectric constant affect line impedance. Figure 7 gives a table of values for characteristic impedance versus line width for 0.031" and 0.062" G-10 board with one ounce copper (widths for two ounce copper are nominally 1 to 2 mils narrower).

The propagation delay of microstrip line may be calculated by:

$$t_d = 1.017 \sqrt{0.475\, e_r + 0.67} \text{ ns/ft.}$$

Note that the propagation delay of the line depends only on the dielectric constant and is not a function of line width or spacing. For G-10 fiberglass epoxy boards (e_r = 5.0) the propagation delay of the microstrip line is calculated to be 1.77 ns/ft.

FIGURE 7 – Microstrip Characteristic Impedance versus Line Width for One Ounce G-10 Fiberglass Epoxy Board

Z_o (OHMS)	LINE WIDTH (MILS) (Dimension w of Figure 6b)	
	0.062" BOARD	0.031" BOARD
50	103	47
55	89	41
60	77	35
65	66	30
70	57	26
75	49	22
80	42	19
85	36	16
90	31	14
95	27	11
100	23	10

(3) Strip Line – A strip line (figure 6c) is a copper ribbon centered in a dielectric medium between two conducting planes. This type of line is used in mutlilayer boards and is not seen in most systems. Multilayer boards are justified when operating MECL 10,000 at top circuit speed, and when high density packaging is a system requirement. Since most designers need not concern themselves with strip lines, little is presented here about them. A detailed discussion of strip lines is presented in the "MECL System Design Handbook," reference 1.

UNTERMINATED LINE LIMITS

As previously mentioned, a MECL signal line may be considered as an unterminated transmission line. Rise time, characteristic impedance of the line, and loading affect the maximum interconnection length for unterminated lines. Figure 8 shows a tabulation of suggested maximum open line lengths for various fanouts and line impedances.

The tabulated values were calculated for limiting overshoot to 35% of the logic swing, or undershoot to 12% (whichever was the limiting factor under specified conditions). Severe overshoot can slow down clock rates, and severe undershoot can result in reduced noise immunity. The transmission line model of figure 3 was used in calculations.

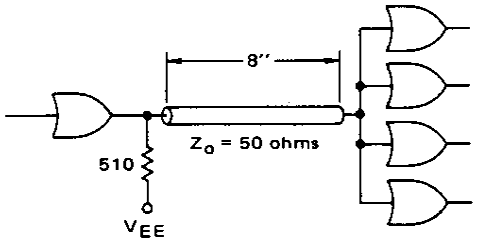
As an example of how the table of line limits may be used, consider a system layout using 0.062" board (G-10 fiberglass epoxy). Assume that signal interconnection widths may be from 25 to 40 mils wide. If a ground plane is used on one side of the system PC board, all system interconnects would show a corresponding characteristic impedance. The wide line (40 mils) is preferable since Z_o would be 82 ohms which is lower than that for a 25 mil line ($Z_o \approx 97$ ohms) and the lower impedance allows a longer maximum length line. The lower impedance line with a fanout of 4 would then have a suggested maximum length of about 4.2 inches. On normal system-sized PC boards (5"x7"), the majority of signal line interconnections will be less than 4 inches in length if the system layout is well planned.

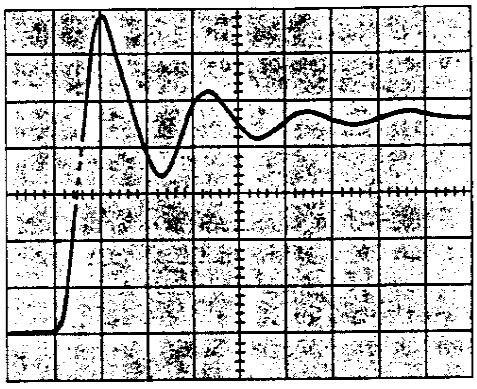
FIGURE 8 – Maximum Unterminated Line Length for MECL 10,000 to Maintain Less Than 12% Undershoot

	Z_o (OHMS)	FANOUT = 1 (2.9 pF)	FANOUT = 2 (5.8 pF)	FANOUT = 4 (11.6 pF)	FANOUT = 8 (23.2 pF)
		ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)
MICROSTRIP (Propagation Delay 0.148 ns/in.)	50	8.3	7.5	6.7	5.7
	68	7.0	6.2	5.0	4.0
	75	6.9	5.9	4.6	3.6
	82	6.6	5.7	4.2	3.3
	90	6.5	5.4	3.9	3.0
	100	6.3	5.1	3.6	2.6
BACKPLANE (Propagation Delay 0.140 ns/in.)	100	6.6	5.4	3.8	2.8
	140	5.9	4.3	2.8	1.9
	180	5.2	3.6	2.1	1.3

An interconnection with the pulldown resistor at the sending end of the line is the worst case situation for an unterminated line. If unterminated interconnection lengths are extended beyond the suggested limits, overshoot and undershoot are increased. The lengths given are calculated so that undershoot never exceeds the guaranteed noise margins, although typically noise margins are much greater than specified.

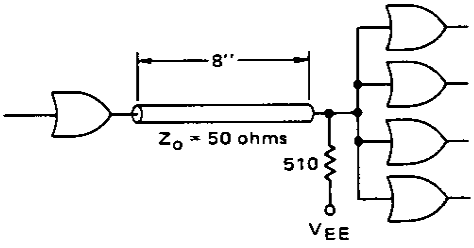
(a) 510-ohm Resistor at Sending End

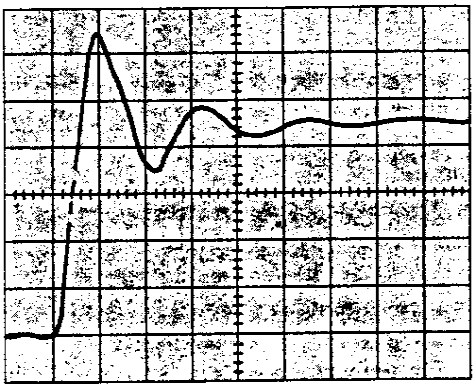




Scale: Horizontal = 5 ns/div., Vertical = 200 mV/div.

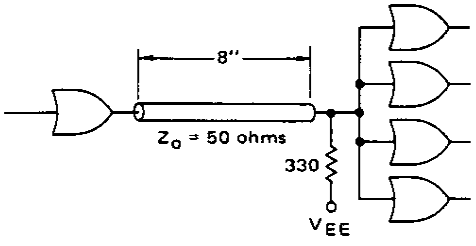
(b) 510-ohm Resistor at Receiving End

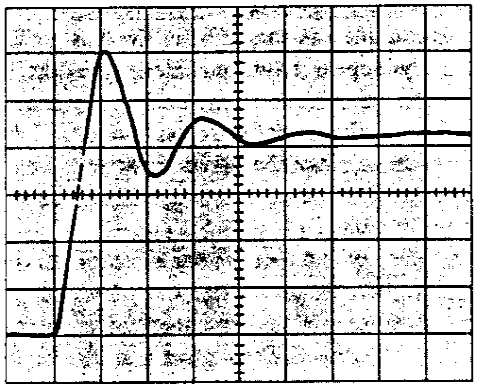




Scale: Horizontal = 5 ns/div., Vertical = 200 mV/div.

(c) 330-ohm Resistor at Receiving End





Scale: Horizontal = 5 ns/div., Vertical = 200 mV/div.

FIGURE 9 – Gate Driving 8-Inch 50-ohm Line with Fanout of 4

Overshoot and undershoot may also be reduced by locating the pulldown resistor at the receiving end of the line. If the pulldown resistor is moved to the receiving end, the reflection coefficient (ρ_L) is reduced. This reduces ringing.

Figure 9 shows the signal at the receiving end of an 8-inch 50-ohm line with a fanout of 4. In figure 9a, a 510-ohm pulldown is at the sending end of the line. Figure 9b has a 510-ohm pulldown at the receiving end, while figure 9c has a 330-ohm pulldown at the receiving end. The overshoot and undershoot are successively reduced in the latter two cases.

For worst case, the reflection coefficient is approximately equal to one ($\rho_L \approx 1$). For the best case shown, using a 330-ohm pulldown, $\rho_L = (330 - 50)/330 + 50) = 0.74$, which represents an improvement of about 25%. In comparing the waveforms, notice that overshoot is reduced by roughly the same percentage (9c versus 9a).

The tabulated values of figure 8 are not necessarily absolute limits for unterminated lines. Longer unterminated lines may be used if the pulldown resistor is moved to the receiving end of the line, or if increased overshoot and undershoot are acceptable.

TRANSMISSION LINE TERMINATION TECHNIQUES

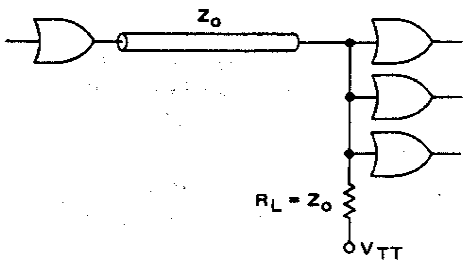
Proper transmission line termination prevents reflections on the line, so ringing does not occur. As a result, interconnection lengths are only limited by attenuation, bandwidth, etc. MECL transmission line interconnections utilize several techniques.

(1) Parallel Termination – A transmission line will have a reflection coefficient, (ρ_L), of zero when driving a load impedance equal to its characteristic impedance. MECL 10,000 can source current for driving a 50-ohm characteristic impedance line with the line terminated by 50 ohms to -2 volts. The termination voltage (V_{TT} = -2 volts) is necessary since 50 ohms loaded to V_{EE} would use excessive current. Figure 10 illustrates parallel termination.

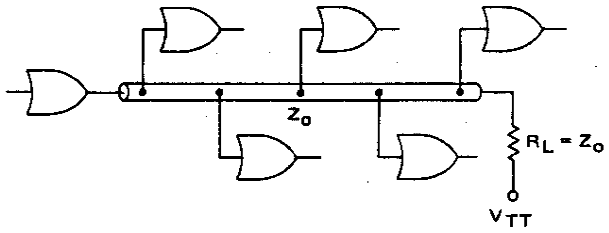
Gate inputs may be distributed along the transmission line (10b), and do not have to be lumped at the end of the line (10a). The gate inputs appear as high impedance stubs to the transmission line and should be as short as possible. While inputs may appear anywhere along the line, the terminating resistor should be at the end of the line. As fanout with this configuration increases, the edge of the waveform slows down, since the signal drives an increasing amount of capacitance. The waveform is undistorted along the full length of the line.

For large systems where total power is a consideration, all lines should be parallel terminated to a -2 volt supply. This is the most power-efficient manner for terminating MECL circuits. The drawback is of course, the requirement for an additional power supply.

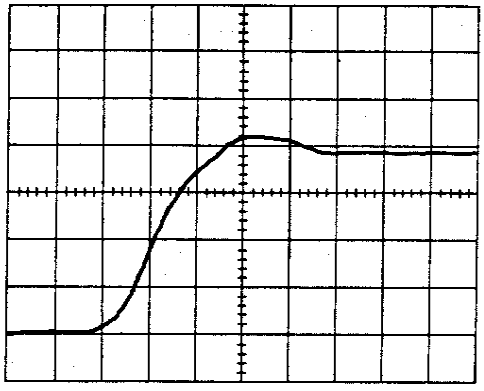
An alternate approach is to use two resistors – as shown in figure 11. The Thevenin equivalent of the resistor network is a resistor equal to the characteristic impedance of the line, terminated to -2 Vdc. R1 and R2 may be calcu-



(a) Parallel Terminated Line with Lumped Fanout



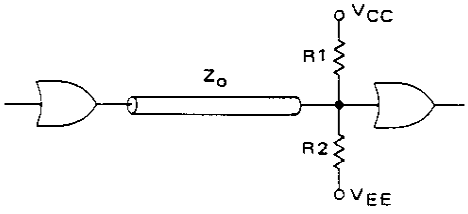
(b) Parallel Terminated Line with Distributed Fanout



Horizontal Scale = 2 ns/div. Vertical Scale = 200 mV/div.

(c) Waveform at Receiving End of Line

FIGURE 10 – Parallel Termination



THEVENIN EQUIVALENT RESISTORS FOR TERMINATION

Z_o (OHMS)	R1 (OHMS)	R2 (OHMS)
50	81	130
70	113	182
75	121	195
80	130	208
90	146	234
100	162	260
120	194	312
150	243	390

FIGURE 11 – Parallel Termination Using a Thevenin Equivalent Resistor Network

lated as follows:

$$R2 = 2.6\ Z_O;$$

$$R1 = \frac{R2}{1.6}.$$

(2) Series damping and series termination – A series terminated line eliminates reflections at the sending end of the line. Series termination is accomplished by inserting a resistor in series with the output of the gate as shown in figure 12. The resistor value plus the circuit output impedance is made equal to the impedance of the transmission line.

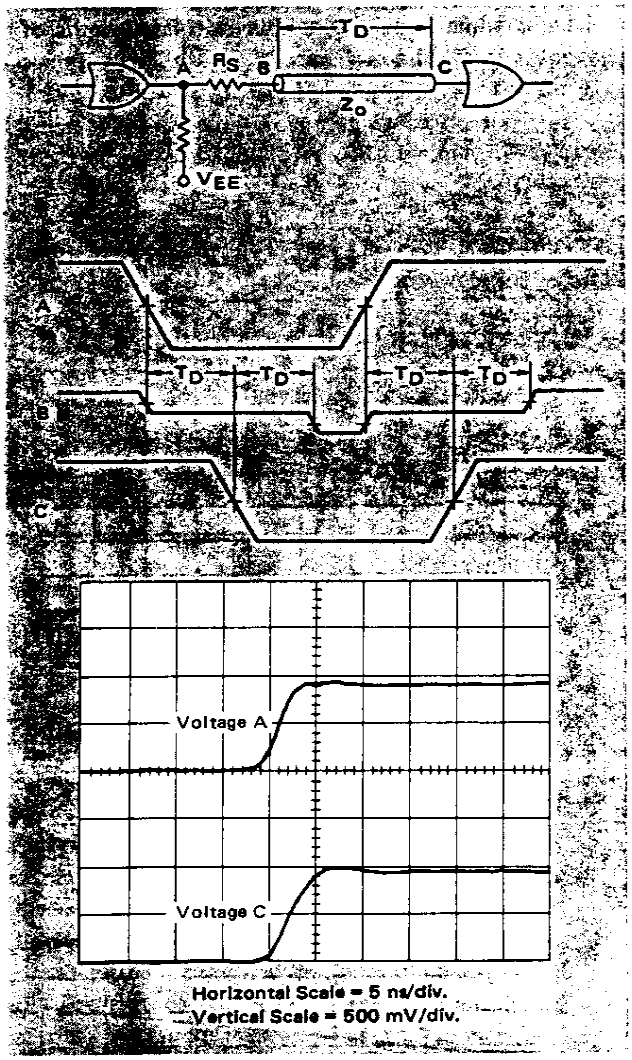


FIGURE 12 – Series Termination and Waveforms

The dc output impedance is 7 ohms for a MECL 10,000 gate. Therefore, the value of R_S should be equal to Z_O minus 7 ohms.

At time t = 0, the internal voltage switches to the low-state which represents a change of 0.8 to 0.9 volts (ΔV_{INT} = -0.8 to -0.9 volts). The voltage change at point B can be expressed as:

$$\Delta V_B = \Delta V_{INT} \frac{Z_O}{R_S + R_O + Z_O},$$

where R_O is the output impedance of the gate.

Since $R_S + R_O$ is made equal to Z_O, the voltage change at B is 1/2 the voltage, ΔV_{INT}. It takes the propagation delay time of the transmission line, T_D, for the waveform to reach point C, where the voltage doubles due to the unity reflection coefficient at the end of the line. The reflected voltage, which is equal to the sending voltage, arrives back at point B at time 2 T_D. No more reflections occur if $R_S + R_O$ is equal to Z_O. Similar waveforms occur when the driving gate switches to the high state.

An advantage of using series terminated lines is that only one power supply is required. The Thevenin equivalent parallel termination technique also uses only one supply, but requires more overall power. A disadvantage of series termination is that distributed loading along the line cannot be used because of the half-voltage waveform traveling down this line (see figure 12, waveform B). A number of lumped loads may be placed at the end of the terminated line as far as reflection at the receiving end is concerned, since a full initial signal transition is observed at this point and all subsequent reflections will be absorbed at the source.

The disadvantage of using only lumped loading at the end of a series terminated line can be eliminated at the expense of more lines (figure 13). As shown, there are n transmission lines for parallel fanout. The value of R_S should be the same as discussed previously for the emitter pulldown resistor, in which case n was equal to one.

The value of R_E, will be determined by the number of lines in the following way. R_E must be small enough to supply each transmission line with the proper voltage level. If R_E is too large, the output transistor will turn off when switching from the high to the low voltage state. The maximum value of R_E is given by:

$$R_{E(max)} = \frac{10\ Z_O - R_S}{N}.$$

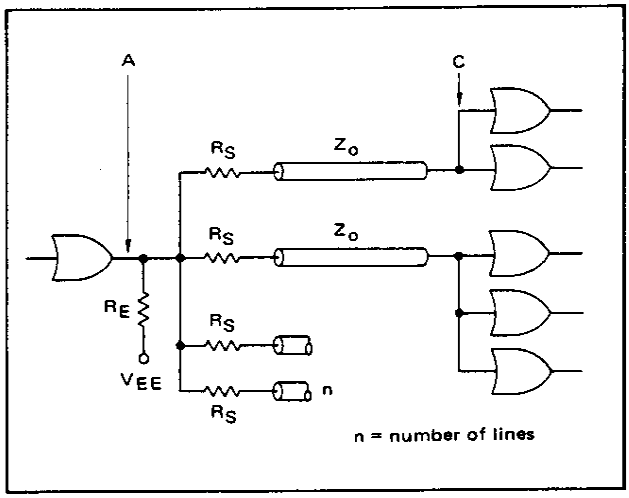


FIGURE 13 – Parallel Fanout with Series Termination

Figure 14a shows the gate output fall time (voltage A) and the fall time at the end of the line (voltage C) when N = 1, Z_o = 50 ohms, R_E = 1 k ohms, R_S = 43 ohms, and fanout = 3. The "steps" in the fall time waveform are due to the output device turning off because R_E is too large. Figure 14b shows the fall time when R_E = 290 ohms ($R_E < R_{E(max)}$).

The fanout at the end of a series terminated line is limited by the value of the series resistor, R_S. In the high state a voltage drop occurs across the series resistor:

$$V_S = (\text{fanout}) \times (\text{input current}) \times R_S .$$

The input current to a MECL 10,000 gate is typically about 160 μA. If the fanout were 4 and R_S were 43 ohms for a 50 ohm line, V_S would equal about 28 mV. Noise margin would typically be cut by that amount. As fanout or the value of R_S increases, V_S increases and results in lower noise margins.

Series damping may also be used to reduce overshoot and ringing. Series damping is similar to series termination in that a small series resistor is used to reduce ringing rather than to completely terminate ringing. The resistor is smaller than the characteristic impedance of the line and it may be used to increase line length for the worst case open line (that is, R_S = 0) as shown in figure 8.

Series damping may also be used for greatly extended line lengths while remaining within calculated limits of overshoot and undershoot. Figure 15 gives minimum values of R_S needed for various line impedances to limit overshoot to 35% of signal swing, or undershoot to 12%. Using these values of minimum R_S, very long lines may be used.

50	9
68	18
75	21
82	25
90	29
100	34
120	43
140	53
160	63

FIGURE 15 – Minimum Values of R_S for Any Length Line, for Less Than 35% Overshoot or 12% Undershoot

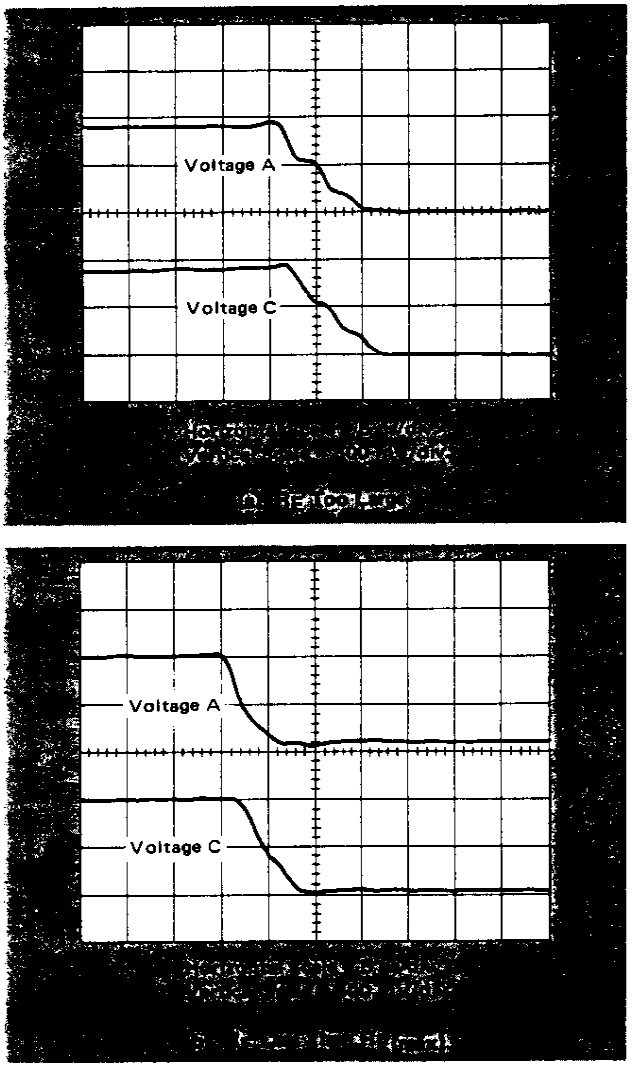


FIGURE 14 – Series Termination Fall Times

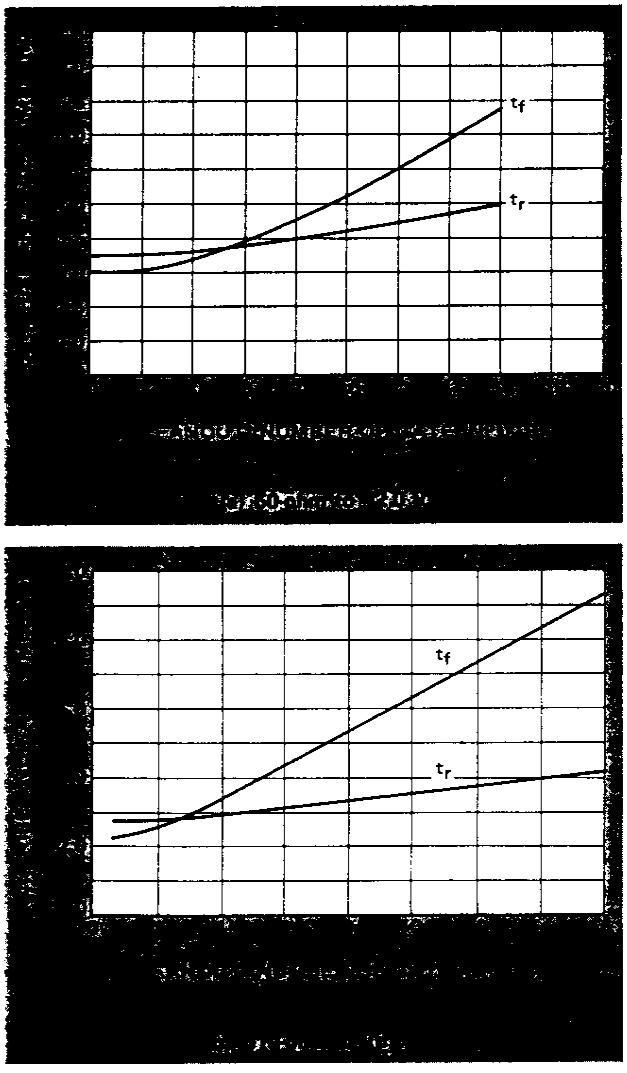


FIGURE 16 – Rise and Fall Time (10 to 90%) versus Fanout

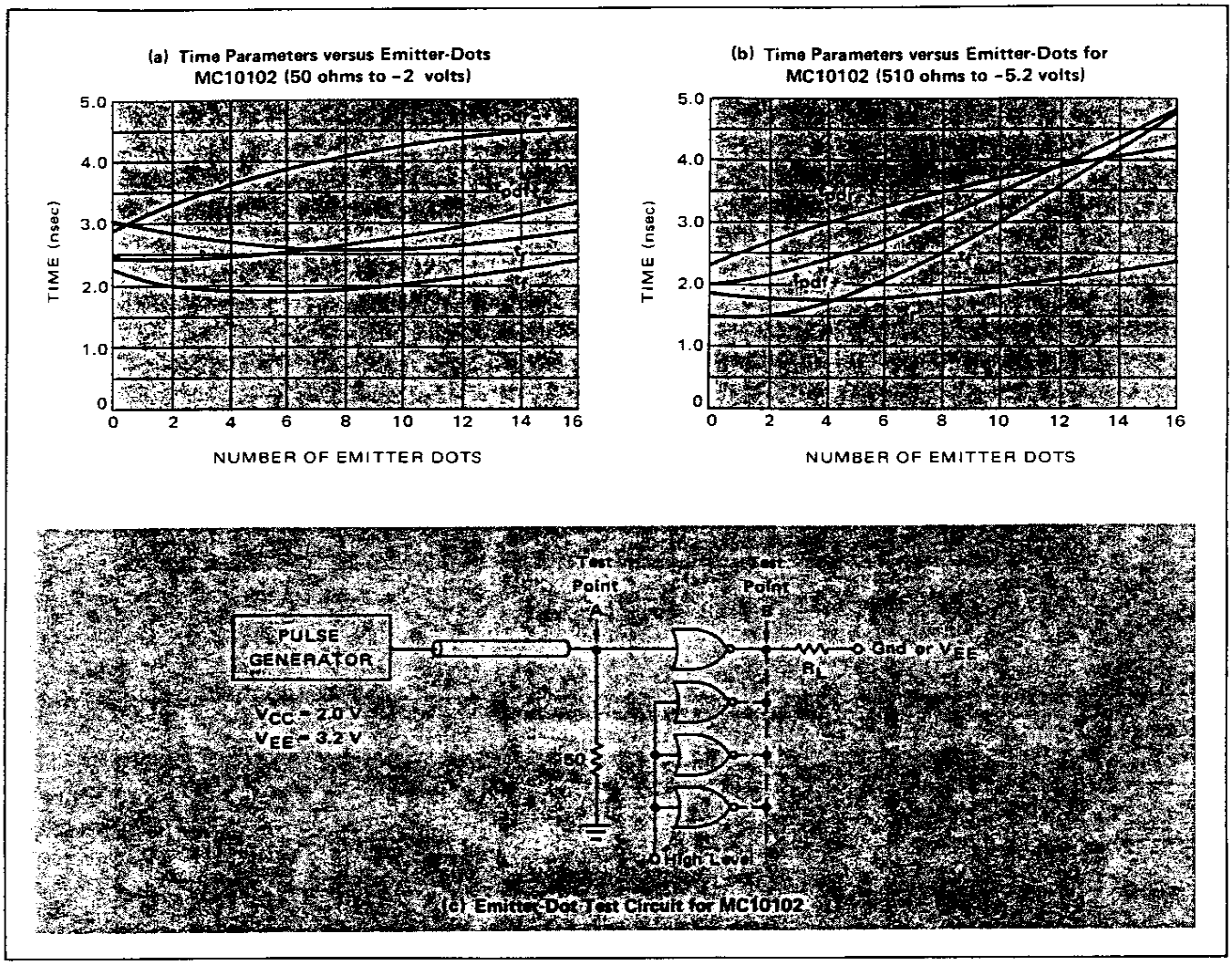


FIGURE 17

OTHER CONSIDERATIONS

Additional factors other than line length and transmission line terminations must be considered in system design. Some of these are discussed here:

(1) Fanout – The dc fanout capability of MECL 10,000 is very high since its high impedance inputs require little current (typically 160 μA). System speed requirements will ordinarily be the limiting factor for ac fanout. Capacitance increases with fanout and can cause rise and fall times to slow down.

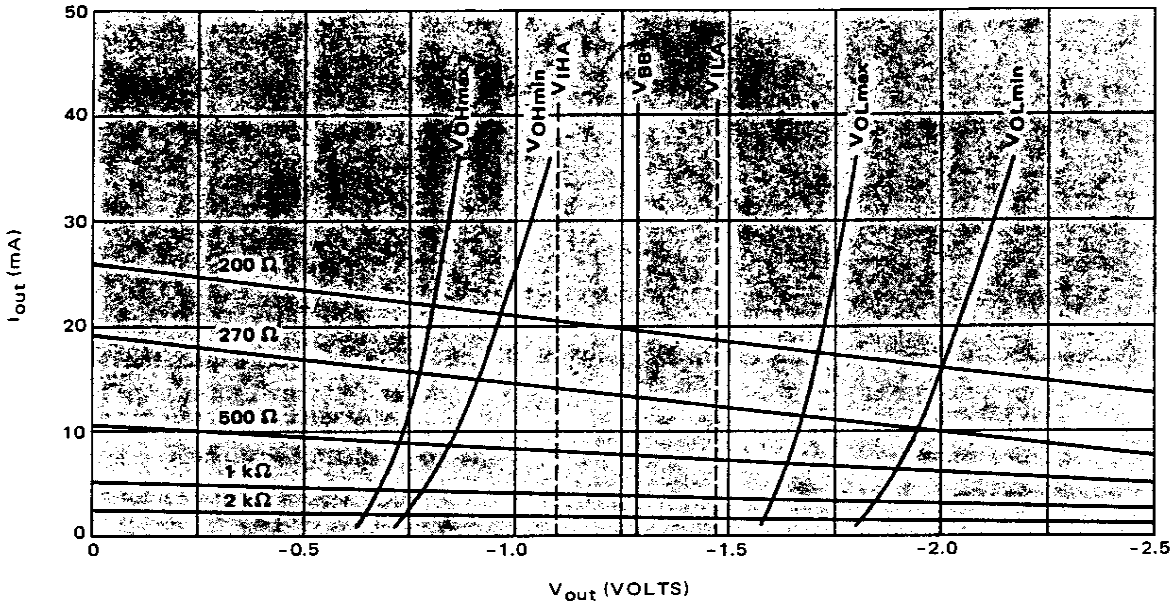
Figure 16 shows the rise and fall times of an MC 10,000 gate as a function of fanout, both for 50 Ω and 510 Ω terminations. As fanout increases, load capacitance (both device and interconnection capacitance) increases, resulting in longer rise and fall times.

Larger fanout will normally result in longer interconnecting lines with their longer line delays, so ringing can become excessive. Under these conditions, use of properly terminated lines will result in best performance. A low impedance (50 Ω) parallel terminated line has a shorter propagation delay than a series damped or series terminated line with equivalent fanout. However, multiple series terminated lines driven from a single gate output (figure 13), with lower fanout per line, will show shorter delay times than a single parallel terminated line with an equivalent total fanout. Multiple series terminated or damped lines also show greater flexibility in line routing than a single parallel terminated line. The choice between the two schemes will depend on the fanout number and physical layout of the system.

(2) Wired-OR – The outputs of several gates may be tied together to perform the Wired-OR or emitter dot function. One resistor is normally used to pulldown the outputs.

Figure 17 graphs typical rise and fall times and propagation delays versus the number of emitter dots for both 50 Ω to - 2 volts termination and 510 ohms to V_{EE} termination. Rise and fall times are not greatly affected by emitter dotting, with the exception of fall times with the 510 Ω loading. The reason for this is that the discharge path for load capacitance has a longer time constant with the 510 Ω resistor. The most significant effect of Wired-ORing is increased propagation delays. As for ac fanout, desired system speed is the basic limiting factor for the emitter dot.

(a) Load Lines for Termination to V_{EE} (-5.2 Vdc) at 25°C



(b) Load Lines for Termination to -2.0 Vdc at 25°C

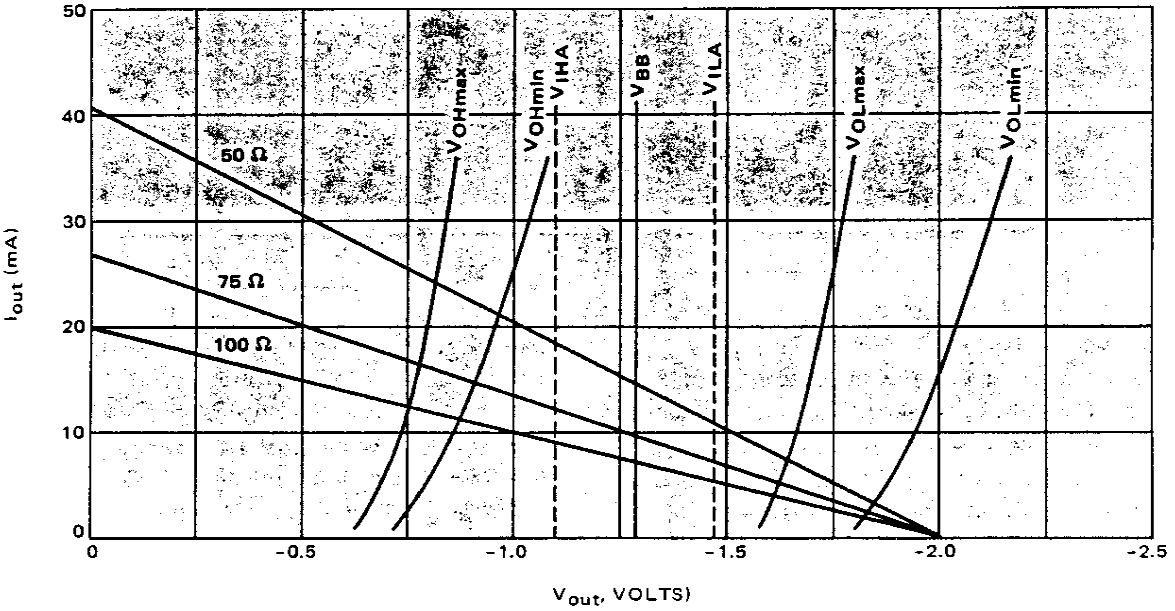


FIGURE 18 — MECL 10,000 Operating Characteristics

A second limiting factor in the case of the emitter dot is a dc level shift as the number of dots increase. The wired emitter-followers share current through the pulldown resistor and each additional wired output causes the current in every output to decrease. The logic levels shift upward as device current decreases. As the ∅ level shifts upward, noise margin may be lost. Figure 18 shows loading curves for a typical MECL 10,000 output and illustrates the shift in logic levels with output current. The ∅ level shift and resulting reduction of noise margin may be a greater limiting factor than ac considerations, depending on system requirements.

When using Wire-OR, interconnections should be held to minimum lengths for unterminated lines and parallel terminated lines. For larger numbers of distributed emitter-dots and longer interconnections, a doubly terminated line called a "data bus" may be used. Figure 19 shows an example of a 100-ohm data bus system. The dc loading

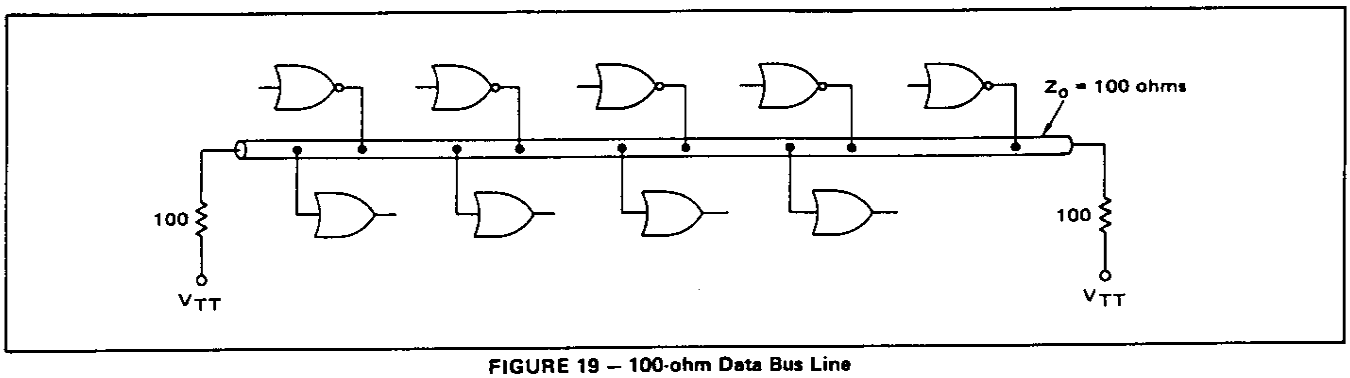


FIGURE 19 – 100-ohm Data Bus Line

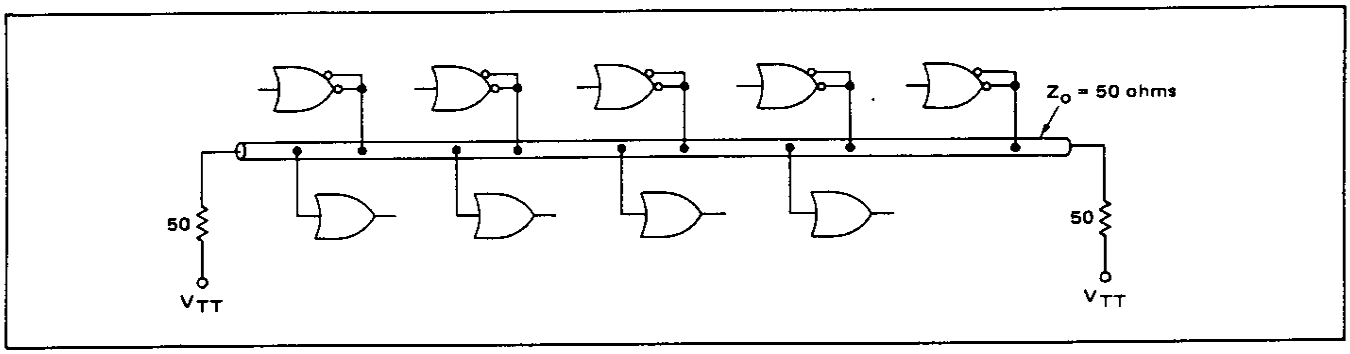


FIGURE 20 – 50-ohm Data Bus Line

on the line is 50 Ω as the 100 Ω terminating resistors are in parallel. However, for a transient waveform driven from any point on the line, the waveform travels to either end of the line and is properly terminated, so reflections are eliminated.

A lower impedance system is better for driving the high capacitive loading of a bus system. A 50 Ω system similar to the 100 Ω system is shown in figure 20. Notice that the drivers for the 50 Ω line must have two outputs in parallel to drive the 25 Ω dc load of the paralleled 50 Ω terminating resistors. The MC10110 or MC10111 multiple output gates may be used conveniently in this application.

When considering system timing, it must be noted that a long bus will add delay time to a data path. The worst case length on the bus, plus the effects of capacitive loading, should be considered for delay time. More will be said on bussing in the following section on board-to-board interconnections.

(3) Clock distribution – Clock lines usually handle the highest frequency in a system. For large fanout, a distribution tree should be used for maximum frequencies (figure 21). A good rule of thumb is to limit fanout to 4 per line and use as low an impedance line as possible. Parallel terminated lines or series damped lines (as in figure 13) may be used. A parallel terminated 50 Ω line with a fanout of 4 will drive a clock line to a frequency of about 110 to 120 MHz.

For higher clock frequencies, series terminated lines with fanout limited to 1 or 2 may be used; line lengths should be kept short and of equal length. A MECL III gate with faster edges will provide highest clock frequency capability.

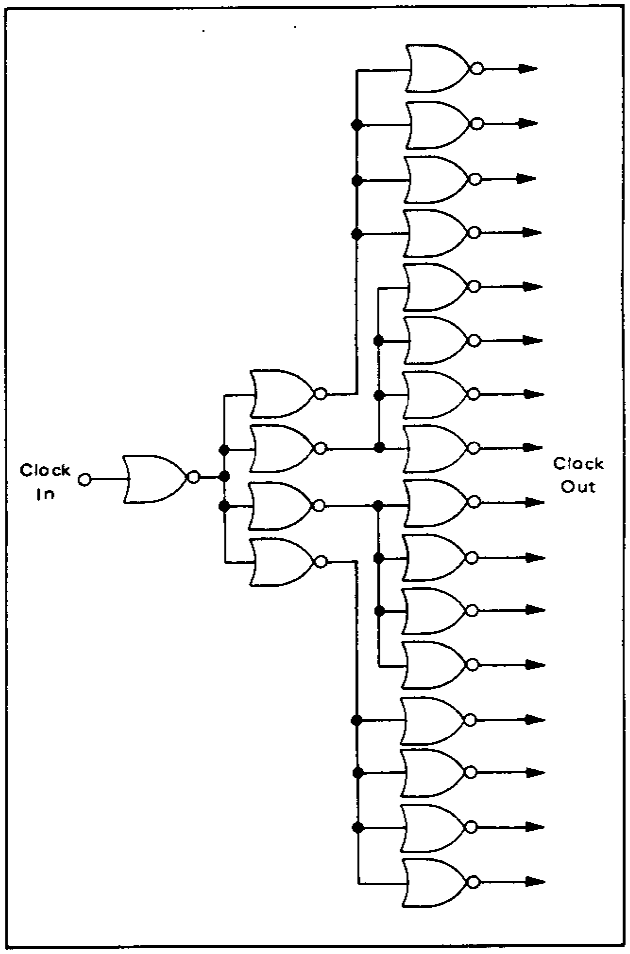


FIGURE 21 – Distribution Tree for a Clock Line with Large Fanout

BOARD-TO-BOARD INTERCONNECTS

Signal connections among logic cards, card panels, and cabinets are important for maintaining the best possible system performance. Ringing and crosstalk can appear when line lengths are long, or when characteristic impedance varies due to lack of a good ground. Ringing and crosstalk, along with power supply variations and system noise, can seriously affect system operation. To be within system noise margins (as previously mentioned, 125 mV worst case), maximum undershoot should be less than 100 to 110 mV.

The most practical means for limiting undershoot to less than 100 mV is either to limit line lengths, or else to use matched terminated transmission lines. Line lengths in board-to-board applications are necessarily long; therefore, some kind of terminated line should be used. The edge speeds of MECL 10,000 permit a choice among several methods for producing nominally constant impedance interconnections. Coaxial cable, mother-daughter boards, striplines, and wire over ground may be used.

When designing system interconnections, four parameters must be taken into consideration.

(a) propagation delay per unit length of line;
(b) attenuation of the line;
(c) crosstalk between lines;
(d) reflections due to mismatched impedance between the line and the line termination.

Propagation delay of the line is significant because unequal delays in parallel lines cause timing errors. Moreover, on long lines the total delay time will seriously affect system speed. Since the propagation delay of one foot of wire is approximately equal to the propagation delay of a MECL 10,000 Series gate, line lengths must be minimized when total system propagation time is of concern.

Attenuation is a characteristic of the line which increases for high frequency signals, due to higher impedance in the line. Attenuation first appears as a degradation in edge speed, then as a loss of signal amplitude for high frequencies on long lines. Within a backplane attenuation seldom is a problem, but is must be allowed for when interconnecting panels or cabinets.

Crosstalk is the coupling of a signal from one cable to a nearby cable. A coupled pulse in the direction of undershoot gives a reduction of noise immunity and should be avoided. A good ground system together with shielding is the best method for limiting crosstalk. Differential twisted pair line connections avoid problems of crosstalk by virtue of the common mode rejection of line receivers.

Reflections due to mismatched lines also cause loss of noise immunity. Successful termination of a line depends on how constant the impedance is maintained along the line. Coaxial cable is easier to terminate than open wire because of its constant impedance. In many cases twisted pair cable and ribbon cable may be purchased with specifications on the impedance of the line.

Conventional edge connectors may be utilized to get on and off PC boards with little mismatch in line impedances. Coaxial cable connectors which have excellent characteristics across the bandwidth exhibited by MECL 10,000 exist in a variety of types. The most popular types are BNC, and subminiature types such as SMA, SMB, or SMC.

SINGLE-ENDED LINES

Single ended lines are interconnections such as coaxial cable or other single path transmission line as opposed to a twisted pair of lines over which a differential signal is sent. To maintain some kind of constant impedance, a ground must be present. A ground plane may not be present for board-to-board interconnects, and so a ground must be run together with the signal line.

Types of single ended lines are discussed in the following paragraphs.

(1) Coaxial Cable – The well defined characteristic impedance of coaxial cable permits easy matching of the line, and the ground shield internal to the cable minimizes crosstalk between lines. In addition, low attenuation at high frequencies allows the cable to transmit the rise times associated with MECL signals.

Bandwidth and attenuation are the limiting factors in using coaxial cable. The bandwidth required for MECL 10,000 is:

$$f \approx \frac{0.37}{\text{rise time}};$$

$$\approx \frac{0.37}{3 \times 10^{-9}};$$

$$\approx 125 \text{ MHz bandwidth for } 50\ \Omega \text{ load}.$$

Attenuation is due mainly to skin effect in the cable. The loss in signal amplitude due to attenuation will limit the maximum usable length of line. For a maximum signal reduction of 100 mV from the logic 1 and Ø levels (800 mV p/p to 600 mV p/p) the permissible attenuation is 2.5 dB:

$$\text{dB} = 20 \log \left(\frac{V_{in}}{V_{out}} \right) = 20 \log \left(\frac{0.8}{0.6} \right) = 2.5 \text{ dB}.$$

The maximum line length which will produce no more than 2.5 dB attenuation will be:

$$\text{max length} = 100 \text{ ft.} \left(\frac{2.5 \text{ dB}}{\text{Atten.}} \right),$$

where Atten. is the cable attenuation in dB/100 ft. at the operating frequency.

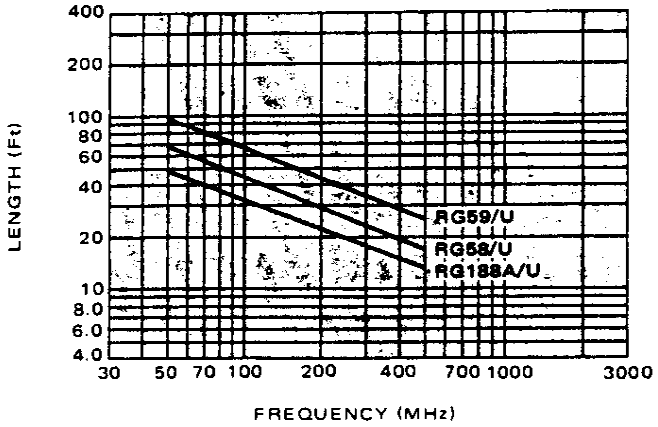


FIGURE 22 – Coaxial Cable Length versus Operating Frequency: Constant 2.5 dB Loss Curves

Figure 22 shows curves for maximum line lengths versus operating frequencies for a 2.5 dB loss. Data for three cable types are plotted. A high bandwidth line is necessary to preserve fast signal edges regardless of the bit rate of a system.

In figure 22 it is assumed that the coaxial line is properly terminated with a resistive load equal to the characteristic impedance of the line. Standard carbon 1/8 or 1/4 watt resistors work well for all line terminations. However when using precision wire-wound or film resistors, care should be taken to determine the high frequency properties of these devices since they may become highly inductive at high frequencies, and thus be unusable.

Coaxial cable should be used for sending single-ended signals over long lines. The constant impedance and low attenuation of such cable allows transmission of signals with minimum distortion.

(2) Parallel Wire Cable – Multiple conductor cable as purchased, or as constructed by lacing interconnecting wires together, is not normally used with MECL or other high speed logic types because of crosstalk. Such crosstalk is due to the capacitive and inductive coupling of signals between parallel lines. Such cable is also susceptible to external signals coupling to the entire cable. Multiple conductor, single-ended cable is not recommended for use with MECL unless individual shields on each wire are employed.

(3) Ribbon Cable – Systems requiring large numbers of board-to-board interconnections may take advantage of multiconductor ribbon cable (figure 23). Ribbon cable is easily wired to connectors because of its in-line wire arrangement. Its flexibility permits easy routing and board removal. The side-by-side arrangement of signal lines produces a defined characteristic impedance because of the presence of alternate ground wires.

Commercial ribbon cable is available with a wide variety of characteristic impedances, and the manufacturer should be consulted for information on such cable parameters as attenuation, characteristic impedance, and number of conductors.

With ribbon as with coaxial cable, the maximum permissible attenuation is 2.5 dB. Attenuation per foot is generally higher for ribbon cable than for coaxial cable. Consequently maximum line lengths for ribbon are limited by operating frequency.

(4) Point-to-point Wiring – A system made up of several logic cards may be assembled using edge connectors to form a card file. Point-to-point wiring via the board connectors may then be used for system interconnections.

A ground plane is often formed by a large printed circuit board to which the card connectors are mounted. The ground plane may be connected to the frame holding the card connectors. Metal is left on one side of the PC board to form the backplane system ground, or metal may be left on both sides of the board to supply power to the system logic cards. These card file systems are commercially available from a number of manufacturers.

When a solid ground plane is not practical, a ground screen should be constructed on the backplane. A ground screen may be made by connecting bus wires (wire size compatible with connector) to the edge connectors in a grid pattern, prior to signal wiring (figure 24). About every sixth pin on the card edge connectors is used as a ground, providing connection points for the ground grid. This interconnection of ground points forms a grid network of approximately 1 inch squares over which the signal lines are wired. A characteristic impedance of about 140 ohms can be expected for a wire over ground screen, depending upon the exact routing and distance from the screen.

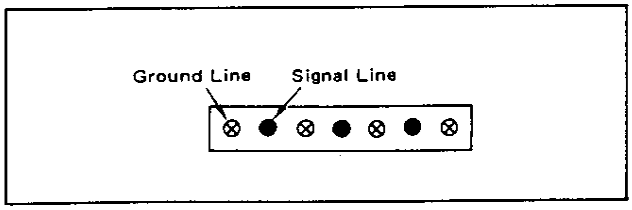


FIGURE 23 – Cross-Section of a Typical Multiconductor Ribbon Cable

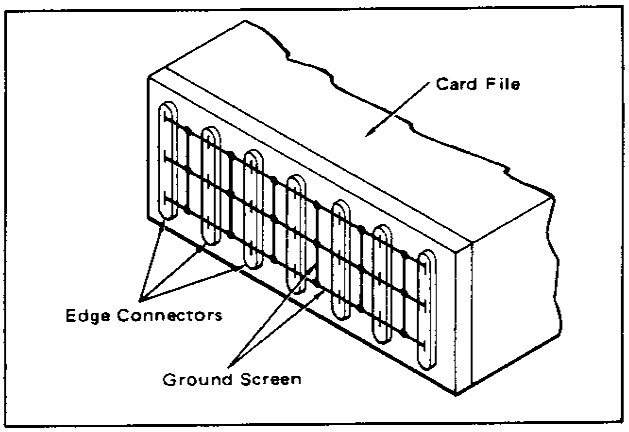


FIGURE 24 – Ground Screen Construction

To provide maximum signal purity, a motherboard composed of multilayer or two layer board may be used to mount the card connectors. Striplines or microstrip lines are designed on the circuit board, along with ground and voltage planes. Connectors are available to interface between cards and the motherboard with little line discontinuity. The motherboard technique is normally used when the system design is sufficienty determined that changes in the backplane wiring will be few.

When using point-to-point wiring with a ground plane or screen, soldered connections or wire wrap techniques may be used. In general one good terminating technique is to parallel terminate with approximately 100 to 120 Ω to - 2 volts. The resistor will be near the characteristic impedance of the line and so minimize ringing. Series damping or termination may be used, following the rules presented previously. An unterminated line with a fanout of 4 may be up to 15 inches long when a ferrite bead is placed at the sending end of the line.

For high speed lines, such those for clock distribution, coaxial cable and twisted pair lines should be used between cards. Maximum signal integrity of clock signals should be maintained for best system performance.

DIFFERENTIAL TWISTED PAIR LINES

Twisted pair lines, differentially driven into a line receiver (figure 25), provide maximum noise immunity. Any noise coupled into a twisted pair line appears equally on both wires (common mode). Because the receiver senses only the differential voltage between the lines, crosstalk noise has no detrimental effect on the signal up to the common mode rejection limit of the receiver. The line receivers MC10115 and MC10116 have a common mode rejection limit of 1 volt to a positive-going common mode signal, and 2.5 volts to a negative-going common mode signal.

The partial schematic of an MC10115 line receiver is shown in figure 26. Each receiver is a differential amplifier whose output level is dependent on the input voltage differential. If the inputs, IN1 and IN2, are at the same voltage, the output will be at the mid point of a MECL 10,000 logic swing; that is, at - 1.3 V = V_{BB} (note that a pulldown resistor on the output is necessary). The output voltage will go more positive as input IN2 goes more positive than input IN1; that is when the differential voltage from IN2 to IN1 is plus to minus. The inverse is also true. The output goes more negative than V_{BB} when the polarity of the differential voltage from IN2 to IN1 is minus to plus (cf figure 26b).

The output voltage change of the receiver is equal to the input voltage differential times the voltage gain of the amplifier. To have a full MECL swing, the output must swing ±400 mV about V_{BB}. Therefore, with the voltage gain of the differential amplifier typically 6 V/V, the minimum input differential must be approximately: 0.4 V/6 = 67 mV (either plus to minus or minus to plus.)

For system design, other factors affect the minimum differential input voltage. Decreasing voltage gain with increasing frequency (figure 27), offset voltage of the am-

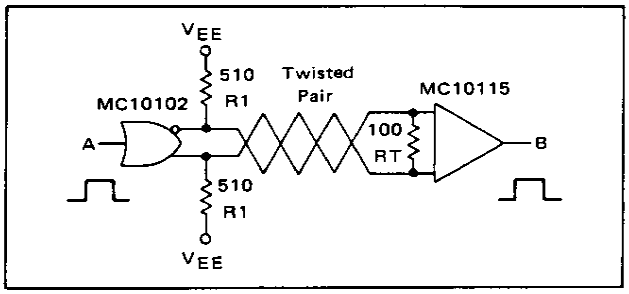


FIGURE 25 – Twisted Pair Line Driver and Receiver

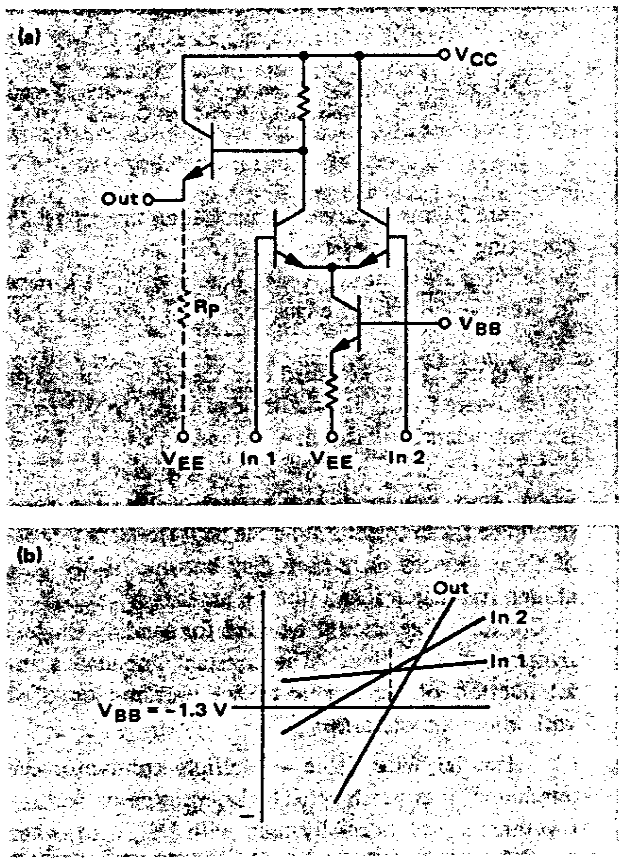


FIGURE 26 – 1/4 MC10115 Circuit Schematic

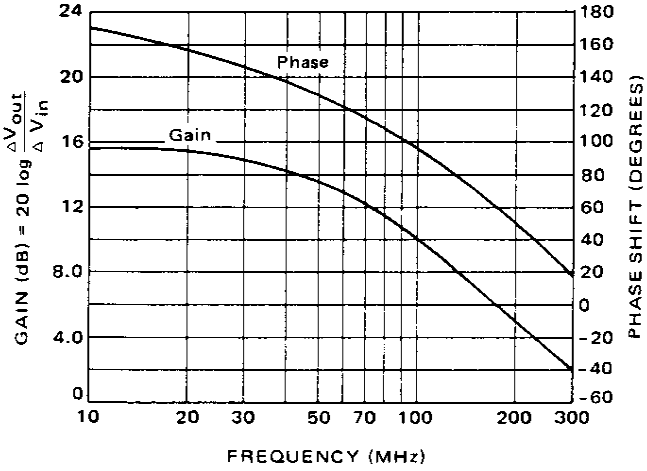


FIGURE 27 – Typical Gain and Phase Characteristics for MC10115 Line Receiver

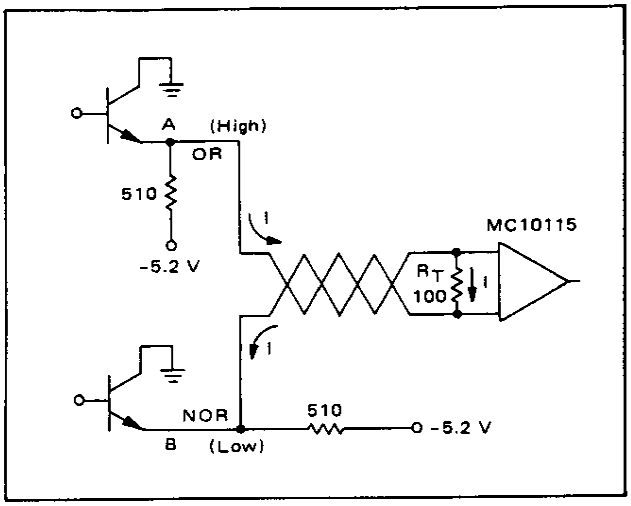


FIGURE 28 – DC Equivalent Circuit of Line Driver and Receiver

plifier, noise, and other system parameters demand a larger input differential voltage. A minimum differential input voltage of 150 mV at maximum frequency is recommended for system design.

Except at slow bit rates, attenuation will be the limiting factor for twisted-pair line length. The dc equivalent of the twisted pair line of figure 25 is shown in figure 28. Ignoring the dc resistance in the line, the voltage across the terminating resistor is:

$$V_{RT} = \frac{(5.2\ V - 0.9\ V)\ (100\ \Omega)}{510\ \Omega + 100\ \Omega},$$

$$= 0.705\ V.$$

Note that if V_R becomes as large as 800 mV and begins to go below a logic ∅ level of -1.7 V, the NOR output will clamp the voltage at node B.

The voltage across the terminating resistor decreases as frequency increases due to attenuation in the line. Figure 29 tabulates the maximum differential voltage appearing across the termination resistor, versus frequency for a 50 ft. line as shown in figure 25. Maximum line length will be determined by operating frequency.

A different termination method for a twisted pair line is shown in figure 30. The pulldown resistors terminate the line. As a result, full output levels are presented to the receiver. Attenuation data for this line is shown in figure 31. Waveforms for input and output signals for both termination methods are pictured in figure 32.

FIGURE 29 – Attenuation of 50 Ft. of Twisted Pair Line with MC10102 and MC10115

FREQUENCY (MHz)	MAX DIFFERENTIAL VOLTAGE AT R_T (mV)
25	520
50	420
75	325
100	235
125	165

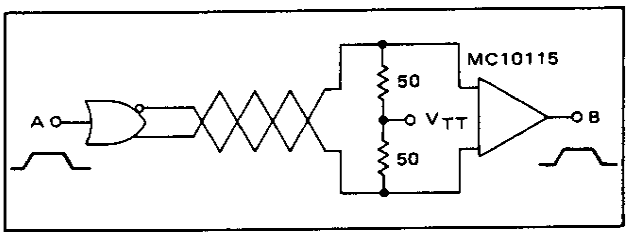
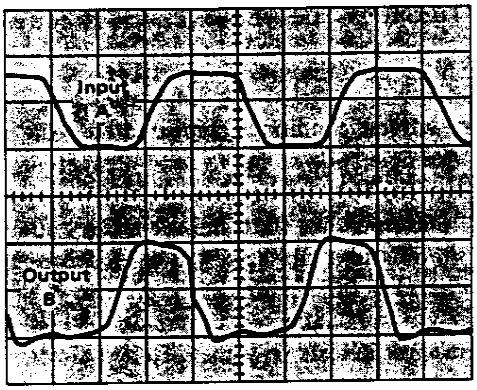


FIGURE 30 – Twisted Pair Line with Pulldown Resistors As Equivalent Termination Resistor

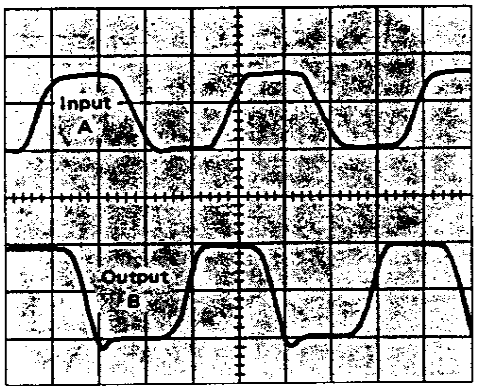
FIGURE 31 – Attenuation of 50 Ft. of Twsited Pair Line Driven By an MC10102 with 50-ohm Pulldowns

FREQUENCY (MHz)	MAX DIFFERENTIAL VOLTAGE AT R_T (mV)
25	600
50	475
75	350
100	240
125	175



Horizontal Scale = 5 ns/div.
Vertical Scale = 500 mV/div.

(a) 510-ohm Pulldowns (cf Figure 25)



Horizontal Scale = 5 ns/div.
Vertical Scale = 500 mV/div.

(b) 50-ohm Pulldowns (cf Figure 30)

FIGURE 32 – Waveforms for 50 Feet of Twisted Pair Lines at 50 MHz

A variety of cable types can be used with differential twisted pair lines:

(1) Bundled twisted pair cable – Cable with several bundled twisted pairs is commercially available. When running MECL signals in parallel with higher voltage analog or logic signals, shielded twisted pair lines should be used. Shielded twisted pair lines have foil shield on each twisted pair that may be tied to the system ground.

(2) Ribbon cable – Ribbon composed of several twisted pairs is one type of ribbon cable available. Conventional side-by-side cable (figure 23) may also be used with differentially driven signal lines (figure 33). With every other wire grounded, the signal lines will have a constant characteristic impedance.

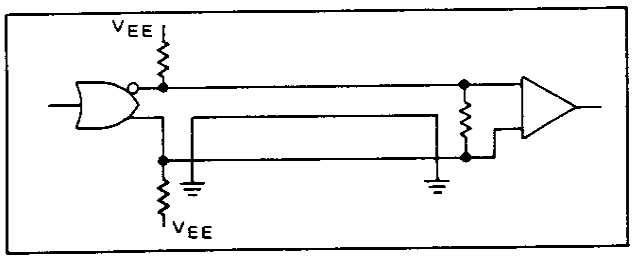


FIGURE 33 – Using Ribbon Cable as Twisted Pair Line

Differential twisted pair lines offer several advantages under adverse conditions compared to single ended lines. For example, power supply and temperature variations might occur between panels or between cabinets of a system. Corresponding shifts in logic levels within the system will subtract from noise margins when driving single ended lines between these points in the system. However, differential lines are unaffected by variation in logic levels, since the receiver detects only the differential voltage between the driver outputs, rather than detecting absolute logic levels.

With single ended lines, noise generated on the signal line by crosstalk and inductive coupling directly reduces noise immunity. Noise is coupled equally onto both wires of a twisted pair line, so the differential voltage is unaffected. As a result, the receiver will not detect noise as long as it is within the common mode range of the receivers.

DATA BUSSING AND PARTY LINE TECHNIQUES

Data bussing usually requires large fanout, long lines, and several driving points. A MECL 10,000 bus or "party line" may be made by emitter-dotting gates together, with the restriction that only one driver is allowed to go high at one time.

Figures 19 and 20 illustrate data bus lines which may be extended for board-to-board use. The characteristic impedance of board-to-board interconnections will generally be from 100 to 150 ohms so the termination resistors must be adjusted accordingly.

Another scheme for bussing is the twisted-pair party line of figure 34. The driving gates are emitter-dotted. It is required that all their outputs be held low when not sending data. (V_{BB} is available from the MC10115 and MC10116, and may be buffered as shown in figure 35 to handle the necessary termination current).

In both bussing schemes the driving lines are operating single ended. However, the twisted pair bus retains the advantage of the common mode rejection of the line receivers. As previously mentioned, the limiting factors for emitter-dotting also apply to the party lines shown.

WIREWRAPPING TECHNIQUES

The versatility of MECL 10,000 allows the use of this logic family with wirewrapping techniques. Wirewrapping is popular for breadboarding large system prototypes and for interconnecting system logic boards. The ability to change system interconnections easily has made wirewrap extremely usable for breadboarding new system designs.

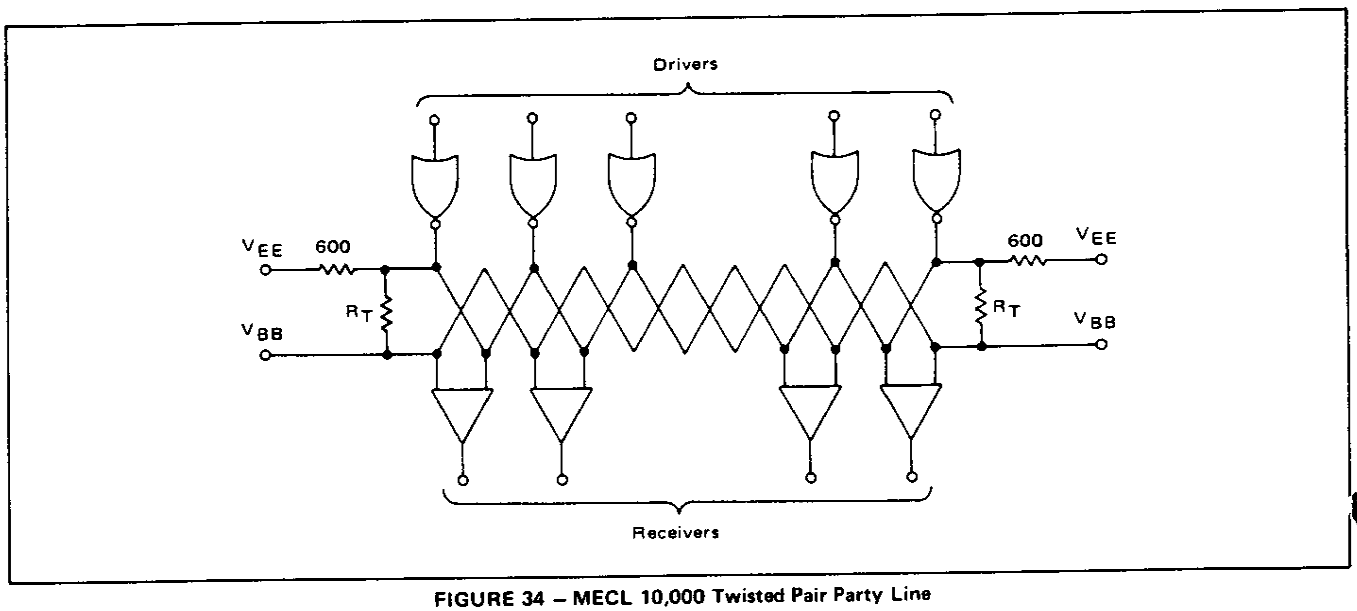


FIGURE 34 – MECL 10,000 Twisted Pair Party Line

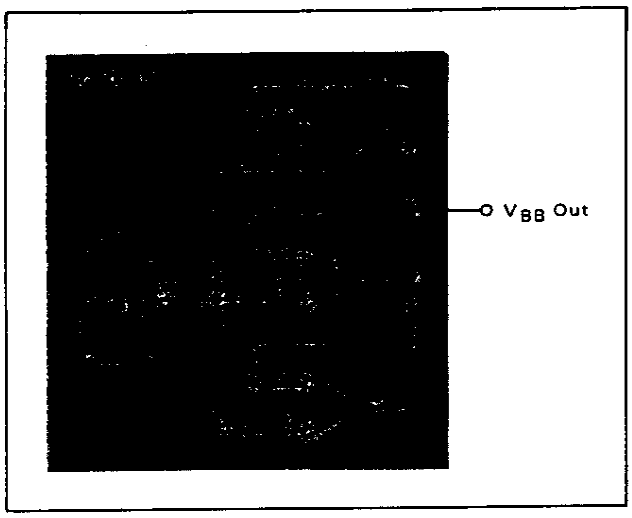


FIGURE 35 – V_{BB} Generator

MECL 10,000 systems may be wirewrapped using high density dual-in-line packaging boards. In addition, wirewrapping may be used for board-to-board interconnections when the logic boards are mounted in a card file in edge connectors. Some general guidelines for use of MECL 10,000 with wirewrap follow:

SYSTEM PROTOTYPING – Several types of wirewrap boards for dual-in-line packages are commercially available. For MECL 10,000 systems, a board should be used that has voltage planes on both sides of the board and low-profile device mounting. Device mounting via pins set in the boards is the most satisfactory method.

The V_{CC} pins of the device mounting should be soldered to the V_{CC} voltage plane (the voltage plane on the device side of the board is the best choice.) When the V_{CC} pins are wirewrapped to the V_{CC} voltage source, a ferrite bead on a wire between the V_{CC1} and the V_{CC2} pins of the same package will help avoid high frequency noise and will prevent possible oscillation. Long leads from the ground plane to the V_{CC} pins help induce oscillation and noise, due to their added inductance. V_{EE} pins may be wirewrapped to the V_{EE} voltage plane with no detrimental effects. Bypassing on the board should be provided in a manner similar to that mentioned for a two-sided PC board with a ground plane.

Wiring rules for wirewrapped interconnections are similar to those for a wire over ground. If a voltage plane is present, the characteristic impedance of a wirewrap interconnection is 100 to 150 ohms. Parallel termination, series damping, and unterminated lines may all be used, and the unterminated line lengths of figure 8 (backplane) also apply to wirewrap. However, in prototyping and breadboarding these lengths may be extended if low bit rates are present or if greater ringing is acceptable. When doing prototype breadboarding, the designer is often concerned with the "workability" of the design, as opposed to operation with best noise margins and signal waveforms.

With wirewrap, the pulldown resistors may be provided by commercial resistor networks in a dual-in-line package or via adaptor plugs. Many manufacturers are marketing resistor networks in a variety of values suitable for MECL 10,000 terminations. Resistor networks with good high frequency characteristics should be used. Networks composed of discrete resistor chips mounted in a package, or thick-film cermet resistors with a minimum of interconnect metal within the package, provide the best high frequency characteristics. Wirewrap equipment manufacturers have made dual-in-line adaptor plugs available, to allow discrete components to be mounted for use on the wirewrap board (cf figure 36).

An example of a wirewrap system is shown in figure 37. A 4 x 4 bit multiplier (figure 38) was constructed using MECL 10,000. The delay line oscillator has a frequency of 30 MHz and the total multiplication cycle time is about 175 ns. The multiplier uses an add-shift algorithm.

The clock distribution for this system used a parallel terminated wirewrap line (Thevenin equivalent). Twisted pair lines may also be used for clock distribution, and are helpful for higher clock rates. With wirewrap, maximum clock rates are in the neighborhood of 100 MHz, when using twisted pairs.

To get signals on and off the board, commercially available multiconductor ribbon cable was utilized. Commercial cable adaptors, which plug into the wirewrap board, are available. Alternate lines are grounded to minimize crosstalk and generate a characteristic impedance for the signal lines.

BACKPLANE WIREWRAP – A card file composed of several logic cards may use wirewrap for board-to-board interconnection. The same rules as discussed in the section, SINGLE-ENDED LINES #4 for board-to-board interconnects, apply to wirewrap. A ground plane or ground screen is recommended; termination techniques and line lengths should follow the rules previously presented.

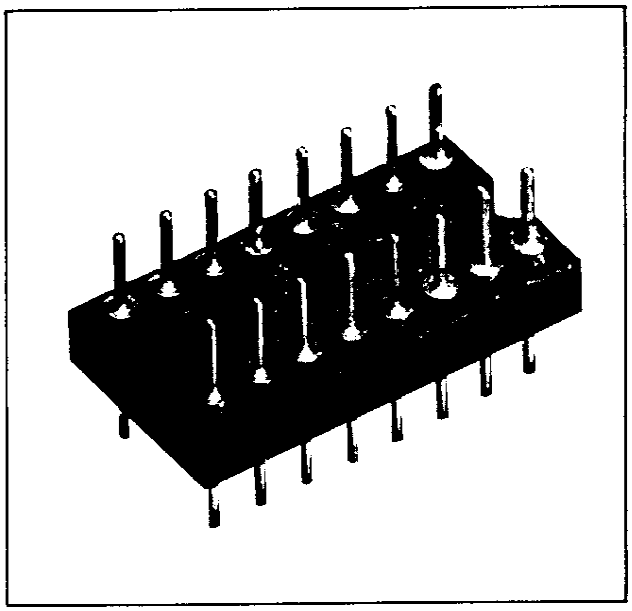


FIGURE 36 – Dual-in-line Adaptor Plug for Mounting Discrete Components.

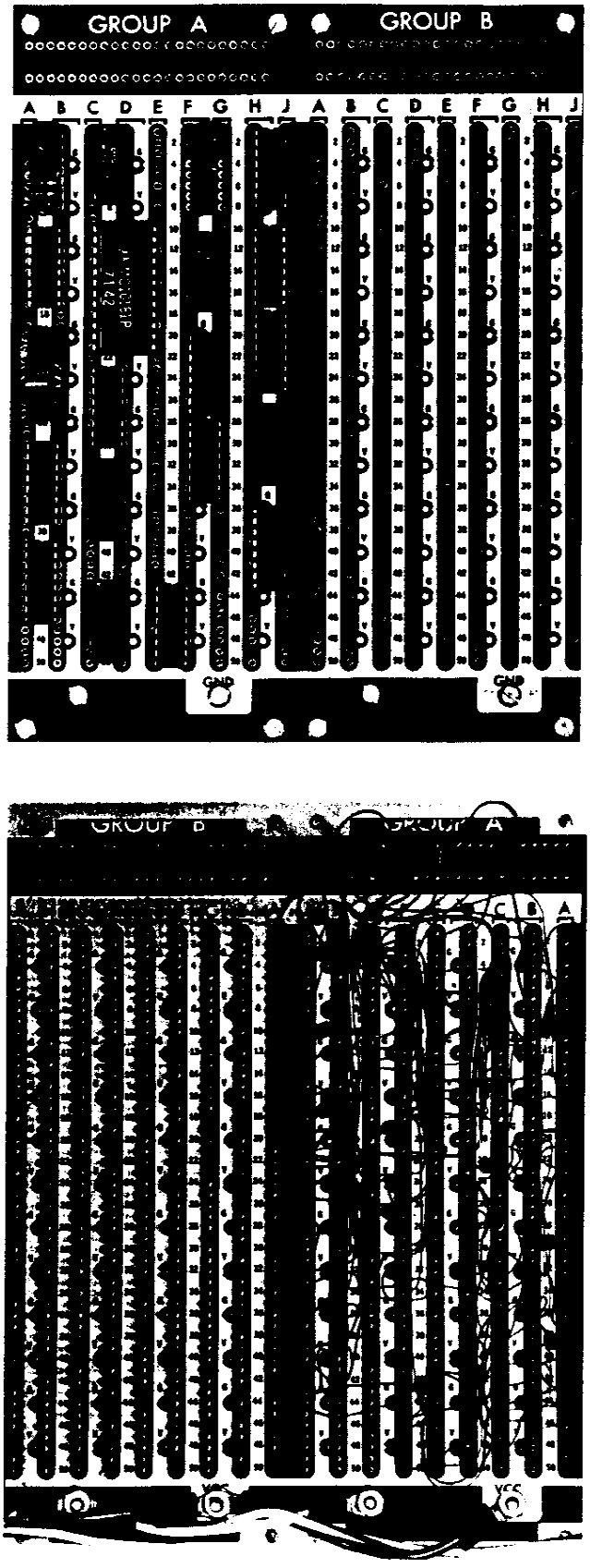


FIGURE 37 – 4 x 4 Bit Multiplier Prototype Showing Wirewrap with MECL 10,000 Logic

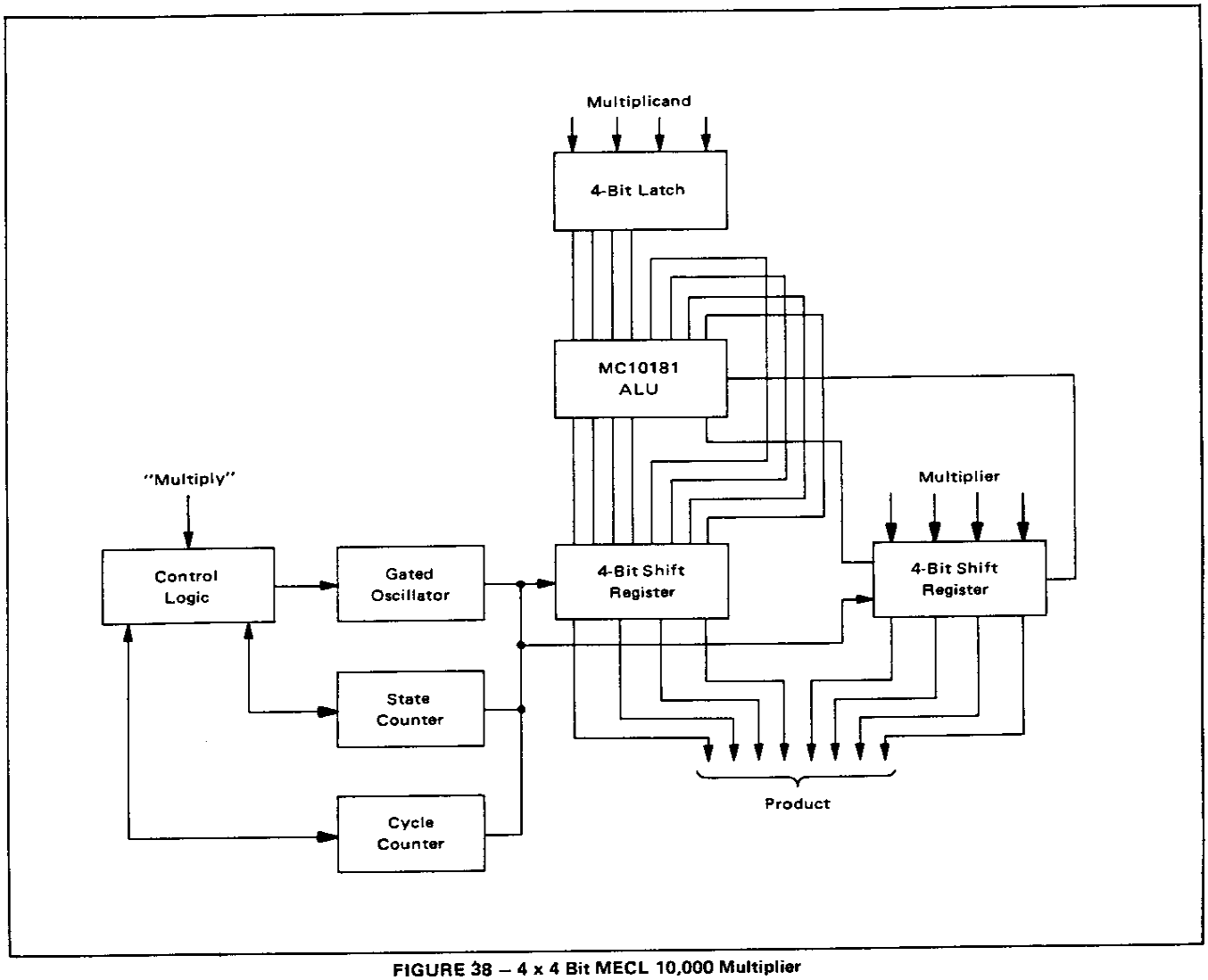


FIGURE 38 – 4 x 4 Bit MECL 10,000 Multiplier

CONCLUSION

This application note has been written to present information which a designer may use to construct a reliable, high performance MECL 10,000 system. Much of the transmission line theory that explains the effects of high speed signals on interconnects has not been presented here because the application note is directed toward usage rules rather than a detailed theoretical discussion. For more detailed information on transmission line theory and other MECL system considerations such as power supply variations and thermal considerations, the designer is directed to the MECL System Design Handbook, published by Motorola Semiconductor Products Inc.

References:

1. "MECL System Design Handbook", Motorola Inc., 1972.
2. "MECL Integrated Circuits", Semiconductor Data Library, Volume 4, Motorola Inc., November 1974.