AN1686

Intelligent LDO Regulator with External Bypass Control

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Introduction

Glitch–Free Supply Transition from the *5V primary supply* to the *auxiliary 3.3V supply* can be easily implemented for PCI/NIC and other motherboard slot cards via the MC33565 Intelligent LDO regulator. This linear regulator contains detection and logic circuitry to determine which supply is active and take appropriate action to maintain a steady 3.3V output, even as the supply planes change from "working" state to "system sleep" state.

The Advanced Configuration and Power Interface (ACPI) design specification for managing power consumption within PC's provides for various power consumption states from G0 (CPU actively executing code) to four different levels (S1–S4) within the G1 sleep state. The system can be roused from the various levels of the sleep state without requiring a reboot of the Operating System because both the system hardware and software save large elements of the system context. To be ACPI compliant, Network Cards and modems plugged into the motherboard should be designed to function both from the 5V main supply plane (available in G0 state) and the auxiliary 3.3V supply (available in G1 state).

ACPI compliant systems can provide important benefits to the end–user, including:

- PC's appear "off" and quiet when not actively in use, but resume full operation when required.
- Network communication can be received by an ACPI compliant card even though the PC is in sleep state.
- Energy efficient operation without inconviencing the end–user.[1]

The MC33565 Intelligent LDO has been developed to provide the hardware designer a convenient and easy implementation of the dual supply compliance.

An External Bypass MOSFET is controlled by the MC33565 to connect the 3.3V auxiliary supply directly to the output, thus bypassing the internal linear low dropout regulator whenever the 5V main supply is not present. When the 5V main supply power *is* present, the internal LDO circuitry regulates this down to 3.3V and provides it to the output at currents up to 200 mA (the bypass MOSFET's gate is biased "off" at this time). The internal 5V detection and logic circuitry has sufficient hysteresis to prevent inappropriate toggling between the two supplies if a full load is suddenly applied. (Note: this requires that the source impedance of the 5V supply, including wiring and printed circuit trace DCR, be less than 0.25 ohm for 200 mA loads.)

Power Dissipation of the MC33565, when mounted appropriately on conventional FR4 epoxy pcb, is sufficient to support regulation of the 5V input down to 3.3V at an output current of 200 mA. The power dissipated by the external bypass P–channel MOSFET is a function of its $R_{ds(on)}$. The dissipation is trivial with the recommended MGSF1P02ELT1 SOT–23 packaged MOSFET which has a typical $R_{ds(on)}$ of 400 milliohms at V_{gs} = 2.5V. P–channel MOSFETs with similar or lower $R_{ds(on)}$ and gate sensitivity parameters should work as well.

Functional Description

The MC33565 device contains 121 active transistors comprising the following functions:

- Low dropout regulator
- Internal voltage reference and 5V detection circuitry
- Voltage compensation and hysteresis control
- Voltage comparator and MOSFET gate driver

The Figure 1 depicts the functional relationships in block diagram form. Note that the 3.3 V_{in} is an input to both the MC33565 and to the drain of the external P–channel MOSFET. The 3.3 V_{out} is derived either internally via linear regulation from the +5 V_{in} input, or else is simply passed directly from the +3.3 V_{in} input to the +3.3 V_{out} via statically gating *on* the external MOSFET which then acts as a bypass switch around the LDO.

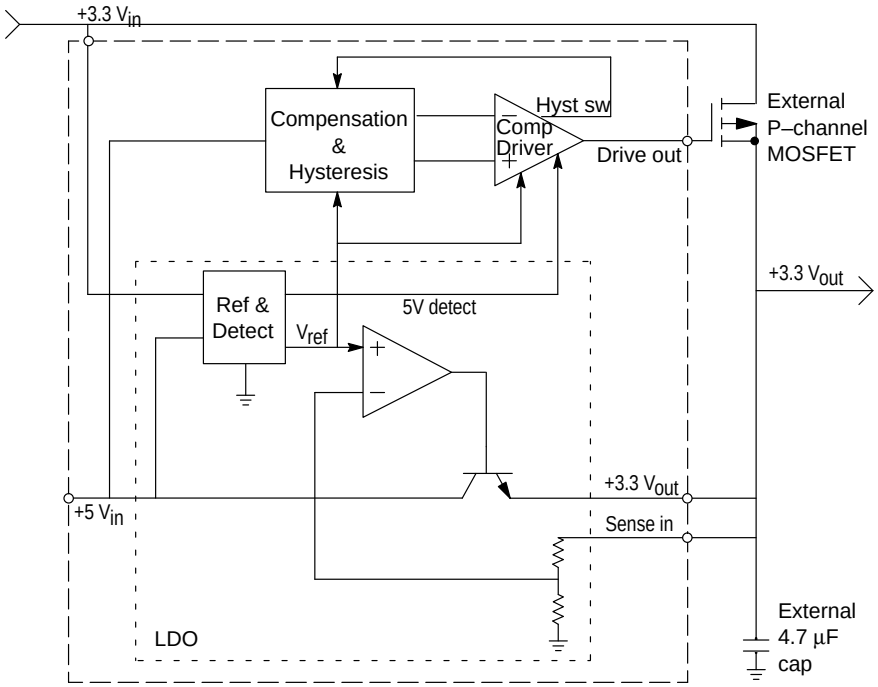


Figure 1.

The voltage reference and 5V detection circuitry provides the reference for LDO regulation and also provides a 5V detect signal which acts as a disable to the MOSFET driver circuitry. The +3.3 V_{out}, therefore, is provided via regulation down from the +5 V_{in} whenever +5 V_{in} is present. When +5 V_{in} is absent, the MOSFET driver is enabled and the external MOSFET can pass the +3.3 V supply directly to the output. By using an appropriately low $R_{ds(on)}$ rated P–channel MOSFET, trivial voltage will be dropped across the drain–source impedance of the transistor.

Compensation and hysteresis circuitry is provided to prevent the overall circuit from oscillating (bouncing or toggling) between enabling the MOSFET and enabling the LDO when making the transition when significant load present. The hysteresis provided is sufficient to permit glitch–free transitions with +5 V_{in} source impedances as high as 250 milliohms (at 200 mA loading). As long as the source impedance, including cabling and pcb trace DCR, is less than 250 milliohms, we are assured that $I_o \times R_{source} < V_{hyst}$, thus avoiding MOSFET drive bounce during the 5V detect threshold transitions.

The diagram below illustrates a minimum configuration for utilizing the MC33565. The only external components required are a P–channel MOSFET such as the SOT–23 packaged MGSF1P02ELT and a capacitor of at least 4.7 µF with maximum ESR of 500 milliohms. (Note 22 µF is recommended to ensure stable operation over the temperature range, as the temperature coefficients of many capacitor types are both large and poorly controlled.)

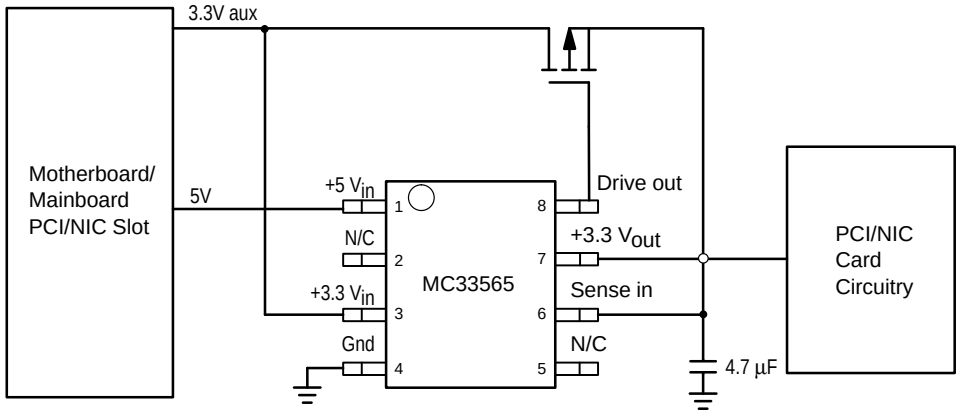


Figure 2.

Reference Design Example

A more conservative design approach would include additional filter capacitors on both the inputs and output. For example, to allow for varying distances from the supply planes' bulk filter capacitance, the designer could incorporate 4.7 μF tantalum or ceramic and 0.1 μF ceramic capacitors close to the +5 V_{in} input pin. This combination would provide robustness to input voltage droop (during rapid changes in load) as well as provide high frequency decoupling. High frequency decoupling capacitors would also be recommended close to the +3.3 V_{in} and +3.3 V_{out} pins.

The pcb copper and component layout artwork and schematic below (Figures 3, 4, and 5) incorporate the above recommendations. Also included is provision for either jumpering the sense input directly to the +3.3 V_{out}, or connecting it to the load via an external non–current–carrying trace.

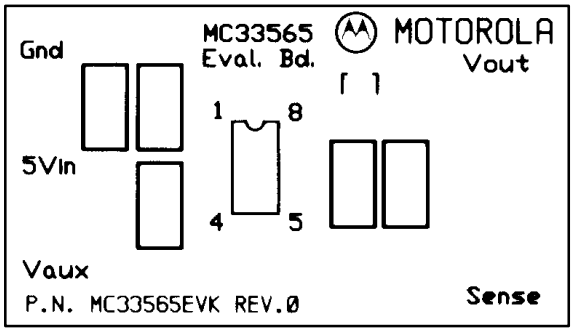


Figure 3. PCB Component Layout

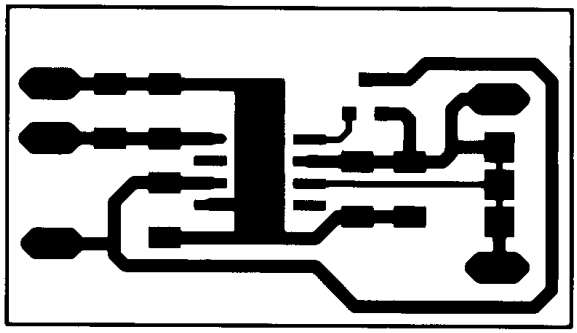


Figure 4. PCB Copper Layout

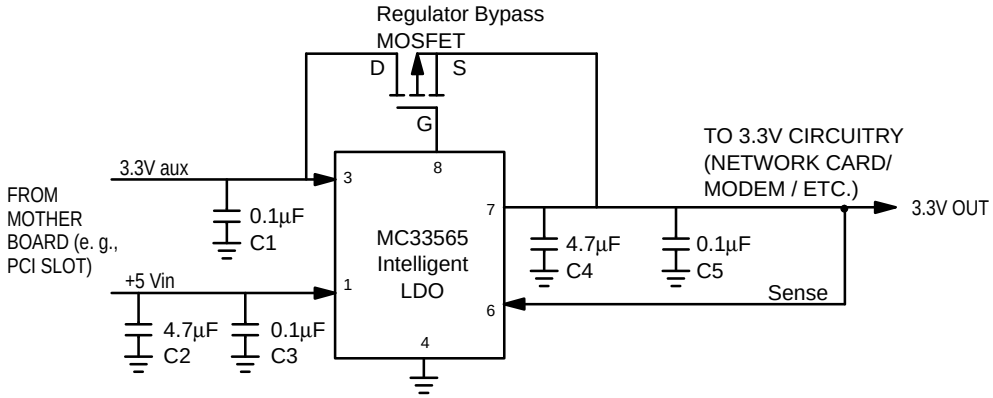


Figure 5. PCB Schematic

By using the artwork in Figures 3 and 4 to create a small surface mount single sided evaluation board (components and copper on the same side), the reference design can be easily breadboarded onto existing prototype pci (or other form factor) cards.

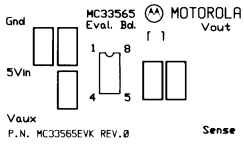
Summary

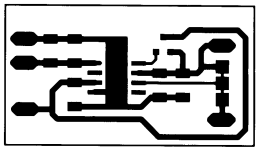
The MC33565 has been designed to provide easy implementation of ACPI power management for PCI and network interface cards (NICs), where operation from a 3.3 V auxiliary supply is required when the 5V supply has been shut down due to the main processor entering a reduced power state (e.g., sleep state).

The MC33565 permits glitch–free transitions from "sleep" to "active" system modes by providing the internal logic circuitry to detect whether the system is being powered from the motherboard main 5V power supply or the 3.3V aux supply. The MC33565 provides a regulated output voltage of 3.3V via either an internal low dropout 5.0V–to–3.3V voltage regulator or an external P–channel MOSFET, depending on the operating status of the system. During normal operating mode (5V main supply available) the 3.3V output is provided from the internal low dropout regulator at an output current of 200mA. When the motherboard enters sleep mode, the MC33565 operates from the 3.3V aux supply and routes the aux current to the output via the external P–channel MOSFET bypass transistor. As a result, the output voltage provided to the peripheral card remains constant at 3.3V even during transitions to and from sleep mode.

References

1. Mobile Power Guidelines 2000, pp51, Rev 1.0, Dec. 11, 1998, Intel Corporation.
2. PCI Bus Power Management: Hardware Considerations for PCI 3.3 Vaux Implementations, Wireless Symposium / Portable by Design, San Jose CA, 1999.
3. “Basic Semiconductor Thermal Measurement”, Gary E. Dashney, Thermal Modeling and Management of Discrete Surface Mount Packages, Motorola document BR1487/D Rev 1.
4. “Thermal Characterization of the SO–8 Package for Power Semiconductor Applications”, Kent Kime, Mike Lissy, Dave Shumate, Larry Walker, Thermal Modeling and Management of Discrete Surface Mount Packages, Motorola document BR1487/D Rev 1.





1:1 Images of PCB Artwork

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