AN1582
Application Note

Board and Interface Design for AutoBahn™ Spanceiver™ (MC100SX1451FI50/100)

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This application note provides detailed information about board design and interface circuits for the AutoBahn Spanceiver.

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'Spanceiver' has been formed as a contraction of Serial/Parallel Transceiver.

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Board and Interface Design for AutoBahn Spanceiver

Interface Circuits

The following circuits describe different ways how to build up a data transmit or receive interface to the AutoBahn Spanceiver. All timings refer to a data register access. That means that REGSEL (Pin29) is high.

All calculations and timings refer to 100 Mbyte/s datarate and a 32 Bit wide interface.

Tx – Interface

A data write access to the Spanceiver, places the data in the transmit register. To write to the Spanceiver, the R/W signal (Pin 28) has to be low.

Transmit Handshake

The FULL signal (Pin 31) reflects the status of the transmit register. If the register is full the FULL signal is high. As soon as the PISO shift register is empty the data moves from the transmit register to the PISO shift register, and empties the transmit register. As a result FULL goes low.

This elastic buffer architecture enables a high flexibility on the write access cycle time.

The following timing shows the behavior of the FULL signal as a result of an asynchronous STRB signal, asserted with minimum delay after FULL de–assertion.

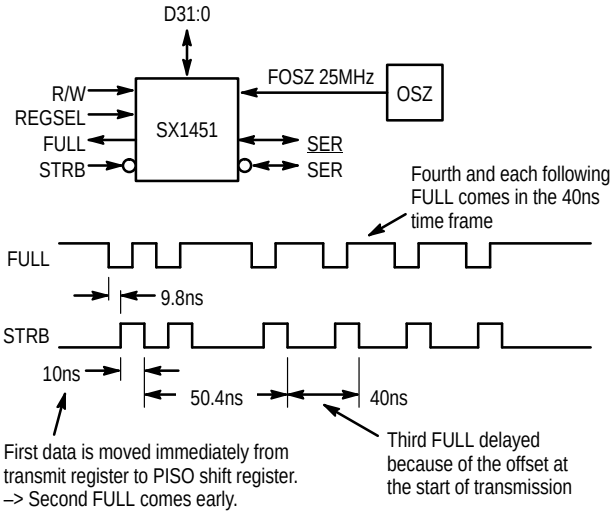

Figure 1. Transmit Handshake

The falling edge of STRB writes the data into the transmit register, which leads to an assertion of FULL after approx. 10 ns. The de–assertion of STRB is a precondition for the de–assertion of FULL. FULL is de–asserted at the earliest 6.8 ns after STRB rising edge.

Asynchronous Interface

The normal handshake requires that the de–assertion of FULL (empty transmit register) leads to a renewed assertion of STRB for maximum datarate.

Actually that is not required in every case. Due to the presence of the elastic buffer, the data can be written into the transmit buffer without the risk of overloading the buffer, as long as the datarate of the write access is exactly the same as the Spanceiver is running at. That is the case as long as the clock source of the Spanceiver (25MHz oscillator at FOSZ Pin) is the same as the parallel data write access (see Figure 2). The jitter between the clock trees can be easily equalized in the elastic buffer.

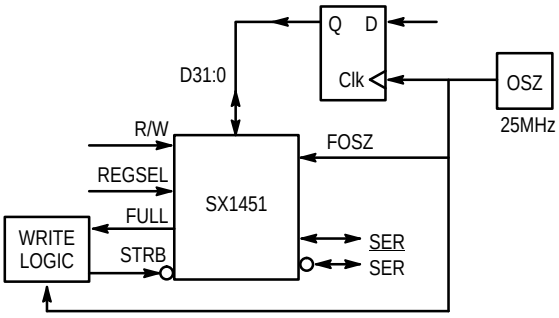

Figure 2. Single Clock Source

The absolute time difference, which can be equalized in the Spanceiver elastic buffer can be calculated as follows:

A two step deep buffer means, that after the first write access, the first buffer step remains empty. Assuming the transmission would start immediately the duration of one transmit cycle could be equalized. In case of the Spanceiver the transmission offset has to be subtracted.

T_{cycle} = 40 ns

$T_{overhead} = T_{strb\_to\_differntial} + T_{startuppulse}$
= 9.9 ns + 15 ns
= 24.9 ns

$T_{elastic\_buffer} = T_{cycle} - T_{overhead}$
= 15.1 ns

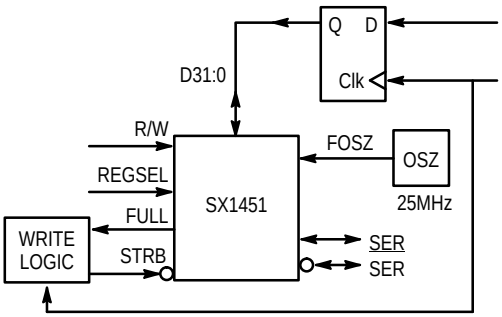

Figure 3. Dual Clock Source

Even in the case of two different clock sources for Spanceiver and the write access logic, a certain amount of data can be transmitted without the risk of overloading the Spanceiver buffer (see Figure 3).

The amount of data, which can be transmitted in one burst before overloading can be calculated as follows:

Assume two oscillator clocks with an accuracy of:

±100 ppm.

1 cycle ≅ 40 ns ≅ 4 Byte

(100Mbyte/s 32Bit)

100ppm * 40 ns = 4ps

That means the maximum difference between two cycles is:

$T\Delta = 8$ ps

$Cycle_{max} = T_{elastic\_buffer}/T\Delta = 15$ ns/8 ps = 3750

$Data_{max} = 3750 * 4$ Byte = 15 Kbytes.

Synchronizing to External Clock

In some cases, where two de–coupled clock sources have to be used, the limitation of the maximum data burst might be critical. The circuit in Figure 5 describes a way to work with two different clock rates.

The basic idea of the circuit is to write in the data until the elastic buffer is completely filled up. Then the logic will insert a wait state of one cycle which leads to an emptying of the Tx–register. Then the write access can continue until the buffer is filled up again.

The write control logic is enabled with a low at /EN. The external clock is provided at CLK_EXT.

Due to the fact, that the read access out of the data source (SRAM, Latch) has to be stopped during the wait state cycle, a RD_CLOCK signal is generated.

The functional timing (see Figure 4) explains, how the circuit works. Using an external clock with a slightly higher datarate than the Spanceiver is capable to transmit, leads to the effect, that the elastic buffer fills up. That is shown by the increasing pulse width of the FULL signal. The pulse width of the FULL signal determines the preset pulse at the STRB flip–flop. If it matches the rising edge of a external clock cycle, no STRB pulse will be generated for one cycle (wait state). Now the elastic buffer empties again.

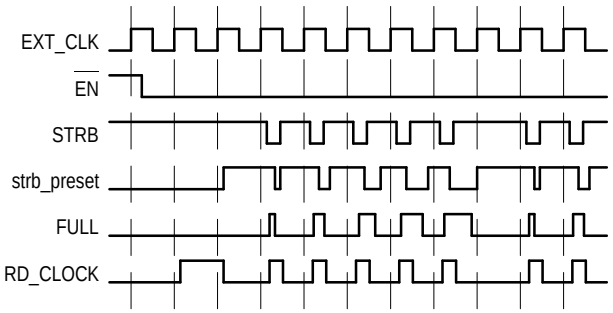

Figure 4. Tx External Clock Synchronization

How this circuit interfaces to the system is shown in Figure 6. The RD_CLOCK is used to trigger the read access to a SRAM (i.e., MCM6206D–12). The external clock latches the SRAM data at every rising edge. That provides a stable 20 ns data window matched to the STRB signal (see Figure 7).

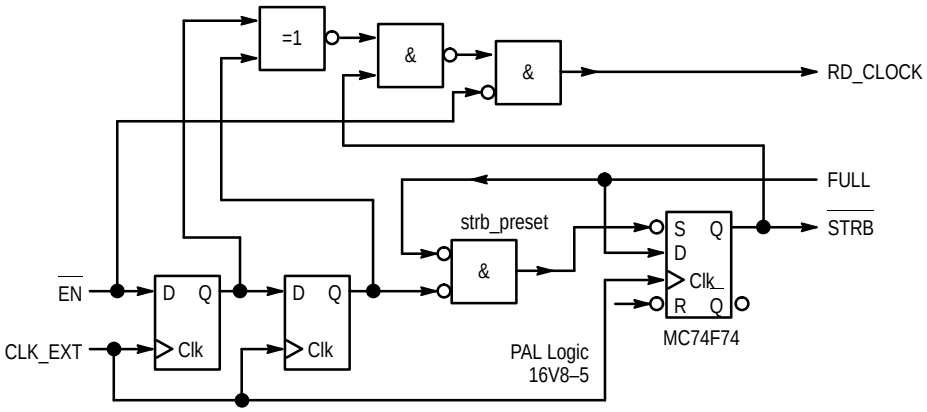

Figure 5. Tx External Clock Synchronization

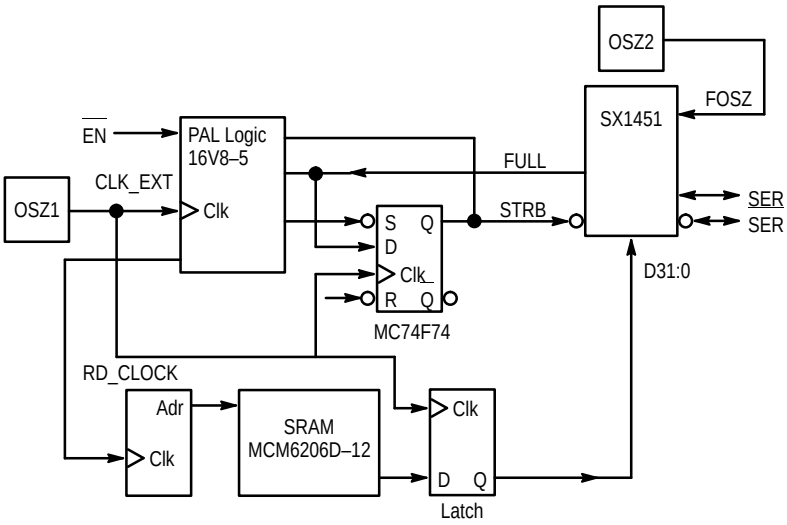

Figure 6. Tx External Clock Sync System Design

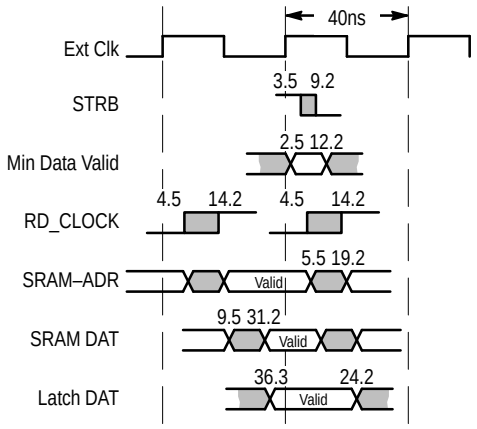

Figure 7. Timing for SRAM Access

Rx – Interface

A data read access to the Spanceiver, reads the data out of the receive register. To read from the Spanceiver, the R/W signal (Pin 28) has to be high.

Receive Handshake

The FULL signal (Pin 31) reflects also the status of the receive register. If the register is full the FULL signal is high.

As soon as the SIPO shift register is filled up with serial data the data moves from the SIPO shift register to the receive register. As a result, the FULL signal is asserted to high.

The falling edge of STRB reads the data out of the receive register which leads to a de–assertion of FULL after approx. 6.8 ns.

A low level at STRB enables the data output drivers. If STRB is de–asserted to high, the data drivers go to high impedance state. The output drivers are optimized to drive a capacitive load of 50 pF. If the D31..D00 data lines are connected to a CMOS type latch or buffer using a not–terminated bus, the data will be stable on the bus until the next data word is driven on the bus.

Asynchronous Interface

The receiving Spanceiver produces FULL pulses according to the datarate of the transmitting side up to the maximum speed of 40 ns. For the receive data the Spanceiver acts as clock master.

The easiest and fastest way to generate read STRB pulses is to feed back the inverted FULL signal.

Receive – Data Clock Generation

Additional to the STRB generation for satisfying the handshake an appropriate data latch signal is required to latch the data in the external data sink.

The purpose of the following circuit is to provide an asynchronous latch signal, according to the receive datarate.

Due to the fact, that every external clock at FOSZ pin runs asynchronously to the receive FULL, a latch signal derived from this clock, won't be able to serve the full datarate.

The basic idea of the interface circuit is to use the next FULL signal to latch the data. In case of a burst with full speed that works perfectly, due to the fact, that the next STRB assertion, which will place new data onto the bus is derived from the FULL signal. There are two exceptions. Utilizing this concept there is a missing latch signal for the last word of a burst and in case of lower speed transmission the gap between the reading STRB pulse and the next FULL pulse for latching the data could be too long to get valid data.

So the idea is to use either the rising edge of the external clock, if it occurs in an appropriate window or to use the next FULL signal.

That ensures that at a transmission with 100 Mbyte/s the data will be latched at least every 40 ns and that the last word is latched using the next appropriate clock edge. The circuit is shown in Figure 8.

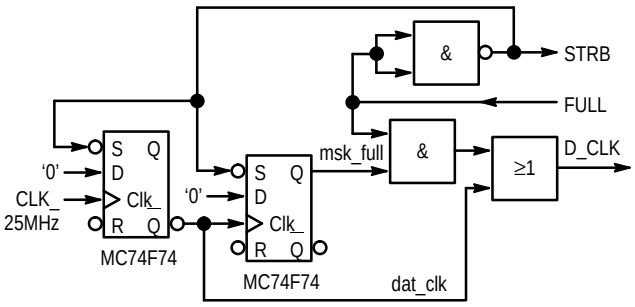

Figure 8. Receive Data Clock Generation

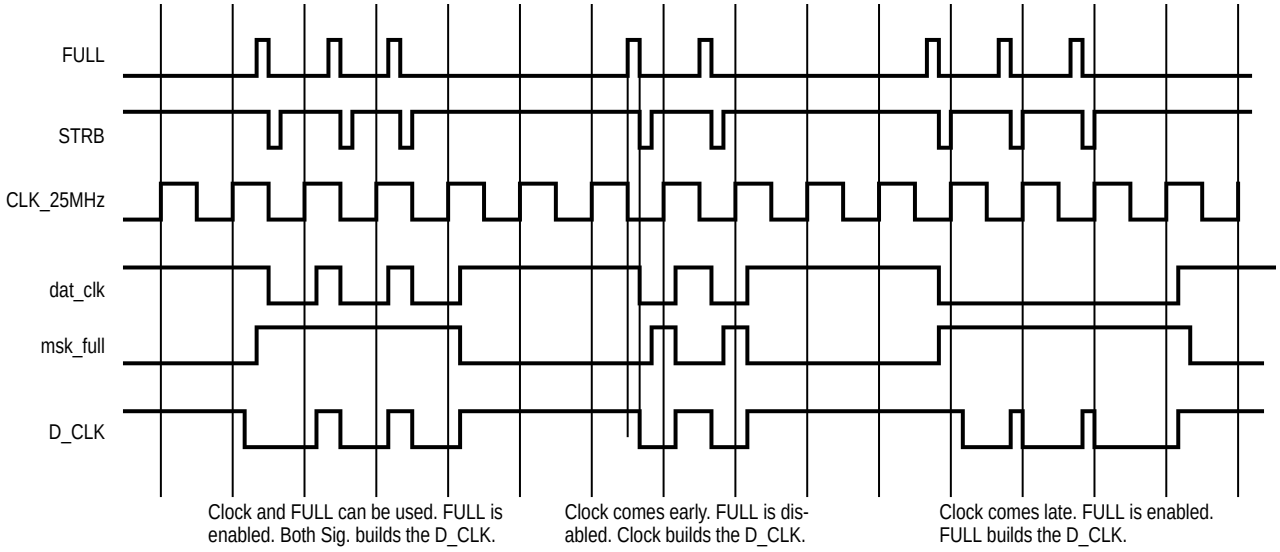

Figure 9. Rx Data Latch Signal

The timings explain the different cases, in which the circuit can work (see Figure 9).

As a precondition, it is assumed that the data bus is not loaded with a DC load like a resistor termination and that it is distributed to a CMOS type latch. So the data will be stable after deassertion of STRB for a certain time.

The whole system solution is shown in Figure 10.

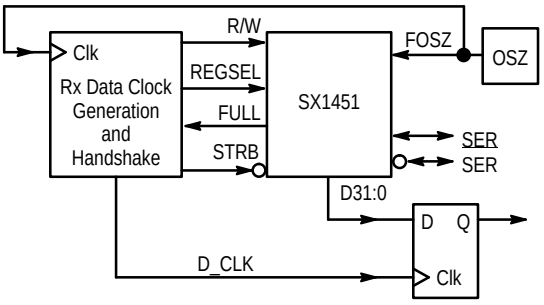

Figure 10. Rx Data Processing

Power Supply

Providing a Stable Voltage Supply

In every design, where signals are distributed using single ended techniques, common–path noise voltage appears. Though AutoBahn is using differential transmission line techniques with best robustness against this type of noise at the serial side, the parallel TTL level IO's and the reference clock are affected by common path noise voltage phenomena.

The common path noise can be considered as a virtual voltage source added between the ground connections of two IC's. In the Spanceiver case between the Data source, the control logic and the reference oscillator clock.

What is the root cause of noise voltage between ground? The main contributor to this noise is high speed return signal currents. The returning signal current driven through the ground impedance generates the common path noise voltage.

(1) To reduce this common path noise, it is mandatory to use low–impedance ground connections.

In addition to common path noise generated at the impedance of the ground plane, noise can also also be generated at the inductance of the supply wires.

During the high state of a gate the output voltage depends on the supply voltage. Any voltage bounces at the supply wiring caused by return currents affects one to one the output signal.

(2) Also the impedance between the supply pins has to be as low as possible.

Due to the fact that every signal return current flows through the power supply, here is additional source to generate supply voltage swings.

(3) To get a stable supply level a very low impedance path between ground and power supply is required.

The constrains (1) – (3) leads to the following recommended power and ground plane system:

(a) Use separate planes for power and ground.

(b) Perform the connection to the planes using direct vias from the IC pad to the supply or ground plane.

(c) Provide a low–impedance path between power and ground by bypass capacitors.

Power Supply Schemes in Mixed TTL/PECL Designs

Since PECL devices are top rail referenced it is imperative that the V_{CC} rail be kept as noise free and variation free as possible. To minimize the V_{CC} noise of a system liberal bypassing techniques should be employed.

AutoBahn designs are normally mixed TTL/PECL designs. The PECL and TTL power supply has to be isolated as much as possible to keep the large current spike noise away from the Spanceiver.

(1) The ideal implementation would be a multiple power plane solution. Two dedicated PECL V_{CC} and ground planes and two dedicated TTL/CMOS V_{CC} and ground planes.

(2) However, if these extra planes are not feasible due to board cost, TTL/CMOS and PECL can share one common solid ground plane. If you have separated +5V for TTL and PECL the TTL noise can hardly couple into the PECL system.

(3) If separated power supply planes cannot be used, a reduction of noise leakage can be achieved in the following way: The ECL and TTL area should be physically separated. Divide the +5V supply plane into a TTL section and a PECL section. Keep one commonly used ground plane!! Connect the TTL side to the power supply. Connect the PECL supply area via 1µH inductors to the TTL supply area. The inductor has to be able to carry sufficient current. In this case supply the reference oscillator from the PECL supply area though it is a TTL part.

Layer Stacking and Board Layout

Ground and Power Plane Stacking

For AutoBahn designs it is recommended to stack the power and ground layers directly together. That maximizes the capacitive coupling and leads to the lowest impedance for high speed signal return currents.

Only use additional ground planes to separate routing layers. Otherwise if power and ground planes are used, the return current has to travel through various bypass capacitors.

Keep in mind that the high speed signal return current follows the path of least inductance.

Layout Constraints

All layout recommendations have one common goal:

To achieve the best possible noise margin on the serial data and clock recovery.

The serial data–stream is derived from a high speed and high precise bit clock. This transmit bit clock is generated using a PLL. Every jitter on the bit clock leads 1:1 to jitter on the serial data–stream. On the receiving side a receive bit clock, which is self aligning to the middle of the data window, is provided to sample the serial incoming data.

Transmit clock jitter and the resulting jitter of the data stream plus the receive clock jitter reduce the remaining data retiming window (noise margin).

(1) Jitter and noise on the reference clock system leads 1:1 to jitter at the receive and transmit clock. That reduces the noise margin of the serial data and clock recovery. For getting best performance and lowest bit error rates it is required to generate a stable and clean clock reference. Therefore an oscillator as specified in the Spanceiver datasheet is mandatory. The clock path to the Spanceiver should be as short as possible. That will help to minimize crosstalk to the clock tree. If possible avoid additional loading of the clock tree. Best performance will be achieved if the oscillator is supplied with the PECL power supply system.

(2) To avoid any crosstalk to the sensitive high speed clock generation circuits in the Spanceiver, it is a good idea to avoid any routing of switching TTL signals under the Spanceiver.

(3) If you don't need to control some of the signals like REGSEL, R/W, RESET, or some of the databits D00..31, make sure that every signal is driven all the time with a low impedance driver. High Ohm resistors connecting the inputs to ground or V_{CC}, or tri–state condition at these inputs will lead to an injection of noise which again reduces the noise margin of the serial data and clock recovery.

(4) Avoid every type of impedance mismatch at the connectors, the transmission media or the cabling.

Serial Interconnection

In general there are two ways how to implement a serial interconnect between Spanceiver's. A point to point link, perhaps using coaxial cabling and a multipoint link.

In both cases a transmission line design is required to interface to the Spanceiver.

Point to Point Application

For establishing a point to point connection no additional circuit is required. The Spanciever has a built–in capability to drive up to 10 meters of coaxial cable.

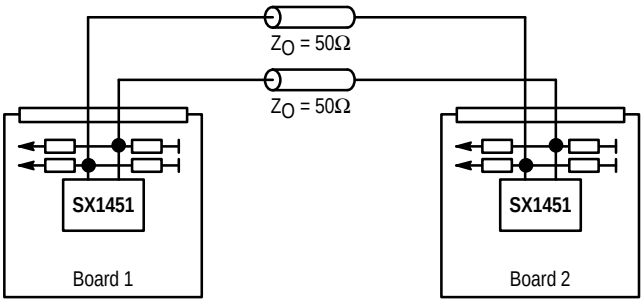

Figure 11. Spanceiver Point–to–Point Application

Multipoint Application

For establishing a multipoint connection the ABSD is required. The ABSD (MC100SX1452) is a bi–directional serial bus driver. It will separate the impedance controlled bus from the stub line to the Spanceiver.

The ABSD allows the build up of impedance controlled serial transmission systems with a constant load independent of how many nodes are connected to the system.

The stub line from the serial bus to the ABSD has to be as short as possible.

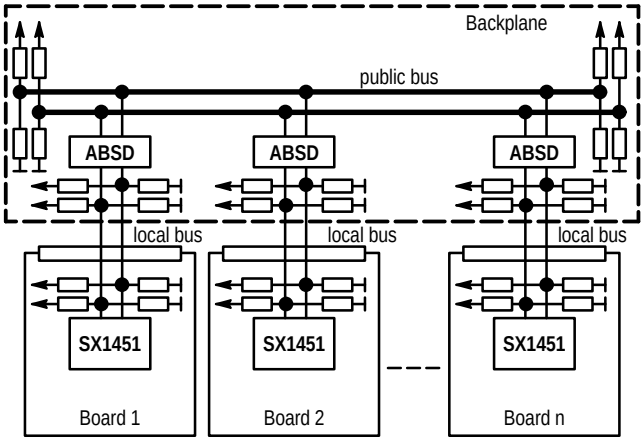

Figure 12. AutoBahn System with ABSD–Chip

Termination Scheme

There are two ways of terminating the serial line.

In case of a point to point connection the serial lines are terminated at both ends, with a parallel termination of 50 Ohm to +3V.

In case of a serial bus system, the serial transmission lines are terminated at both ends with a parallel termination of 50 Ohm to +3V. The single ABSD chips are connected directly via very short stub lines to the serial bus system. There is no termination at the ABSD!

For large systems where total power is a consideration, the lines are normally terminated to a +3Vdc supply. For power conservation, this is the most efficient manner of terminating the serial bus system.

An alternative approach is to use a resistor divider. R1 is connected to +5V and R2 is connected to ground.

In case of the 50 Ω impedance of the serial transmission line, R1 is equal to 81Ω and R2 is equal to 130Ω.

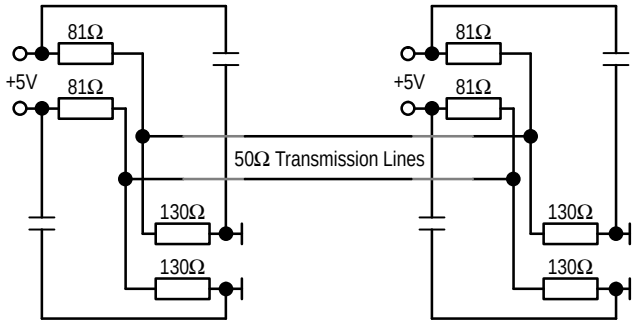

Figure 13. Termination Scheme

Transmission Line Design

A transmission line as used with AutoBahn technologies is a signal path that exhibits a characteristic impedance. Coaxial cables and twisted pair lines have a defined characteristic impedance.

AutoBahn applications require that type of signal path implemented at a printed circuit board. These signal paths, having a closely controlled transmission line impedance, are so called microstrip and stripline (see Figure 14).

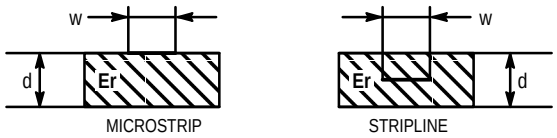

Figure 14. Stripline and Microstrip Parameters

There exists a set of formulas to calculate the geometries to achieve a certain impedance.

Based on the assumption of a FR–4 substrate with Er=4.5 the following two formulas can be used to receive a 50 Ω impedance.

(1) In case of a microstrip:

$$w = 2 \times d$$

with d := dielectric thickness
w := line width

(2) In case of a stripline:

$$w = d / 3$$

with d := dielectric thickness
w := line width

(3) In case of a microstrip there is a more general formula:

$$Z_O = \frac{87}{\sqrt{E_R + 1.41}} \times \ln\left(\frac{5.98 \times d}{0.8 \times w} \right)$$

with d := dielectric thickness
w := line width

Thermal Management

All integrated circuits, including the high speed PECL IC's like the AutoBahn Spanceiver have maximum allowable junction temperature limits. The Spanceiver assembled in the ceramic package has a maximum junction temperature $T_{J(max)}$ of 150°C, for a 10 year lifetime.

That leads to the following maximum allowable ambient temperature:

$$T_A = T_J - P_D \times \Theta_{JA}$$

$T_{J(max)}$	Θ_{JA}	Air Flow	$T_{A(max)}$
150°C	32°C/W	0m/sec	70°C
150°C	23°C/W	2m/sec	92.5°C

P_D = 2.5 Watt Spanceiver Power dissipation
Θ_{JA} = Thermal resistances junction to ambient

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