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APPLICATION NOTE

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Understanding and Predicting Power MOSFET Switching Behavior

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The best way to predict a MOSFET's switching speed is not by using an RC time constant or the concept of the Miller capacitance. RC time constants and Miller capacitance have their uses, but they are usually not appropriate for the selection of a power MOSFET's gate drive resistor. Before we discuss the preferred method of gate drive design, let's look at the problems of using RC time constants and Miller capacitance. Since using an RC time constant is the easier prey, let's take a look at it first.

Authors of books and papers commonly suggest using the formula t_r or $t_f = 2.2\, R_g\, C_{iss}$ as a first pass estimate of gate voltage rise and fall time. Of course, the idea is to estimate the 0 to 90% transition time by using the time constant established by the gate drive impedance and the MOSFET's input capacitance C_{iss} (the parallel combination of the gate-to-source capacitance and the gate-to-drain capacitance). The formula is inappropriate for use with power MOSFETs because the MOSFET's input characteristics are poorly modeled by a single gate-to-source capacitor.

One problem is that the magnitude of C_{iss} changes during switching. But more importantly, using a simple RC model ignores the large amount of charge required by the drain-to-gate capacitance when the drain-to-source voltage changes. Using 400 pF as the C_{iss} of an MTP2N50 (a 2 A, 500 V MOSFET) and setting R_g equal to 200 Ω, the gate voltage rise or fall time is estimated to be 176 ns, far from the 850 ns seen in **Figure 1**. Even if the gate voltage transition time is known, it gives little information about the more important drain-to-source voltage switching time. Amazingly, by coincidence, the drain-to-source voltage rise time in **Figure 1** is very close to 176 ns. This is probably why the method has enjoyed popularity even though it has little basis in fact.

Using the concept of the "Miller" capacitance is a better approach in that it can account for the charge required by C_{dg} due to the changing V_{ds}. The Miller capacitance is not a physical capacitance, but a fictitious one placed in parallel with C_{gs} (not gate-to-drain). Since it models the effects of C_{dg}, C_{dg} is removed from the equivalent circuit when the Miller capacitance is inserted.

The Miller capacity is equal to $A_V\, C_{dg}$, where A_V is the voltage gain, $\Delta V_{DS}/\Delta V_{GS}$. For a resistive load A_V is equal to $-g_{FS}\, R_L$. During switching the gate drive sees an effective input capacitance equal to $C_{gs} + |A_V\, C_{dg}|$. The apparent increase in capacity is due to the large amount of charge required by C_{dg} during the drain-to-source voltage rise or fall time. The effective value of C_{iss} is then used in the calculations of gate voltage rise and fall times.

Several problems make using the Miller capacitance difficult or inappropriate in a typical motor controller or power supply. First, during the turn on and turn off delay, voltage gain is zero and the effect of the presence of C_{dg} is lost. Second, the magnitude of C_{dg} varies by about 50 fold during switching, making selection of an average value difficult. Third, voltage gain is defined in terms of a resistive load. In a power supply or a motor controller, the MOSFET usually switches an inductive load. Because of the square load line and the shape of the MOSFET's output characteristics, the gate-to-source voltage changes very little as the drain-to-source voltage rises. Therefore, at turn-off A_V and the Miller capacitance approach infinity, which makes estimating transition times very awkward.

The presence of the inductive load at first appears to complicate matters and dash any hope of having a simple method of calculating drain-to-source voltage rise time. However, adopting an alternate approach that capitalizes on the nature of the load makes the selection of a gate drive resistor quite simple.

Understanding and predicting the MOSFET's switching behavior is complicated only in that the above methods divert attention from the real issues. A key concept is that in most power applications the load line at turn-on and turn-off is approximately square since the load is inductive and the inductor is clamped in some manner by a catch diode. From the simple solenoid drive circuit to the full bridge motor controller or power supply, each contains the basic inductor/rectifier combination.

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Not surprisingly, then, switching transistors of power systems often have similarly shaped load lines. At turn-off the load line is square since the inductor ensures that the transistor current will remain high until the drain-to-source voltage peaks. At turn-on the transistor switches at zero current if the coil current is discontinuous or for continuous coil current it clears a rectifier's reverse recovery charge and takes on the load current, which again squares up the load line.
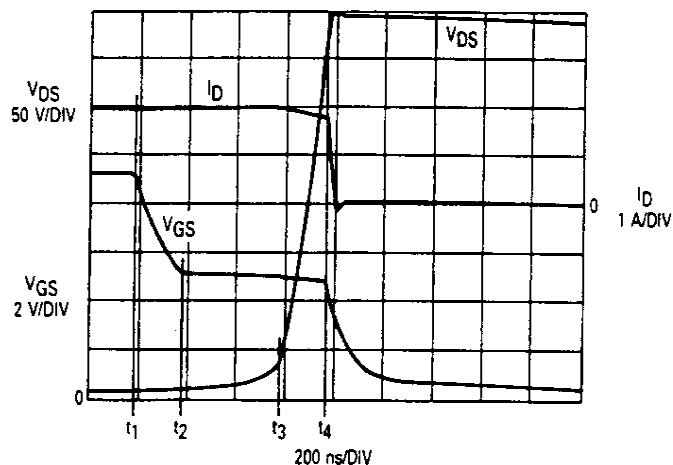

Figure 1. Turn-Off of the MTP2N50
I_D = 2 A, Clamp Voltage = 400 V, R_G = 200 Ω
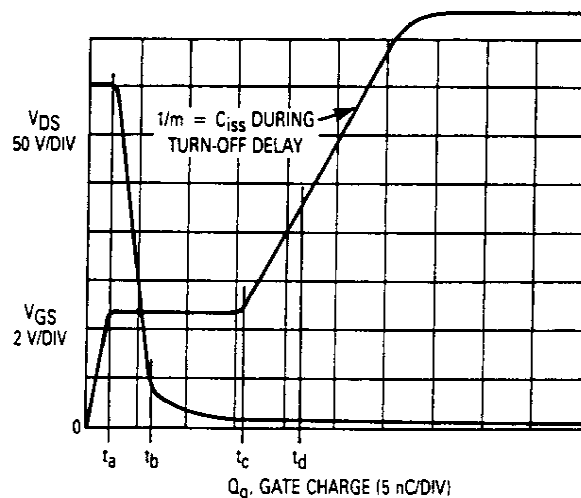
Figure 2. Gate Charge Waveforms of the MTP2N50
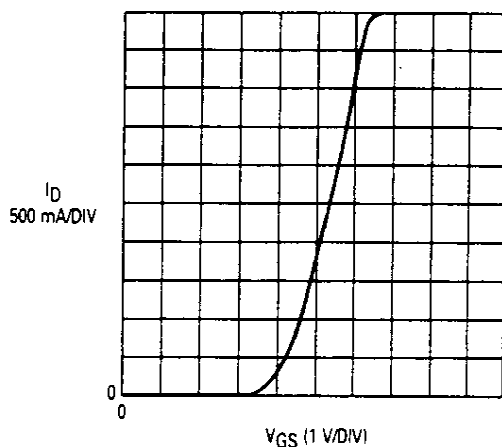
Figure 3. Transfer Characteristics of the MTP2N50
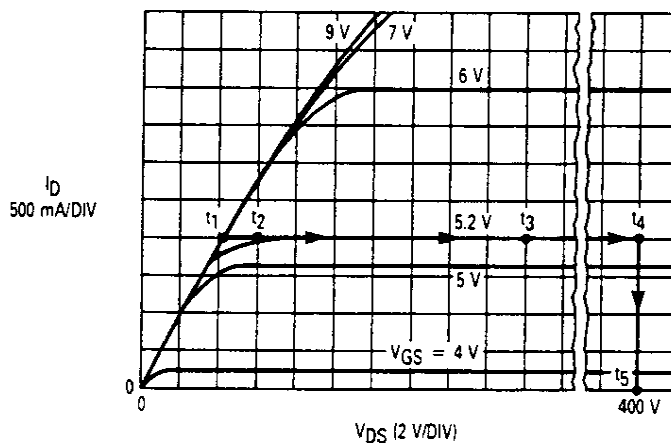
Figure 4. Output Characteristics of MTP2N50 and Load Line During Turn-Off of a Clamped, Inductive Load

The waveforms shown in **Figure 1** and the gate charge curve of **Figure 2** serve as guides to analyzing turn-off of an inductive load. In this example the MOSFET's drain voltage is clamped to 400 V, and the test device is the MTP2N50. The gate drive is the MC34151 (a high performance power MOSFET driver with very low output resistance) feeding a 200 Ω series gate resistor.

In **Figure 1** the gate voltage falls from the 9 volts gate supply to about 5.2 volts before the drain-to-source voltage begins to rise. The gate-to-source "plateau" voltage is significant and predictable since 5.2 volts in **Figure 3** corresponds to the 2 A load current. **Figure 4** shows that the operating point moves from t_1 to t_2 during this precursor to turn-off.

Since C_{dg} takes on very large values when the MOSFET is on, the magnitude of C_{iss} is high during the turn-off delay. Unfortunately, very few manufacturers characterize C_{iss} or C_{dg} under these conditions (Motorola data sheets have complete characterization of C_{iss} and C_{dg}). If C_{iss} data is not available, it can be calculated from a standard gate charge curve. During the turn-off delay C_{iss} is equal to the reciprocal of the V_{gs} curve's slope on the highest portion of the curve. For example, in **Figure 2** C_{iss} is $\Delta Q/\Delta V$ = 5 nC/4 V = 1250 pF. During the turn-off delay (t_1 to t_2), the fall of V_{gs} can be predicted by

$$t_{delay(off)} = \left| R_g\, C_{iss} \ln\left(1 - \frac{\text{plateau voltage}}{\text{supply voltage}}\right) \right|$$

if the final gate voltage is about zero volts. Using a plateau voltage of 5.2 V and a supply voltage of 9 V, t_{delay} is 215 ns, which is in close agreement with the actual turn-off delay time in **Figure 1**.

When V_{ds} starts to rise, it initially rises so slowly that the first portion of the rise time could arguably be included in the definition of the turn-off delay time. The reason for the leisurely rise is that the value of C_{rss} in this region is very high. You can predict this time in a couple ways, but the simplest is to use the gate charge curve — if the V_{DS} waveforms are also shown.

As the drain voltage rises, the load line passes through points t_1 to t_4, and almost all gate charge enters C_{dg} since V_{gs} is virtually constant. The unchanging gate-to-source voltage assures a constant gate current equal to the plateau voltage divided by the gate resistance, in this case 5.2 V ÷ 200 Ω = 26 mA. The constant i_g allows use of data from the gate charge curve and the formula Q = it to determine charging time. The charge of interest here is the 8 nC needed to move from t_b to t_c in **Figure 2**, resulting in an estimate of 308 ns. If the gate charge curve does not include the V_{ds} waveform, it is best to assume that the charge from t_a to t_b is roughly equal to that of t_b to t_c.

With respect to switching losses and noise concerns, the 10% to 90% V_{ds} rise time is by far the most important. Since V_{gs} is still essentially constant from t_3 to t_4, the gate current at turn off is the 26 mA calculated above. However, now the required charge is 4 nC (from t_a to t_b in **Figure 2**), which gives an estimated drain voltage rise time of 4 nC ÷ 26 mA = 160 ns. Again the estimated time is very close to actual performance.

A similar analysis can be used for turn-on behavior. The major differences are: 1) during the turn on delay time C_{iss} is equal to the reciprocal of the first slope of the gate charge curve and 2) the gate current during the plateau region is equal to the gate supply voltage minus the plateau voltage divided by the series gate resistance. The above method works well for the most common applications. Conditions that alter the actual switching time are: inductance in the source circuit, on-voltage of the transistors in the drive IC, drain-to-source snubbing networks, etc.

An additional benefit of this method is that the designer gains a greater understanding of how the MOSFET switches. For instance, it becomes clear that adding gate-to-source capacitance may not slow the drain-to-source voltage rise time. Adding 100 pF to the gate drive circuit above increased turn-off delay time, but did not alter switching speed. Placing the same 100 pF from drain-to-gate more than doubles V_{ds} rise time.

Brushless motor control circuits which PWM the transistors for speed control are another example of a situation where the concepts are useful. Assume that in a 3 phase system the upper transistors are switched at a low commutation frequency determined by the motor and that the lower three transistors are switching at 20 kHz. The tendency is to build a high speed gate drive for only the lower transistors. However, as V_{ds} changes on a lower device, an upper device experiences a V_{ds} change of equal magnitude and opposite polarity. The dv/dt also appears across the upper MOSFETs drain-to-gate capacitance. If the upper transistor does not have a gate drive impedance equivalent to that of the lower, the upper device may partially turn on, briefly pass shoot through currents, and increase switching losses.

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