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Basic Thermal Management of Power Semiconductors

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Thermal management of power semiconductors is often overlooked by design engineers, either through oversight, misconception, inexperience, or even perceived unimportance. Then it is only addressed when the system is ready for packaging and by that time, it may be too late. Because of the need in maintaining the junction temperature of these semiconductors as low as possible to ensure increased reliability, understanding thermal management becomes very important. Thus it is the intent of this article to provide the basics of thermal management, its meaning, significance, characteristics and measurements.

Reliability, service life and performance of a semiconductor device is a direct function of its junction temperature. A rule of thumb is that for every 10°C rise above 100°C, the operating life of the device will be halved. It is imperative that the device run as cool as possible, within cost-performance constraints; the heat sink cannot be unlimitedly large nor excessively expensive.

STEADY STATE THERMAL RESISTANCE

Power ratings of semiconductors are based on the maximum junction temperature which in turn, is dictated by its thermal resistance. When power is applied to the semiconductor, the junction temperature will rise to a value based on the power dissipated at the junction and the ability of the device and its heat sink to conduct this heat away. A steady-state (average) condition is reached when the heat generated equals the heat conducted away. Thermal resistance is thus a measure of the ability of the semiconductor device and its package for removing heat away from the junction. It can be expressed by the equation:

$$T_J - T_R = P_D R_{\theta JR}$$

where:

T_J = Junction Temperature

T_R = Temperature at reference point

P_D = Power dissipated at the junction

$R_{\theta JR}$ = Thermal resistance from junction to the temperature reference point.

Figure 1 describes the basic steady-state thermal resistance model showing the thermal to electrical analogy. Note the similarity to Ohm's Law: temperature "T" could be thought of as voltage, thermal resistance as electrical resistance, power dissipation "P_D" as current and the ambient temperature "T_A" as a battery.

The temperature at any reference point in the loop can be determined when the individual thermal resistances are known. For example, if the reference is the semiconductor case, all related subscripts become "C" (for case), and the equation for junction temperature becomes:

$$T_J = P_D R_{\theta JC} + T_C$$

If the reference is the ambient temperature T_A, then:

$$T_J = P_D R_{\theta JA} + T_A$$

where $R_{\theta JA}$ is the sum of all the thermal resistances:

$$T_J = P_D (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A.$$

$R_{\theta JC}$ is the semiconductor thermal resistance junction to case,

$R_{\theta CS}$ is the interface thermal resistance case to heat sink,

$R_{\theta SA}$ is the heat sink thermal resistance sink to ambient.

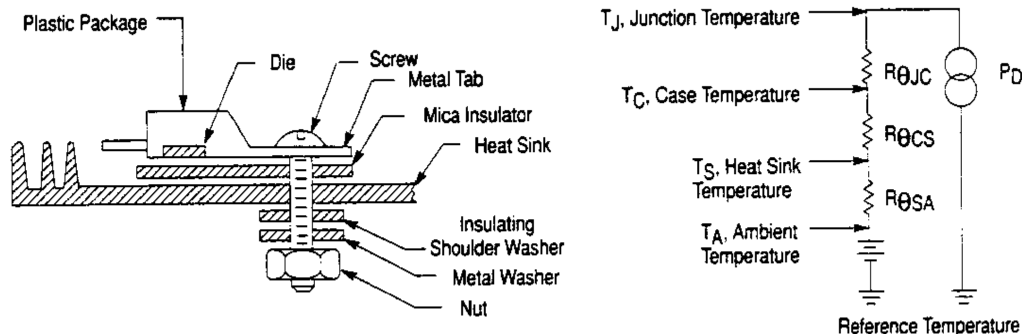

Figure 1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy For a Semiconductor

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MAXIMUM RATINGS				
Rating	Symbol	MJE13008	MJE13009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current - Continuous	I_C	12		Adc
- Peak (1)	I_{CM}	24		
Base Current - Continuous	I_B	6		Adc
- Peak (1)	I_{EM}	12		
Emitter Current - Continuous	I_E	18		Adc
- Peak (1)	I_{EM}	36		
Total Power Dissipation @ $T_A = 25°C$,	P_D	2		Watts
Derate above 25°C		16		mW/°C
Total Power Dissipation @ $T_C = 25°C$,	P_D	100		Watts
Derate above 25°C		800		mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to +150		°C

THERMAL CHARACTERISTICS			
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Figure 2A. Thermal Specifications For the MJE13009

Each thermal resistance must be minimized if the lowest junction temperature is to be achieved at a given power level. Although each element might be thought of as a constant, that's not quite the case. $R_{\theta JC}$ is the value specified on the device data sheet, presumably worst case, with enough margin built in to accommodate a production spread of devices. Even for the same transistor, the thermal resistance $R_{\theta JC}$ derived from a constant power dissipation but different voltage-current products can vary by as much as 10%. Normally the bias for a transistor (V_{CE} and I_C) is chosen where the current density is uniform (i.e. low V_{CE}, high I_C); for higher V_{CE}, the current density becomes less uniform and higher $R_{\theta JC}$ can result.

The interface thermal resistance $R_{\theta CS}$ can also vary due to different mounting pressures, heat sink surface finish, non-flatness of the semiconductor case and non-uniformity of the insulator, if used.

Heat sink thermal resistance is affected by the orientation of the sink (horizontal or vertical) and the ambient temperature ($R_{\theta SA}$ decreases somewhat as T_A increases).

BIPOLAR POWER TRANSISTOR THERMAL CHARACTERISTICS

Once the thermal resistance $R_{\theta JC}$ and/or $R_{\theta JA}$ is known, the power dissipation P_D of the package can be calculated. Take the example of the plastic package TO-220, NPN power transistor MJE13009 specification shown in Figure 2A. Perhaps one of the most misunderstood parameters is the total power dissipation P_D spec. For this device, whose maximum operating temperature is 150°C, the P_D is specified at 100 W when the case temperature T_C is maintained at 25°C. What this implies is that the transistor is mounted on an infinite sink, certainly not a realistic or practical situation. The second P_D spec is where the ambient temperature T_A is 25°C and P_D is rated at only 2 W. This condition implies a free-air mounting and would be the maximum power capability of the device if it were soldered into a printed circuit board without a heat sink. The real world is usually somewhere in between. Both specifications are derated with temperature at 800 mW/°C and 16 mW/°C respectively. Figure 2B shows the typical thermal derating curve being derated down to zero at a case temperature of 150°C.

At a case temperature of 100°C, for example, the transistor can dissipate 40 W and still maintain T_J at 150°C. Recall that P_D is derived from a measured (and derated) $R_{\theta JC}$ (or $R_{\theta JA}$). For this transistor, $R_{\theta JC}$ is specified as 1.25°C/W. P_D thus becomes:

$$P_D = \frac{T_J - T_C}{R_{\theta JC}} = \frac{150°C - 25°C}{1.25°C/W} = 100\ W$$

In actuality, P_D is rounded off to the nearest whole number and the $R_{\theta JC}$ specified is based on that number; the result of 1.25°C/W shows three figure accuracy. As will be shown later, the measured thermal resistance is accurate and repeatable at the best to only two figures.

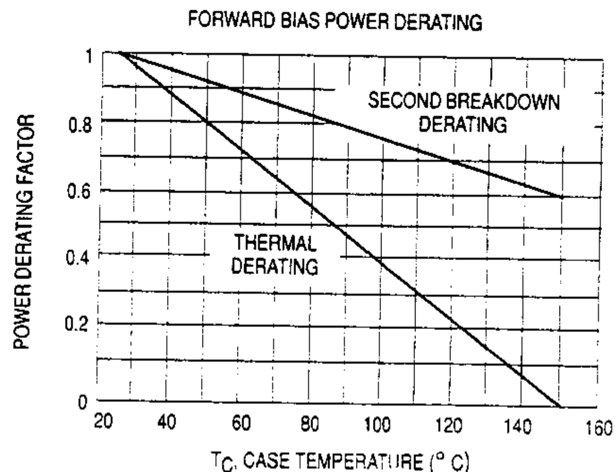

Figure 2B. Thermal Derating Curve For the 100 W MJE13009 TO-220 High Voltage Transistor

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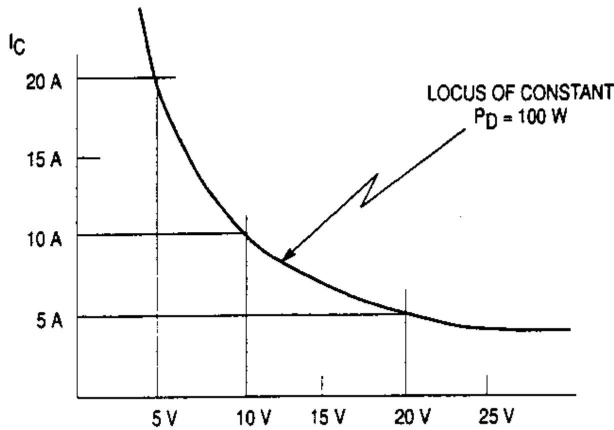

Figure 3A. Linear-Linear Plot of Constant P_D

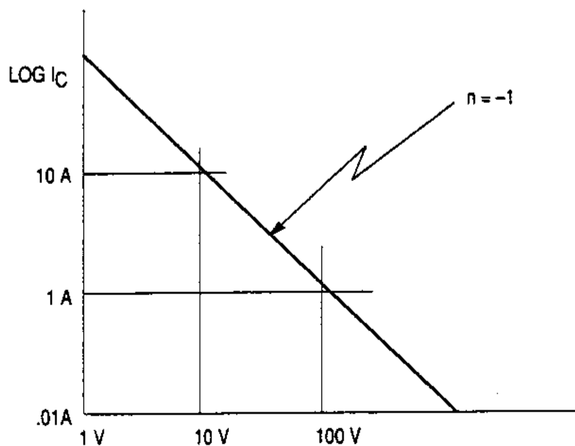

Figure 3B. Log-Log Plot of Constant P_D

Figure 3A shows the locus of constant DC power dissipation on a linear-linear plot resulting in the hyperbolic function:

$$I_C = \frac{P_D}{V_{CE}}$$

When this curve is replotted on a log-log scale, Figure 3B, the constant power curve results in a straight line with a slope n of –1. The example of Figure 3 describes a transistor with a power dissipation of 100 W (10 V, 10 A; 100 V, 1 A). In actuality, this constant P_D seldom extends to the high voltage rating of a bipolar power transistor, as shown by the Active Region Safe Operating Area curves of Figure 4 (also known as Forward Bias Safe Operating Area, FBSOA). The dashed portion of the DC curve and the 1 ms and 100 µs pulsed curves represent the locus of constant power when the case temperature is maintained at 25° C. Under these conditions, these portions of the curves are the thermal limits whereby the junction temperature T_J is 150° C, the maximum operating temperature.

Second breakdown limits – shown by the solid lines – occur at the higher voltage, lower current portion of the curves and will greatly reduce the power handling capability of the transistor. These empirically derived curves are obtained through destructive testing of many transistors to determine their V_{CE}, I_C limits. Simply stated, FBSOA second breakdown results from current crowding around the periphery of the emitter finger when the transistor is turned on. Under these extreme bias conditions, a hot spot is created which ultimately burns through the transistor die, destroying the device.

Note that there are no thermal limits for the 100 µs pulse, that it is only second breakdown limited. Of interest is that these second breakdown curves were generated from a common-base configuration where V_{CE}, I_C and the pulse width are made variable. This configuration is also used in measuring thermal resistance.

The other two limits shown in Figure 4 are the maximum voltage rating V_{CEO} of the transistor and the maximum collector current I_C. The current is both a bonding wire limit for the DC curve and h_{FE} limit for the pulsed curves.

POWER MOSFET THERMAL CHARACTERISTICS

Since power MOSFETs are, in theory, immune to second breakdown their FBSOA curves are somewhat different than bipolars: there are no second breakdown limitations, only the thermal limits of the constant P_D curves. Consequently, all curves will be the constant P_D slope of –1, straight lines extending to the voltage breakdown rating BV_{DSS}.

For some power MOSFETs, at the high voltage, low current portion of FBSOA, the parasitic transistor second breakdown susceptibility might lower the curve. There is however, an $r_{DS(on)}$ limit which truncates the low voltage, high current portion of FBSOA. It is simply due to $V_{DS(on)}$ being equal to I_D ($r_{DS(on)}$), thus limiting the FET's on-voltage.

The maximum current limits, like the bipolar power transistor are dictated by the bonding wire and gain of the device.

TRANSIENT THERMAL RESISTANCE, r(t)

Another point of interest is the thermal response curve shown in Figure 5. The lower curve, the single pulse, is empirically derived by measuring the temperature effects with time of the transistor's base emitter voltage V_{BE} to a power

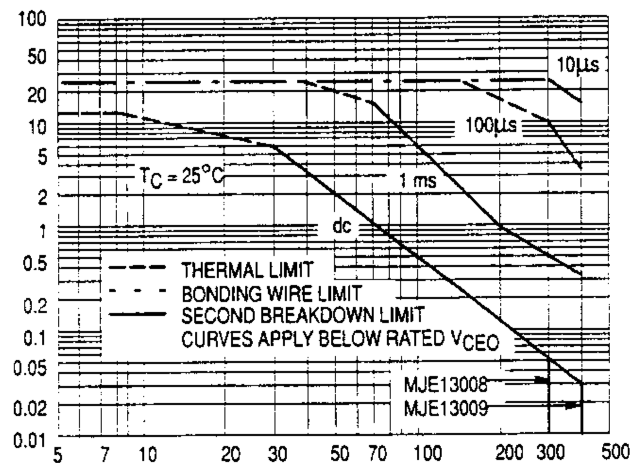

Figure 4. Forward Bias Safe Operating Area

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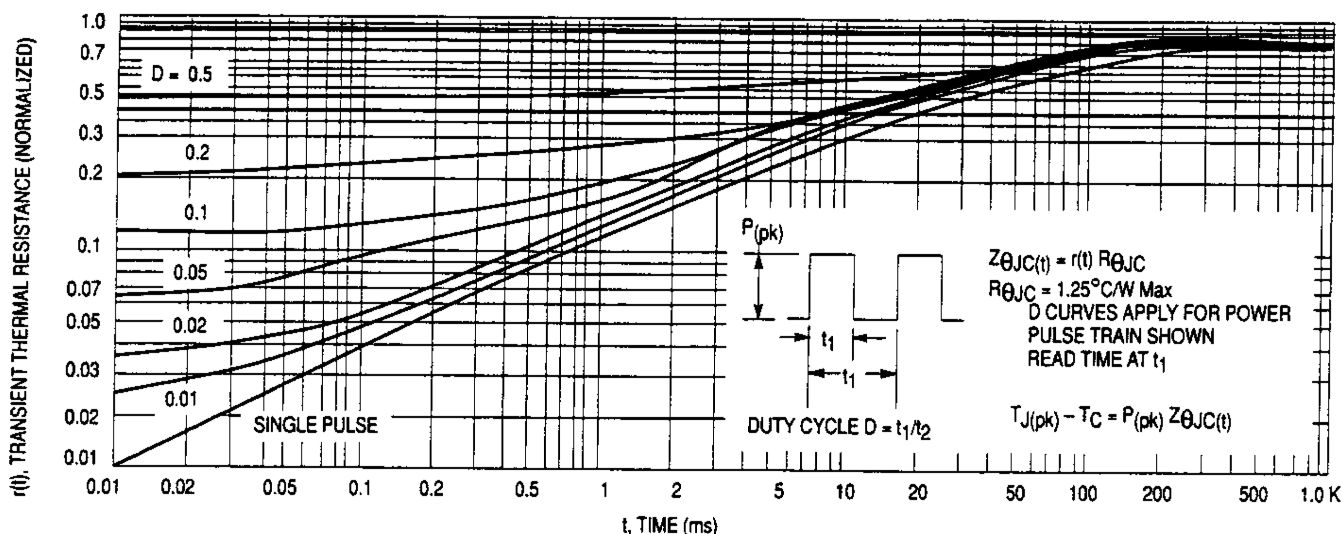

Figure 5. Typical Thermal Response ($Z_{\theta JC}(t)$)

pulse. Although not shown in Figure 1, the complete thermal resistance model would have thermal capacitances associated with each thermal resistance node. Each capacitance, with its resistance, would thus relate to the thermal response of that portion of the network, similar to the RC time constant of its electrical analog.

To measure the transient thermal resistance r(t), the transistor is self-heated by a power pulse of about ten seconds and then V_{BE} is measured during a cooling period with samples taken from 20 µs to as long as ten seconds. This r(t) data is then normalized to 1.0 and plotted on multi-cycle log paper as a function of time. The remaining duty-cycle curves are mathematically derived through superposition techniques (for details, please refer to Motorola Application Note AN569, Transient Thermal Resistance - General Data and Its Use). The end result is that the thermal impedance $Z_{\theta JC(t)}$ is now equal to:

$$Z_{\theta JC}(t) = r(t)\, R_{\theta JC}$$

and the complete thermal equation (referenced to the case) is:

$$T_{J(pk)} - T_C = P_{(pk)}\, Z_{\theta JC}(t)$$

The significance of this is that the transistor can sustain for narrow pulses much greater peak power than the steady-state case; in fact, from the above equations, this peak power capability is inversely proportional to r(t). For example, if a 0.5 ms, 20% duty cycle pulse were applied to this 100 W transistor, from the curves r(t) equals about 0.085 and thus 100 W/0.085 or about 1180 W of peak power could be dissipated when an infinite heat sink is used. Under these conditions, the junction temperature would be the rated temperature of 150°C.

As can be expected, the thermally limited portion of the pulsed FBSOA curves are related to thermal response curves. Referring to the 1 ms thermally limited curve of Figure 4, the peak power results in about 900 W (60 V, 15 A). Figure 5 shows for a 5 ms single pulse curve (FBSOA is derived with less than 10% duty cycle pulses) r(t) equals about 0.11. Consequently,

$$P_{(pk)} = 100\ W/0.11 = 909\ W.$$

The two figures are in agreement.

The curves also relate to the response of the various elements of the transistor package. For example, short times are associated with the thermal response time of the die, medium times from about 10 ms to 100 ms relate to the die-header interface and larger times, for the package. It is for these reasons that the narrow pulse, peak power capability of the same die in two different packages will be the same.

To carry this one step further, the steady state thermal resistance of different sized die encased in the same package are not the same. It is not too surprising that larger die produce lower thermal resistance as the test data points of Figure 6 show. A best straight line through these approximately 40 different bipolar transistors and power MOSFET's housed in the TO-220 package illustrates this.

The deviation of some of these data points from the straight line can possibly be attributed to many factors including different test times and operators, different packaging materials and

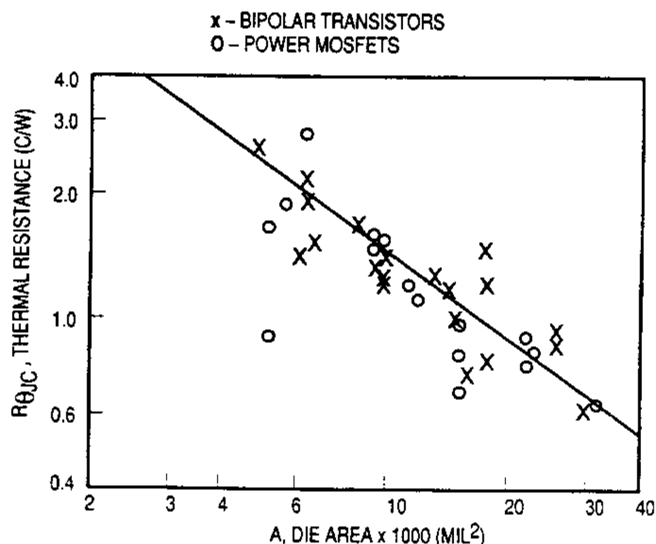

Figure 6. Thermal Resistance RθJC Junction to Case of TO-220s as a Function of Die Area

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different mounting techniques.

STEADY STATE THERMAL RESISTANCE MEASUREMENTS

Using Temperature Sensitive Parameters – TSP

There are several methods of measuring thermal resistance of semiconductors, each one with their own trade-offs. For example, a fairly accurate IR scan requires complex and expensive instrumentation. Also, the device die has to be exposed through decapping or depotting the package which certainly does not facilitate production testing. A more common, simpler and production amenable technique, but one that is not quite as accurate as the IR scan, uses the Temperature Sensitive Parameter – TSP – of the DUT itself. Semiconductor junctions have this feature. Thus by knowing how this parameter behaves to an elevated temperature, the junction temperature, when powered, can be indirectly determined and the thermal resistance derived.

In order to determine the thermal resistance of any semiconductor device, an accurate and repeatable method of measuring the device temperature is required. The linear temperature dependence of the on-voltage of a forward biased semiconductor junction has proven to be a reliable parameter and is consequently used for bipolar transistors (emitter-base or collect-base junctions), rectifiers, zeners, and thyristors. Because of their intrinsic D-S diode, this technique is also applicable to power MOSFETs.

These semiconductor junctions have a negative temperature coefficient of about 2mV/°C. A typical temperature derating curve, that of an avalanche rectifier surge suppressor, is shown in Figure 7. Note that for this device the slope m is:

$$m = \frac{610 \text{ mV} - 320 \text{ mV}}{50\ ^\circ\text{C} - 200^\circ \text{C}} = 1.93 \text{ mV/}^\circ\text{C}$$

When measuring bipolar transistors, the forward biased base-emitter-junction generally is used as the temperature sensitive parameter (the collector is open). This junction is calibrated at an elevated temperature in the forward direction with a low calibration current (I_M) and should be in the linear region above the diode knee. Also, I_M should not contribute significantly to junction temperature; typical values are 2.0 to 100 mA, depending on package type, die size and technology.

Calibration can be performed in a temperature chamber with the temperature set for a normal operating temperature value for the semiconductor being measured. A typical temperature for a silicon die is around 100° C. The base-emitter forward voltage is measured and recorded at I_M and at the calibration temperature.

For information purposes, the room temperature readings can be noted and if required, a calibration curve can be drawn through the two points.

SIMPLIFIED BIPOLAR THERMAL RESISTANCE TESTER

After calibration, a bipolar power switching fixture (Figure 8) is used to alternately apply and interrupt the power to the test device. The transistor is operated as a common-base in the active region and power dissipation can be adjusted by varying I_E and/or V_{CE} until the junction is at the calibration temperature. This condition is known by monitoring the base-emitter voltage during the time when I_M only is flowing with either an oscilloscope or a sample-and-hold circuit. When V_{BE} is equal to the value obtained in the calibration procedure, the junction temperature is known. The case temperature is noted at this time as well as I_E and V_{CE}.

The heating period is long, so the temperature of the transistor case is stabilized and the interval of power interruption short, usually 300 µs, so junction cooling will be minimal.

Although not shown in the simplified circuit of Figure 8, a PNP power transistor placed in series with the collector of the DUT is often used. This transistor is synchronized with the emitter switching transistor, thus allowing only I_M to flow through the DUT emitter-base during the sense period. This was also the case during temperature calibration.

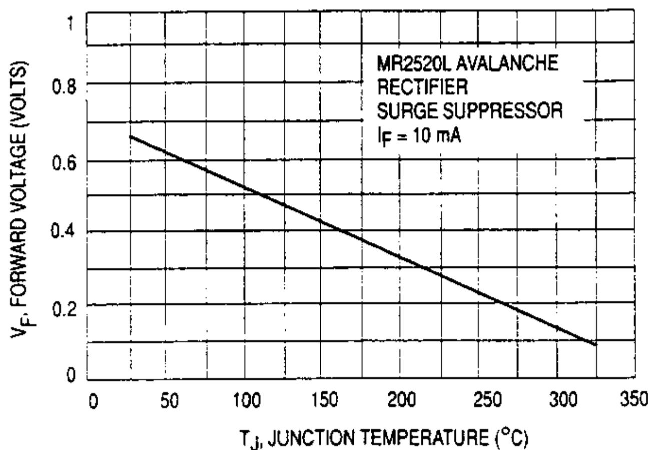

Figure 7. Temperature Calibration Curve of the MR2520L

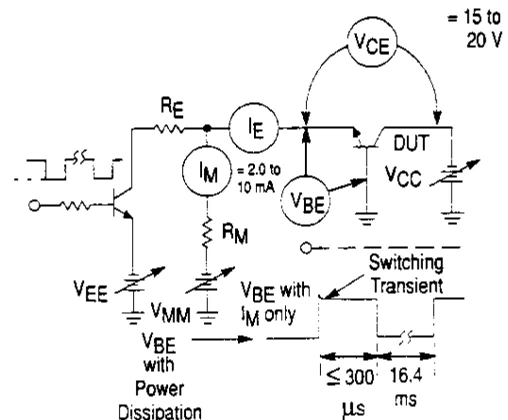

Figure 8. Basic Block Diagram of Steady State Thermal Resistance Test Circuit for Bipolar Transistors

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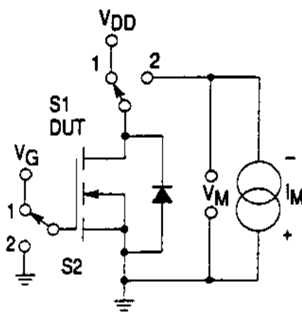
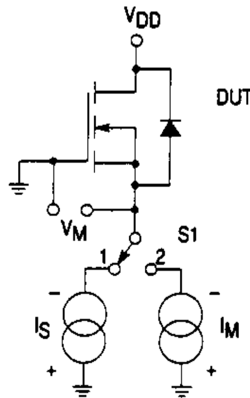
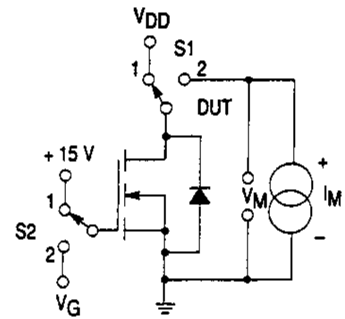


9a. Drain-Source Diode Voltage



9b. Gate-Source Threshold Voltage



9c. Drain-Source On Resistance

Figure 9. Circuit Configurations For Measuring TSP of Power MOSFETs

The steady state thermal resistance can be easily calculated from the information obtained in the calibration and power dissipation procedures. The simple formula is derived from the basic thermal resistance model (Figure 1) showing the thermal to electrical analogy for a semiconductor.

Steady state thermal resistance junction-to-case is as follows:

$$R_{\theta JC} = \frac{T_J - T_C}{V_{CE} \cdot I_E} = \frac{\Delta T}{P_D}$$

For junction-to-case measurements, sufficient heat sinking should be provided to prevent excessive junction temperature. Measurement accuracy is improved with a large temperature delta between the junction and case. This delta can be achieved by using an efficient heat sink permitting power dissipation (I_E V_{CE}) of sufficient magnitude to reach the calibration temperature.

MEASURING POWER MOSFETS $R_{\theta JC}$

When measuring the thermal resistance of power MOSFETs, the gate-source threshold voltage or the drain-source on-resistance $r_{DS(on)}$, can be used in addition to the on-voltages of the drain-source diode. Knowing the temperature characteristics of these parameters - by measuring the voltage or resistance variations with temperature in a temperature chamber as an example - the device temperature when powered can be determined and the thermal resistance can be calculated.

These temperature sensitive parameters of a power MOSFET with their approximate temperature coefficients are listed as follows:

Drain-Source Diode = – 2.0mV/°C

Gate-Source Threshold Voltage = – 2.0 to – 6.0 mV/°C

Drain-Source On-Resistance = + 7.0 mΩ/°C when $r_{DS(on)}$ =1.0 Ω

How these TSP can be measured is described in the simplified schematics of Figure 9, with Figure 9a using the D-S diode, Figure 9b the $V_{GS(th)}$, and Figure 9c the $r_{DS(on)}$.

D-S Diode TSP

Generally, the most often used circuit for measuring $R_{\theta JC}$ of power MOSFETs uses the D-S diode. When electronic switches S1 and S2 are in position 1, the FET is biased on and the heating power ($V_{SD}I_D$) is applied to the FET for a relatively long period. Then the switches are thrown to position 2 for a short period of time (sense time) so the FET temperature will not change appreciably. Next, the FET is turned off and a constant current I_M (the same sense current at which the TSP was temperature calibrated) is applied to the forward biased D-S diode. By measuring the forward voltage drop of the diode and comparing it to the calibration curve, the FET junction temperature can be ascertained. Knowing the input power and the junction temperature, the thermal resistance can be calculated. In practice, the input power, either voltage or current, is varied until the D-S diode drop is equal to a calibration point, thus simplifying the test procedure by not having to generate a complete calibration curve.

Figure 9a shows the simplified schematic for using the D-S diode as the TSP. To power the FET in this open-loop configuration requires adjusting the gate voltage V_G to set the required drain current I_D. With this system there can be some difficulty in setting and maintaining a constant I_D. A better approach, one using a closed-loop around the gate-source is shown in Figure 10. Here, the linear regulator will force the source voltage V_S to be equal to the reference voltage V_{REF}. Consequently, the drain current (and source current) will be a constant (Vs/Rs). Waveforms of this tester are also shown in the figure. The source-drain diode voltage V_{SD} should be measured as close to time t_0 as possible to minimize the cooling of the diode during the sense time. Also, please note that V_{SD} is increasing slightly in magnitude as the S-D diode cools.

(A detailed schematic and circuit description of the D-S Diode Thermal Fixture is described in the Appendix.)

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Gate-Source Threshold Voltage TSP

This thermal resistance test circuit is extremely useful for measuring $R\theta_{JC}$ of IGBT's since this device has no parasitic diode. As in the D-S Diode Tester, heating power is applied to the DUT when switch S1 is in position 1. Then switch S1 is briefly thrown to position 2, applying the sense current to the FET (I_D at $V_{GS(th)}$) and the gate-source threshold voltage is measured. Input power (V_{DS}-I_S) is varied to make $V_{GS(th)}$ equal to the elevated temperature, calibration reading resulting in a known junction temperature and thus $R\theta_{JC}$.

DRAIN-SOURCE ON-RESISTANCE

This circuit is conceptually similar to the D-S Diode Tester. However, now when the switch is in position 2 (Sense Time), a positive constant current I_M and + 15V gate bias are applied to the device, turning it on. I_M should be of a value to produce about 0.5 V V_{DS}. The voltage V_{DS} measured (V_M) is related to $r_{DS(on)}$ by:

$r_{DS(on)} = V_M/I_M$

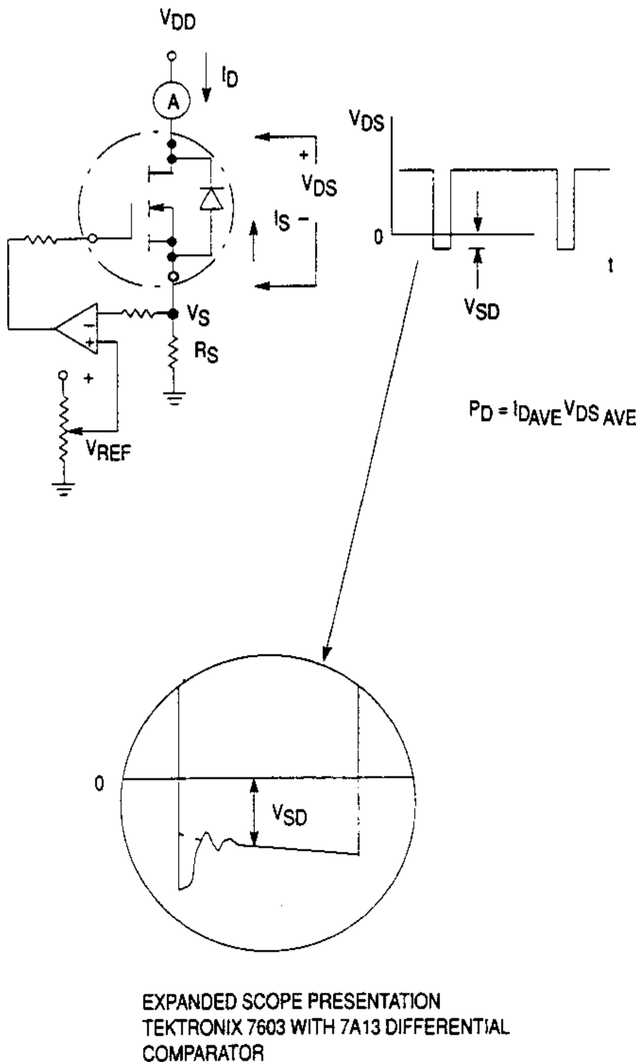

Figure 10. TMOS D-S Diode TSP for $R_{\theta JC}$

RECTIFIER AND SCR SIMPLIFIED CIRCUITS FOR $R\theta_{JC}$

The same drive circuit can be used to power rectifiers and SCRs for measuring $R\theta_{JC}$, as shown by Figures 11a and 11b. Basically all that is required is a transistor switch for controlling up to 200 A for large DUTs during the heating portion of the thermal cycle and a continuously applied sense current loop around the device.

For SCRs (and triacs) a simple, switchable gate circuit is also needed – switch S1 of Figure 11b – to latch on the DUT. Once latched, the SCR will remain on as long as the sense current I_M is greater than the device's holding current with the peak on-state voltage V_{TM} being the TSP.

Since the on-voltages are low – one diode drop for a rectifier and one V_{BE} plus $V_{CE(sat)}$ for the SCR – large heating currents may be required to raise the DUT junction temperature. These large currents can cause regulation problems with the required V_{EE} power supply resulting in high ripple voltage. To "lock" these waveforms on the viewing oscilloscope, it is advantageous to line-sync the driving pulse generator to 60 Hz or 120 Hz; thus, the illustrated $R\theta_{JC}$ testers derive their timing from the AC line. Figure 11c depicts a typical rectifier waveform of V_F. Note that in the time expanded V_F sense waveform, electrical and/or thermal transients can mask the t_0 switching portion of the waveform for tens of microseconds. Consequently, V_F is generally measured through scope viewing or sample-and-hold techniques at 100 µs after the transition time t_0. A more exact method would be to extrapolate the cooling sense voltage waveform to time t_0 and measure V_G at that point.

Thermal Examples

Thermal Resistance Measurements

With the basics of thermal resistance measurements as a background, the best way of describing the calculation of thermal resistance is to actually go through the procedure.

Take for example the following data obtained in measuring $R\theta_{JC}$ for the MTP15N06 (15 A, 60 V)) N channel power MOSFET. The first requirement is to generate the temperature calibration curve. Usually, about six DUT's are placed in the temperature chamber set for about 100°C. The chamber need not be set to exactly 100°C, but whatever temperature it does reach, it should be noted and recorded.

In this case a calibration current I_M of 10 mA is then applied to the forward biased source-drain diode. This is simply accomplished by applying an external (to the chamber) power supply V_M of say +11 V through an external 1 K series limiting resistor R_S to the anode of the DUT diode. Thus,

$$I_M = \frac{V_M - V_F}{R_S} = \frac{11\ V - 1\ V}{1\ K} = 10\ mA$$

For that matter, V_M could be any voltage as long as it is much greater than V_F and therefore will appear as a current source to the diode. Obviously, the limiting resistor must be changed accordingly.

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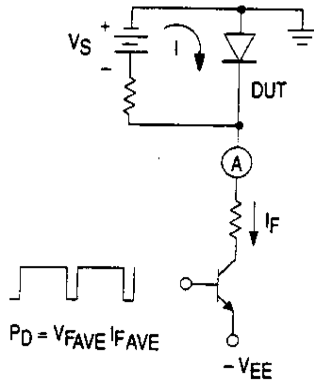
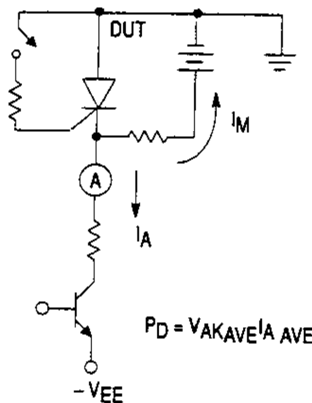
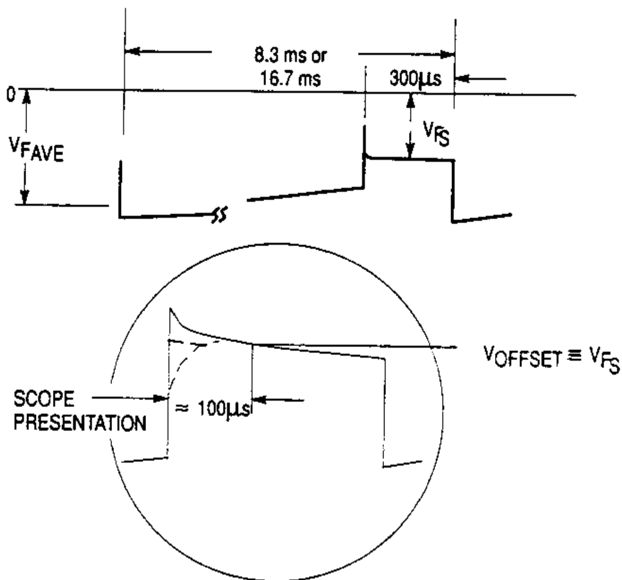
Once the chamber and DUTs have stabilized, the V_F's of the diodes (V_{SD} of the FETs) are read and recorded. This can be done by bringing out of the chamber all six pairs of test leads or using a six position rotary switch that will select the individual diode. If the diode drops are closely matched, then an average reading of the six devices could be used for V_{SD} at elevated temperatures. If not, then each reading should be used for the appropriate DUT thermal measurement. Incidentally, there is nothing sacred about using six DUTs. It could be 5, 10, 12, etc., just enough to give a confident end result.



11a. Rectifier



11b. SCR



11c. Waveforms of On Voltage of DUT

Figure 11. Rectifier and SCR Simplified Circuits for $R_{\theta JC}$

The following brief table illustrates the readings of two power MOSFETs:

V_{SD} @25°C	V_{SD} @100°C	T_C	ΔT	V_{DS}	I_D	P_D	$R_{\theta JC}$
0.556V	0.401V	35°C	65°C	8.66V	3.13A	27.1W	2.4°C/W
0.551V	0.400V	35°C	65°C	8.57V	3.50A	30.0W	2.1°C/W

Some clarification of these numbers is in order.

(1) The 25°C V_{SD} reading is for information only; it is not used in the $R_{\theta JC}$ calculation. The differences between these two readings will produce the derating factor m or slope of the temperature derating curve, e.g.:

$$M = \frac{556\ V - 0.401\ V}{25°C - 100°C} = \frac{-.15\ V}{75°C} = -2.01\ mV/°C$$

(2) Measuring the case temperature is the most critical and most prone to error of all the thermal resistance measurements. A 5°C error in this example, when T_C equals 35°C would produce nearly an 8% error in $R_{\theta JC}$. It would be even greater if T_C were higher (due to a non-infinite heat sink).

One means of obtaining a near infinite heat sink is to use a water sprayed and cooled, four inches by four inches copper plate, 1/4 inch thick, as the heat sink. The DUT is clamped or screwed down to this plate and a spring loaded thermocouple makes close contact to the underside of the device package, directly under the die. The thermocouple could be directed from the underside of the sink through a small hole or perhaps placed in a slot on the top side of the plate. Or a hole could be drilled horizontally in the package to accommodate the thermocouple and placed closely to the die. In any case, it is extremely important that the welded bead (not twisted and soldered) of the thermocouple make solid contact with the semiconductor header directly under the die. (For more information on thermally related mounting techniques, please consult Motorola Application Note AN1040, Mounting Considerations for Power Semiconductors.)

(3) Using the water cooled sink for smaller DUTs requiring lower heating power, T_C would be close to the T_A of 25°C, perhaps 28°C to 32°C. For larger devices, T_C might reach 40 to 50°C. Since the calibration temperature is around 100°C, T_C should be as low as possible so that ΔT (the difference between the calibration temperature and the measured case temperature) is high, thus minimizing the error of taking the difference between two large numbers.

(4) V_{DS} and/or I_D is then varied to force V_{SD} (during the sense interval) to be equal to the V_{SD} obtained in the temperature chamber. I_M should be same as when calibrated. Under these conditions, T_J, by definition, is equal to the chamber temperature.

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Recall that the power is applied for a long period and the sense time is short. For these thermal resistance testers whose switching frequency is 120 Hz and sense time is 300 µs, the high duty cycle becomes:

$$D.C. = \frac{1/120\ Hz - 300\ \mu s}{1/120\ Hz} = \frac{8.3\ ms - 0.3\ ms}{8.3\ ms} \approx 96.4\%$$

Consequently, the power applied to the DUT is an average power and the resultant junction temperature is an average temperature. For that reason, V_{DS} and I_D are average readings obtained with average reading meters.

(5) Knowing T_J, T_C, V_{DS} and I_D, $R\theta_{JC}$ can be calculated:

$$R\theta_{JC} = \frac{T_J - T_C}{V_{DS} I_D} = \frac{100°C - 35°C}{8.66\ V(3.13\ A)} = 2.4°C/W$$

As mentioned previously, T_C is the most difficult parameter to accurately measure (V_{DS}, I_D and V_{SD} are very repeatable when the device mounting pressure is consistent). Just by varying the amount of contact of the thermocouple with the DUT can cause T_C to vary. For this reason, obtaining repeatable $R\theta_{JC}$ from week to week for the same device is considered good if the variation is less than 10%. Consequently, $R\theta_{JC}$ readings should be rounded off to two figures. For this example, where six DUTs were measured and the readings were not "peas in a pod", the highest and lowest readings should be discarded. Then the highest of the remaining should be considered the worst case with an appropriate tolerance, say 20% or 30%, added to it to encompass production variations.

Example of Heat Sink Calculation

For this example, a heat sink has to be selected for cooling an MTP4N45 (4 A, 450 V) power MOSFET operating at a continuous drain current of 3 A. $T_A(max) = 55°C$.

Spec: $R\theta_{JC} = 1.67°C/W$

$P_D = 75\ W$

$(R\theta_{JA} = 62.5°C/W)$

$\left(P_D = \frac{\Delta T}{R\theta_{JA}} = \frac{125°C}{62.5°C/W} = 2\ W\right)$

Given: Insulator $R\theta_{CS} = 0.2°C/W$

MTP4N45: $r_{DS(on)}max] = 1.5\ \Omega$ at 2 A, 25°C

Let: $r_{DS(on)}]\ max = 3\ \Omega$ at $I_D = 3\ A$, $T_J = 150°C$ (from data sheet curves)

$$P_D = I_D^2\ r_{DS(on)} = (3)^2(3) = 27\ W \text{ at } T_J = 150°C$$

$$T_J - T_A = (R\theta_{JC} + R\theta_{CS} + R\theta_{SA})\ P_D$$

$$150°C - 55°C = (1.67°C/W + 0.2°C/W + R\theta_{SA})\ 27\ W$$

$$95°C = (1.87°C/W)\ (27\ W) + R\theta_{SA}\ (27\ W)$$

$$R\theta_{SA} = \frac{95°C - 50°C}{27W} = 1.7°C/W$$

The solution: Consult vendors' specs for heat sinks with $R\theta_{SA} \le 1.7°C/W$.

Example of Calculated T_J Using Finite Heat Sink

Find the junction temperature of a power transistor at a maximum ambient temperature of 55°C when the transistor case temperature is 60°C in an ambient temperature of 25°C. T_C is the result of applying 25 W to the device when mounted on a defined heat sink with insulator and thermal grease.

Given: DUT with $P_D = 25W$

$R\theta_{JC} \approx 1.67°C/W$

$T_A(max) = 55°C$

$T_C \approx 60°C$ at $T_A = 25°C$

$$T_J = P_D\ R\theta_{JC} + T_C \text{ at } T_A = 25°C$$

$$= 25\ W\ (1.67°C/W) + 60°C$$

$$T_J = 102°C \text{ at } T_A \approx 25°C$$

$$T_J\ (\text{at } T_A = 55°C) = T_J\ (\text{at } T_A = 25°C) + \Delta T_A$$

$$= 102°C + (55°C - 25°C)$$

$$T_J = 132°C \text{ at } T_A = 55°C$$

r(t) Example

Find the peak power capability of the MJE13009 power transistor when subjected to a 1 ms, 10% duty cycle pulse.

From the Thermal Response Curve r(t)

at PW = 1 ms 10% D.C.

$r(t) \approx 0.11$

Since $Z\theta_{JC}(t) = r(t)\ R\theta_{JC}$

and $P_{D(pk)} = \frac{\Delta T}{r(t) R\theta_{JC}} = \frac{P_D}{r(t)}$

$P_{D(pk)} \approx \frac{100\ W}{0.11} \approx 900\ W$

Summary

Thermal Management in power conversion applications is extremely important to ensure system reliability. Understanding the basics of thermal management could minimize the problems encountered when this area of design is overlooked. To aid the reader to this end, this article covered the basics of thermal management, its meaning, significance, characteristics and measurements. Included are definitions, data sheet interpretations, calibration of the device temperature sensitive parameters, simplified schematics of thermal resistance testers for bipolars, power MOSFETs, SCRs and rectifiers, and several thermal design examples.

Also described in the following Appendix are detailed schematics of testers for measuring the thermal resistance of power MOSFETs and a universal fixture for bipolars, SCRs and rectifiers.

APPENDIX

Thermal Test Fixtures

D-S Diode Thermal Fixture

$R\theta_{JC}$

The D-S diode Thermal Fixture, shown in Figure 12 is partially an implementation of the simplified circuit of Figure 10. It also contains circuitry for measuring transient thermal resistance r(t) and the analog circuits for reading out the drain–source diode forward voltage and input power (V_{DS} and I_D). Thermal resistance is measured when the Mode Selector

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Figure 12. Power MOSFET D-S Diode Thermal Fixture

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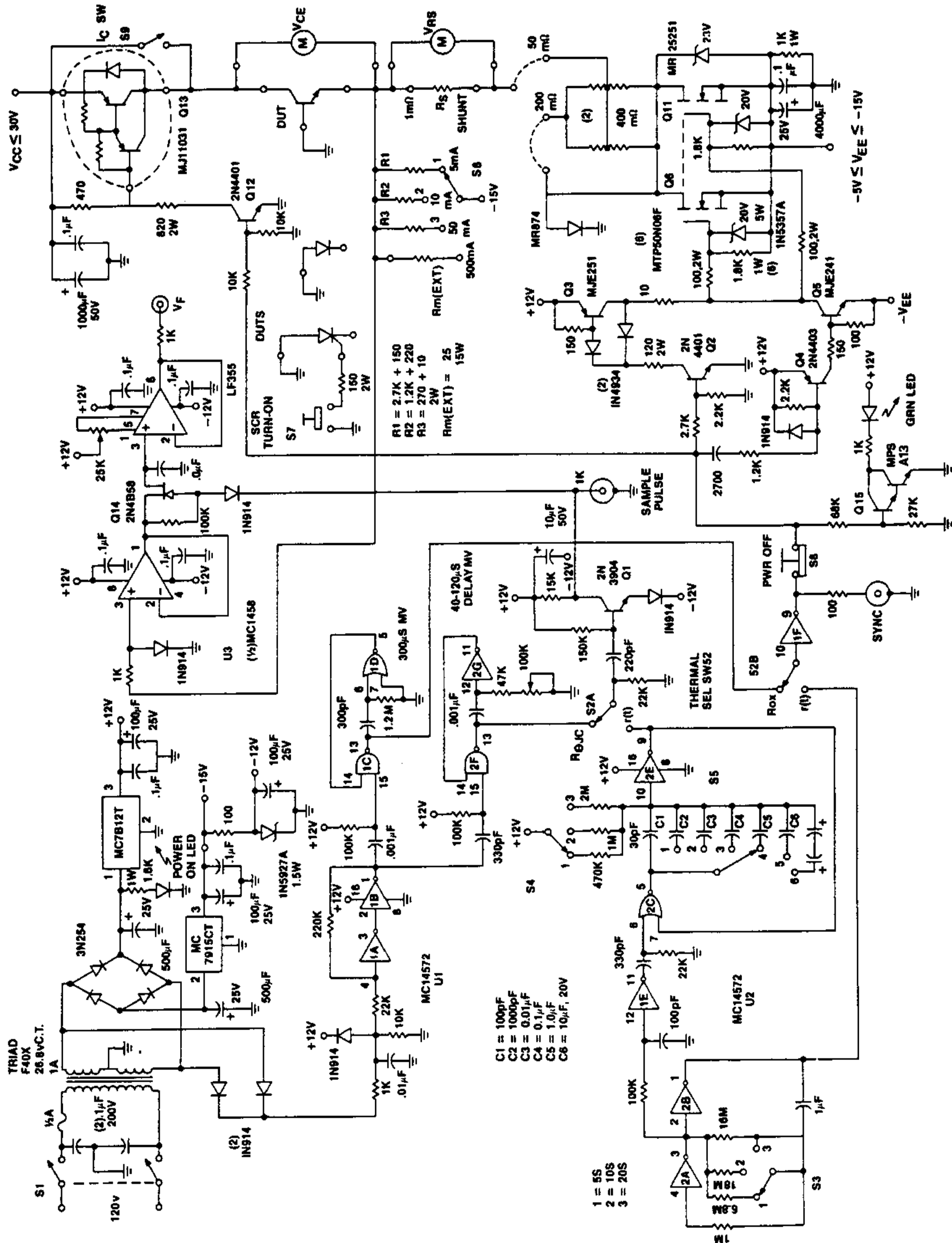

Figure 13. Universal Thermal Resistance Fixture

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Switch S1 is in position 1, $R_{\theta JC}$. System timing is line synchronized and is derived from the Schmitt trigger gates (G1A and G1B) shaping circuit clocking the 300 µs Sense Time Monostable Multivibrator (gates G2A and G2B). Thus, the power MOSFET DUT is turned on via the Drain Switch circuit (cascade transistor Q1 and Q2) and unclamped gate transistor Q3 for 8.0 ms (full-wave rectified line rate minus 300 µs) and off for the 300 µs sense time. Drain current is set and readily controlled by ID Control potentiometer R1 in the gate-source, closed loop, regulator circuit (op-amp U5).

During the sense interval, DUT power is turned off (Q2 is off, Q3 is on) and the sense current I_M is applied to the now forward biased D-S diode by means of turned on transistors Q4 and Q5. The resultant D-S diode voltage can be observed by a scope or measured by the sample-and-hold circuit consisting of series FET switch Q6, buffer amp U6, sample driver Q7 and line synchronized Delay Monostable MV gates G2C and G2D. The Delay Control of this MV allows the sample pulse to be positioned some time after the start of the Sense time so as to measure the settled voltage of the D-S diode, ignoring the possible thermal and/or electrical switching transients on the leading edge of the sense pulse. This delay time is typically 50 µs to 150 µs.

Using similar sample-and-hold circuitry, the applied power ($V_{DS/10}$ and $I_{D/10}$) can be measured. This is accomplished by the respective FETs Q8 and Q9, sample driver Q10, buffer U3A and U3B, and difference connected op-amps U4A and U4B.

Transient Thermal Resistance r(t)

Transient thermal resistance, r(t), is measured when switch S1 is in position 2. Now the system timing is derived by the 22 second astable MV (gates G1C and G1D) which turns the DUT on and off for about 11 seconds each. During the off time, cooling cycle, the voltage of the D-S diode can be measured at any selected period of time. This is accomplished by selecting the various resistor-capacitor timing components of the Delay MV, thus positioning the sample pulse accordingly. The six switchable capacitors, by means of Selector Switch S2, will produce the six time decades of control (100 µs to 10 s) and the three resistors (switch S3), the multipliers within the decade, e.g. 0.2, 0.5 and 1.0.

Universal Thermal Resistance Tester

By combining the features of the bipolar thermal resistance tester with that of the rectifier/SCR tester, a Universal Thermal Resistance Tester was developed, as shown by the schematic of Figure 13. Note the three DUTs in the schematic. When testing rectifiers or SCR's, the heating current flows from ground through the forward biased DUT, a limiting resistor, a high current transistor switch (six parallel connected 50 A, 60 V power MOSFETs MTP50N06E, Q6-Q11) and the variable, negative power supply V_{EE}. Using a high current, low voltage supply, as much as 200A can be switched into the DUT.

When testing bipolar transistors, the collector switch (Q13, PNP Darlington MJ11031) is incorporated with the DUT connected in a common-base configuration. Now, DUT collector current I_C flows from the positive V_{CC} supply, through the collector switch, the DUT, limiting resistor, high power FET switch and the negative V_{EE} supply.

The rest of the circuits provide the gate drive for the power MOSFETs, the CMOS fashioned pulse circuits for both $R\theta_{JC}$ and r(t), the VF sample-and-hold circuits (S/H), and the low level power supplies.

Working backwards from the gates of the power MOSFET, transistors Q2 through Q4 supply the gate drive through the six 100 Ω gate isolation resistors of the six respective FETs. When the 8 ms wide power on pulse is supplied from inverter A5, NPN small signal transistor Q2 and the following PNP medium power transistor Q3 are turned on, thus feeding about 12 V to the gates of the power MOSFETs.

Since the peak current capability of Q12 is fairly high, the FET's total input capacitance C_{iss} will charge up quickly allowing fast load current switching. To quickly turn off the FETs, C_{iss} must be rapidly discharged. This is accomplished by differentiating the trailing edge of the input pulse by means of the RC circuit in the base of the PNP transistor Q4, turning it on and the following NPN transistor Q5. Consequently, C_{iss} discharges through Q5 at a time coincident with the turn off edge of the input pulse.

Clocking for the system is 120 Hz line derived from the secondary of transformer T1 shaped by Schmitt trigger inverters A1 and A2. This output then triggers the 300 µs MV for the Sense period and a variable delay sample pulse generator, gates B5, B6 and transistor Q1. The end result is about a 20 µs sample pulse that is positioned within the 300 µs sense interval for $R_{\theta JC}$ measurements.

The two Op-amps of U3 comprise the two unity gain amps for the S/H with small signal JFET Q14 being the series sample switch. The input op-amp buffers the V_F reading and the output amp is the hold capacitor buffer. Thus, the output DC voltage reading will represent the magnitude of V_F (or V_{BE} for bipolars) at the sample pulse time.

Transient thermal resistance is measured in a similar fashion to the previously described D-S Diode Thermal Fixture. Its timing is derived by astable MV (gates 2A and 2B) clocking the switchable time delay monostable MV (gates 2C and 2E).

$R_{\theta JC}$, Air Cooled Versus Water Cooled

The Universal Thermal Resistance Fixture was packaged with a blower fan and air tunnel to keep the DUT case temperature as cool as possible. For correlation purposes, test devices were measured with both this type of air cooled sink and the cold water sprayed sink. Even though the respective T_C readings varied, the resulting $R_{\theta JC}$'s were quite close, as shown by the table on the following page.

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Table 1. Thermal Resistance Using Forced Air and Water as Cooling Media.

DUT	CASE	T_J (°C)	HEAT SINK COOLING	T_C (°C)	V_{CE} V_F (V)	I_C I_F (A)	$R_{\theta JC}$ (°C/W)
2N3771	TO-3	91.8	WATER	44	27.4	3.31	0.53
			AIR	48	26.13	3.0	0.56
1N3913	DO-5	88	WATER	26	1.189	40.3	1.29
			AIR	46	1.107	29.3	1.29
MUR20010CT	375B	94	WATER	37	0.867	116	0.57
			AIR	44	0.849	97.4	0.61

REFERENCES:

1. Motorola Power MOSFET Transistor Data, DL135 REV 3.
2. Motorola Power Transistor Data, DL111 REV 5.
3. Motorola Application Note AN569, "Transient Thermal Resistance - General Data and Its Use", Bill Roehr and Bryce Shiner.
4. Motorola Application Note AN1040, "Mounting Considerations for Power Semiconductors", Bill Roehr.

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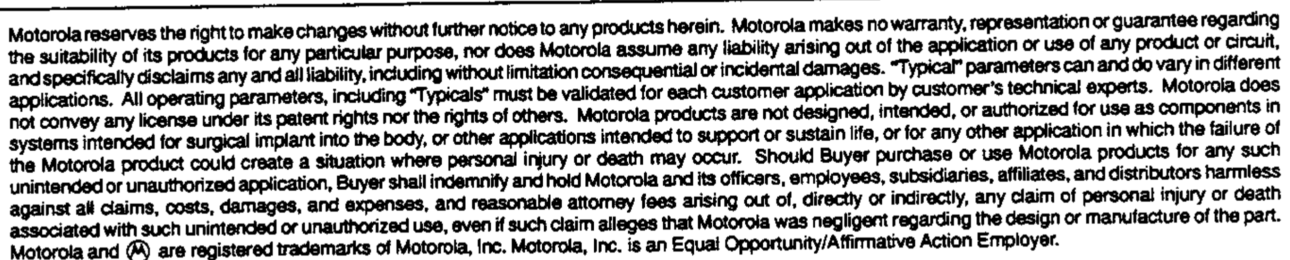
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